Design of a Radiation-Hardened Curvature Compensated Bandgap Reference Circuit

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Thesis to obtain the MSc Degree in Electrical and Computing Engineering

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ABSTRACT

The work present in this thesis belongs to the scientific area of electronic design and dimensioning of analog integrated circuit (ICs), more specifically the design of a bandgap voltage reference – BGV – generator with second order compensation. The developed circuit provides a steady voltage at the output, stable to noise, temperature and power source drifts, which functions as a reference voltage for other circuit blocks. The main purpose of the work is to obtain a BGV generator of a voltage of 1.25V with a performance that can surpass a previous proposed circuit. The figures-of-merit (FOM) that primarily characterize the circuit and that will be the focus of improvement are the PSSR, the TC and the current consumption. The results obtained in the past proposed circuit for typical conditions are a PSRR of -56.54 dB, a TC of 7.75 ppm/°C and a current consumption of 2.34 mA. The circuit presented in this thesis obtained results, in the same conditions, of a PSRR of -81.93 dB, a TC of 2 ppm/°C and a current consumption of 0.737 mA, achieving the main objective. The circuit was developed for XFAB XH035 process technology, using mostly Cadence Virtuoso for drawing and dimensioning the circuit, Mentor Graphics Eldo© for simulation and AIDA C – a tool for integrated circuit dimensioning optimization.

KEYWORDS

RESUMO

O trabalho desenvolvido e apresentado nesta tese pertence à área científica do projecto de circuitos electrónicos analógicos integrados (ICs), mais especificamente no desenho de um circuito de tensão de referencia do tipo bandgap - BGV. O circuito desenvolvido fornece uma tensão estável, imune ao ruído e às variações de temperatura e da fonte de alimentação que funciona como uma tensão de referencia para outros blocos. O principal propósito deste trabalho foi obter um circuito BGV que gere uma tensão de 1.25V e cujo desempenho ultrapassasse o obtida por um circuito anteriormente proposto. As principais figuras de mérito que caracterizam o circuito e que foram alvo de maior foco durante o desenvolvimento são o PSRR, TC e o consumo de corrente. Os resultados obtidos pelo circuito anteriormente proposto para as condições típicas são um PSRR de -56.54 dB, um TC de 7.75 ppm/°C e um consumo de corrente de 2.34 mA. O circuito projectado, nesta tese e nas mesmas condições de referência, apresenta um PSRR de -81.93 dB, um TC de 2 ppm/°C e um consumo de corrente de 0.737 mA, atingindo assim o principal objectivo. O circuito foi desenvolvido na tecnologia XFAB XH035, e como ferramentas de desenvolvimento foi usado maioritariamente o Cadence© Virtuoso para o desenho e dimensionamento do circuito, o Mentor Graphics Eldo© para simulação e o AIDA C – uma ferramenta de optimização de circuitos integrados.

PALAVRAS-CHAVE

Design de Circuitos Integrados Analógicos, CMOS, Tensões de Referência, Tensões de Referência do tipo Bandgap, Resistência à Radiação.
I would like to acknowledge my supervisors Doctor Nuno Horta and Doctor Jorge Guilherme for the guidance and motivation during the development of this work. Thanks to the IT Analog Integrated Systems team, Ricardo Póvoa and Nuno Lourenço for the diligent support and to António, Márcio, André, David, Telmo, Ricardo Martins and Bruno for the companionship.

# CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSTRACT</td>
<td>1</td>
</tr>
<tr>
<td>KEYWORDS</td>
<td>1</td>
</tr>
<tr>
<td>RESUMO</td>
<td>1</td>
</tr>
<tr>
<td>PALAVRAS-CHAVE</td>
<td>1</td>
</tr>
<tr>
<td>ACKNOWLEDGEMENTS</td>
<td>III</td>
</tr>
<tr>
<td>CONTENTS</td>
<td>V</td>
</tr>
<tr>
<td>FIGURES</td>
<td>IX</td>
</tr>
<tr>
<td>TABLES</td>
<td>XI</td>
</tr>
<tr>
<td>ACRONYMS</td>
<td>XIII</td>
</tr>
<tr>
<td>1 INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>1.1 MOTIVATION</td>
<td>1</td>
</tr>
<tr>
<td>1.2 OBJECTIVES</td>
<td>2</td>
</tr>
<tr>
<td>1.3 DOCUMENT STRUCTURE</td>
<td>3</td>
</tr>
<tr>
<td>2 STATE-OF-THE-ART IN BANDGAP VOLTAGE REFERENCES</td>
<td>5</td>
</tr>
<tr>
<td>2.1 BASIC CONCEPTS</td>
<td>5</td>
</tr>
<tr>
<td>2.1.1 PN JUNCTION</td>
<td>6</td>
</tr>
<tr>
<td>2.1.2 BGV CIRCUIT EXAMPLES</td>
<td>9</td>
</tr>
<tr>
<td>2.2 PREVIOUSLY PROPOSED BGV APPROACH</td>
<td>10</td>
</tr>
<tr>
<td>2.2.1 RESULTS</td>
<td>12</td>
</tr>
<tr>
<td>2.3 CURVATURE COMPENSATION</td>
<td>13</td>
</tr>
<tr>
<td>2.3.1 PTAT²</td>
<td>14</td>
</tr>
<tr>
<td>2.3.2 TEMPERATURE DEPENDENT RESISTOR RATIO</td>
<td>15</td>
</tr>
<tr>
<td>2.3.3 II COMPENSATION</td>
<td>15</td>
</tr>
<tr>
<td>2.3.4 PIECEWISE-LINEAR CURRENT MODE TECHNIQUE</td>
<td>16</td>
</tr>
<tr>
<td>2.3.5 MATCHED NONLINEAR CORRECTION</td>
<td>18</td>
</tr>
<tr>
<td>2.4 CIRCUIT COMPARISONS</td>
<td>19</td>
</tr>
<tr>
<td>2.5 CONCLUSIONS</td>
<td>19</td>
</tr>
<tr>
<td>3 CIRCUIT DESIGN</td>
<td>21</td>
</tr>
<tr>
<td>3.1 BASE CIRCUIT</td>
<td>21</td>
</tr>
</tbody>
</table>
A.5 Corner Cases for the 2\textsuperscript{nd} Order BGV Circuit ................................................................. 71

References ................................................................................................................................................. 73
FIGURES

FIGURE 2-1 BASIC CONCEPT OF BGV: PTAT, CTAT AND OUTPUT WAVEFORMS ............................................. 6
FIGURE 2-2 REPRESENTATION OF A SIMPLE BGV CIRCUIT ...................................................................... 7
FIGURE 2-3 BROKAW BGV CIRCUIT [12], .................................................................................................. 9
FIGURE 2-4 AN ALL CMOS BGV TOPOLOGY [7] .......................................................................................... 10
FIGURE 2-5 PREVIOUS PROPOSED BGV CIRCUIT APPROACH [10] ......................................................... 11
FIGURE 2-6 PREVIOUS PROPOSED BGV CIRCUIT APPROACH WITH IMPROVEMENTS [10] .............. 13
FIGURE 2-7 GRAPH REPRESENTING THE CONCEPTS OF PTAT\(^2\) ............................................................ 14
FIGURE 2-8 BROKAW CIRCUIT PRESENTED IN 2.1.2.1 WITH PTAT\(^2\) CIRCUIT IMPLEMENTATION. ........... 15
FIGURE 2-9 II COMPENSATION CURVATURE CORRECTED BGV BLUEPRINT ........................................ 16
FIGURE 2-10 PIECEWISE CURRENT INL GENERATOR. ................................................................................. 17
FIGURE 2-11 MATCHED NONLINEAR CORRECTION PROPOSED CIRCUIT .............................................. 18
FIGURE 3-1 CIRCUIT TOPOLOGY PROPOSED IN [22] ................................................................................. 22
FIGURE 3-2 OTA CIRCUIT SCHEMATIC ........................................................................................................ 24
FIGURE 3-3 BIAS GENERATOR CIRCUIT ...................................................................................................... 25
FIGURE 3-4 2\(^{ND}\) CORRECTION CIRCUIT .................................................................................................. 26
FIGURE 3-5 ELT DRAFT. ................................................................................................................................. 28
FIGURE 3-6 ELT LAYOUT REPRESENTATIONS, WHERE IN A) IS REPRESENTED A CONSIDERED BAD LAYOUT AND IN B) A CONSIDERED GOOD LAYOUT........................................................................ 30
FIGURE 3-7 CASCODE CONFIGURATION TO BE IMPLEMENTED ................................................................. 31
FIGURE 3-8 CLOSE-UP OF THE CASCODE IMPLEMENTATION IN THE MIRROR STAGE OF THE BGV. .......... 31
FIGURE 3-9 OUTPUT FILTER CIRCUIT ......................................................................................................... 32
FIGURE 3-10 TRIMMING RESISTOR ............................................................................................................. 33
FIGURE 3-11 AMPLIFIER WITH ADJUSTABLE GAIN .................................................................................... 33
FIGURE 3-12 CHOPPING TECHNIQUE IN A) FREQUENCY DOMAINS b) TIME DOMAIN. [27] ........... 34
FIGURE 3-13 STARTUP CIRCUIT ................................................................................................................ 35
FIGURE 3-14 DC UNIQUE OPERATING POINT ............................................................................................ 36
FIGURE 3-15 REPRESENTATIONS OF THE CONTINUATION METHOD APPLICATION. IN A) THERE IS REPRESENTED THE BGV CIRCUIT WITH THE LOOPS IDENTIFIED [31], AND IN B) THE RESULTS OF THE CONTINUATION METHOD [31]. ................................................................................................................ 37
FIGURE 3-16 FULL CIRCUIT OF THE PROPOSED BGV. ........................................................................... 39
FIGURE 4-1 CIRCUIT NETLIST OF A SIMPLE BGV 1ST ORDER CIRCUIT. .................................................................43
FIGURE 4-2 TESTBENCH NETLIST FOR A 1ST ORDER BGV CIRCUIT. .................................................................43
FIGURE 4-3 XML SETUP FILE FOR THE OPTIMIZATION OF THE 1ST ORDER BGV CIRCUIT. .............................44
FIGURE 4-4 AIDA-C GUI. ........................................................................................................................................45
FIGURE 4-5 SOLUTION BROWSER SETTING. ...........................................................................................................45
FIGURE 4-6 EXAMPLES OF POFS FOR DIFFERENT CIRCUITS, A) A FINAL “MIN. TC – MIN. VOFFSET” OPTIMIZATION FOR A 1ST ORDER BGV B) A FINAL “MAX. PSRR - MIN. IDD” OPTIMIZATION FOR AN OTA..........................46
FIGURE 4-7 GENERIC TESTBENCH FOR TESTING THE BGV CIRCUIT. ............................................................48
FIGURE 4-8 TC MEASUREMENT BY INTERVAL......................................................................................................49
FIGURE 4-9 OUTPUT BGV VOLTAGE WAVEFORM IN THE TYPICAL CONDITIONS..............................................51
FIGURE 4-10 OUTPUT BGV VOLTAGE WAVEFORM IN: A) ALL CORNERS B) UPPER CORNERS C) “MIDDLE” CORNERS D) “LOWER” CORNERS ........................................................................................................52
FIGURE 4-11 OUTPUT BGV VOLTAGE WAVEFORMS FOR MONTE CARLO SIMULATIONS. .............................53
FIGURE 4-12 STATISTICAL ANALYSIS OF MONTE CARLO SIMULATIONS RESULTS..............................................53
FIGURE 4-13 A) OUTPUT BGV VOLTAGE FOR THE UNIQUE DC OPERATING POINT SIMULATION OUTPUT B) VOLTAGE SOURCE AT STARTUP INPUT SWEEP IN CORNERS CONDITIONS. ..................................................................................54
FIGURE 4-14 OUTPUT BGV VOLTAGE FOR POWER DOWN SIMULATION IN CORNERS CONDITIONS. ..........55
FIGURE 4-15 CURRENT CONSUMPTIONS AT A FULL CIRCUIT), B) STARTUP CIRCUIT AND C) FIRST INVERTER IN STARTUP CIRCUIT IN CORNERS CONDITIONS. ..................................................................................56
FIGURE 4-16 CURRENT TRANSIENT WAVEFORMS, WHERE THE BLUE REPRESENTS THE STARTUP CIRCUIT CONSUMPTION, YELLOW THE BIAS VOLTAGE GENERATOR CONSUMPTION AND ORANGE THE TOTAL CURRENT CONSUMPTION IN POWER DOWN MODE. ................................................56
FIGURE 4-17 PSRR SIMULATION IN CORNERS CONDITIONS. .................................................................................57
FIGURE 4-18 NORMALIZED CURVES AT THEIR VOLTAGE AT 25°C. .......................................................................58
FIGURE 4-19 A) CURRENT THAT MAKE THE BGV VARIATIONS WITH TEMPERATURE, B) CLOSE UP OF SECOND ORDER COMPENSATION CURRENTS........................................................................59
FIGURE 4-20 BGV OUTPUT WITH IDEAL AMPLIFIER................................................................................................60
FIGURE 4-21 OUTPUT BGV WAVEFORM FOR A CIRCUIT WITH RESISTOR SPLIT IN BLOCKS .......................61
FIGURE A-1 BJT COLLECTOR VOLTAGE VARIATION THROUGH TEMPERATURE, FOR A CURRENT VARIATION OF 10m TO 20m........................................................................................................................................67
FIGURE A-2 ELT SPECTRE™ MODEL. .....................................................................................................................68
FIGURE A-3 CALCULATOR SHEET DETAIL........................................................................................................68
<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1</td>
<td>Performance synthesis of previous proposed BGV generator</td>
<td>13</td>
</tr>
<tr>
<td>2-2</td>
<td>BGV 2nd order generators performance</td>
<td>19</td>
</tr>
<tr>
<td>3-1</td>
<td>Estimated theoretical resistors values.</td>
<td>23</td>
</tr>
<tr>
<td>3-2</td>
<td>2 Stage OTA with Miller Compensation expected performance</td>
<td>24</td>
</tr>
<tr>
<td>3-3</td>
<td>RPP1 main information.</td>
<td>25</td>
</tr>
<tr>
<td>3-4</td>
<td>QP4 main specifications.</td>
<td>26</td>
</tr>
<tr>
<td>3-5</td>
<td>Resistor size estimations.</td>
<td>32</td>
</tr>
<tr>
<td>4-1</td>
<td>Typical and corner conditions</td>
<td>41</td>
</tr>
<tr>
<td>4-2</td>
<td>Dimensioning of the OTA circuit</td>
<td>47</td>
</tr>
<tr>
<td>4-3</td>
<td>OTA performance summary</td>
<td>48</td>
</tr>
<tr>
<td>4-4</td>
<td>Summary of the principal performance results of the BGV</td>
<td>51</td>
</tr>
<tr>
<td>4-5</td>
<td>Dimensioning of the BGV circuit</td>
<td>57</td>
</tr>
<tr>
<td>4-6</td>
<td>Dimensioning of the BGV resistors</td>
<td>58</td>
</tr>
<tr>
<td>4-7</td>
<td>Resistor total values and number of blocks</td>
<td>60</td>
</tr>
<tr>
<td>4-8</td>
<td>Results comparison between the previously proposed design and the design</td>
<td>62</td>
</tr>
<tr>
<td>A-1</td>
<td>Corners cases for 2nd order BGV circuit</td>
<td>71</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>AC</td>
<td>Alternate Current</td>
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</tr>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converters</td>
<td></td>
</tr>
<tr>
<td>BGV</td>
<td>Bandgap Voltage Reference</td>
<td></td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
<td></td>
</tr>
<tr>
<td>CTAT</td>
<td>Complementary To Absolute Temperature</td>
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</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converters</td>
<td></td>
</tr>
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<td>DC</td>
<td>Direct Current</td>
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</tr>
<tr>
<td>DOC</td>
<td>Dynamic Offset-Cancelation</td>
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</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random-Access Memory</td>
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<tr>
<td>ELT</td>
<td>Enclosed Layout Transistor</td>
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</tr>
<tr>
<td>GUI</td>
<td>Graphical User Interface</td>
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</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
<td></td>
</tr>
<tr>
<td>MIM</td>
<td>Metal Insulator Metal</td>
<td></td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-oxide-semiconductor (field-effect)</td>
<td></td>
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<tr>
<td>OPAMP</td>
<td>Operational Amplifier</td>
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<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
<td></td>
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<tr>
<td>PDK</td>
<td>Process Design Kit</td>
<td></td>
</tr>
<tr>
<td>POF</td>
<td>Pareto Optimal Front</td>
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<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td></td>
</tr>
<tr>
<td>PTAT</td>
<td>Proportional To Absolute Temperature</td>
<td></td>
</tr>
<tr>
<td>PVT</td>
<td>Process, Voltage and Temperature</td>
<td></td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
<td></td>
</tr>
<tr>
<td>TC</td>
<td>Temperature Coefficient</td>
<td></td>
</tr>
<tr>
<td>TID</td>
<td>Total Ionization Dose</td>
<td></td>
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<tr>
<td>TRAN</td>
<td>Transient</td>
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</tr>
</tbody>
</table>
INTRODUCTION

This chapter presents a brief introduction about the importance of voltage references in analog and digital IC with special emphasis in bandgap voltage references. First the motivation for this work is revealed, then a description of the objectives of this work and an outline of the thesis document.

1.1 Motivation

In analog and digital ICs, blocks like bias circuits, regulators and reference circuits exist purely to generate a DC voltage or current used in distinct application. A bias circuit generates the DC voltages required to keep transistors near some desired operating point – as transistor parameters change, either from chip to chip or with changes in temperature, so must the bias voltage. A regulator circuit improves the quality of a DC voltage of current, usually decreasing the noise. Finally, analog and digital ICs need a reference, being it a voltage, current or time, of a known fixed value. This reference should not fluctuate significantly under various operating conditions such as moving temperature or power supply and process variations as it establishes a stable point used by other circuits to generate predictable and repeatable results.

As an example, high precision ADC and DAC which are widely used in instrumentation and measurement systems require a high precision and steady voltage reference for the larger number of bits corresponds to a correct conversion [1]. DC-DC converters, AC-DC converters or linear regulators are other analog circuits also require reference voltages for their operation, while v’s and flash memories are digital devices that also need a reference. The circuits are other elements of higher systems like laptops or smartphones in which high precision voltage references are equivalent to an overall good performance as references play a pivotal role in the precision of the IC that composed the hardware. So, the accuracy requirements for integrated circuits are more stringent in today’s
marketplace where electronic companies try to be competitive by developing more precise hardware to increase the overall performance of the equipment.

Instituto de Telecomunicações at Instituto Superior Técnico proposed as Master Thesis the redesign of some blocks of an integrated circuit project with the objective to achieve better performance from the ones obtained before for a larger developing project in a space application. One of the blocks to be reworked is a BGV generator, a circuit that is specially designed to produce a voltage independent of temperature variations.

By having well characterized temperature dependent voltages and currents, one can sum these to produce an adjusted compensated response that can be categorized according to the result wave curvature degree. When only a well temperature characterize voltage is used without any attempt of compensation, it is said to be zero-order compensation, if a first-order term dependent of temperature is “canceled”, it is called first-order compensation and finally, if compensating second order or higher term, a curvature-corrected reference is achieved. It is a bandgap voltage reference with curvature correction that is desired to accomplish [2].

![Diagram](image_url)

Figure 1-1 Close-up of the BGV generator block in an ADC architecture.

### 1.2 Objectives

The goal of this work is to develop a radiation-hardened curvature compensated bandgap voltage reference which performance surpasses the previously obtained. The intention is that the project presented in this thesis be delivered for a possible implementation in a project. The following goals were set and were accomplish in order to achieve the proposed:
• **Analyze the state of the art to select the relevant topology:** study the key aspects behind the BGV circuits and analyze classic and some more advanced topologies, including ones with second order compensation and the study of second order compensation alone. Choose a design that can be adapted to the project scope;

• **Simulate and dimensioning the topology:** Dimensioned all the blocks necessary to create a BGV generator with the expected performance, simulating the circuit in typical and corners and realizing Monte Carlo simulations;

• **Deliver the design database:** Organize the database of the project respecting with project norms.

### 1.3 Document Structure

This document is organized as follows:

• Chapter 2 presents a study of the BGV generators family, starting with the basic concepts and traditional circuit, the previous approach and 2\textsuperscript{nd} order implementations;

• Chapter 3 presents the design of the full circuit developed in this work, including a description of all the blocks used;

• Chapter 4 presents the results and the respective observations;

• Chapter 5 concludes the work, with observations about the development of the project and the possible improvements to the work done.
This chapter gives an overview of the BGV generator, starting with the basic concepts. Then, the previous BGV approach is presented, the second-order types of improvements and finally a performance comparison between several topologies.

2.1 Basic Concepts

The most common ways to achieve a voltage reference are:

1) Using a Zener diode that breaks down at a known voltage;
2) Using the difference in the threshold voltage between an enhancement transistor and a depletion transistor;
3) Cancelling the negative temperature dependence of a PN junction with a positive temperature dependence from a PTAT circuit.

Unfortunately, 1) can not be used in IC because the breakdown voltage are bigger than the provided supply voltages and 2) is not an option because depletion transistors are normally not available and due to process sensitivity it is difficult to define the value of the reference [3], remaining the 3) as the most viable and widely used in IC. One of the first topologies was presented by Robert Widlar in 1971 [4] and successfully implemented by National Semiconductor’s voltage regulator LM113 [5].
The basis behind the concept BGV topologies, represented in Figure 2-1, is the mutual sum of two components, one PTAT and other CTAT, that produce a stable self-reliant from temperature fluctuations reference. To measure these fluctuations, the most important metric used is the temperature coefficient, TC, which measures variations of voltage across temperature, expressed as in equation (1).

\[
TC_{ref} = \frac{1}{\text{Reference}} \frac{\partial \text{Reference}}{\partial \text{Temperature}} \times 10^6 [\text{ppm/}^\circ \text{C}]
\]  

(1)

### 2.1.1 PN junction

The PN junction presents a well-known dependence with the temperature and is found in forward-biased diodes or in BJT. The base emitter voltage of a BJT versus temperature, can, in theory, be extrapolated to equal a known physical constant, which has the dimension Volt, at a temperature of 0 Kelvin. This constant is called the *extrapolated bandgap of silicon*, \(V_{BG} \approx 1.206 \text{ V} \), giving the name to this variety of voltage references.

The diagram in Figure 2-2 is the most universally used blueprint to produce a BGV generator and can be a representation of several different topologies. The BJT is employed due to its dependence of temperature, where PTAT voltage is achieve by amplifying the voltage difference between two forward-biased base-emitter junctions and the CTAT from a forward-biased, or in this case, a base-emitter junction.
In a more depth explanation, in a BJT the relation between collector current $I_C$ and the voltage of the forward-biases base-emitter junction, $V_{BE}$, is showed by equation (2), where $I_S$ is the transistor scale current, which has a strong dependence on temperature, $q$ the magnitude of the electrical charge on the electron, $k$ the Boltzmann’s constant and $T$ the temperature.

\[
I_C = I_S e^{\frac{qV_{BE}}{kT}} \quad (2)
\]

The base-emitter voltage can also be written as a function of collector current and temperature as shown by equation (3), where $I_C$ is the current density and the $I_{C0}$ is the current density at a given $T_0$ reference temperature, $m$ is a temperature constant and is equal to approximately 2.3, $V_{BE0}$ the base-emitter voltage at the reference temperature and $V_{g0}$ the extrapolated bandgap voltage of the junction at 0ºK which is approximately 1.206 V.

\[
V_{BE} = V_{g0} \left(1 - \frac{T}{T_0}\right) + V_{BE0} \frac{T}{T_0} + \frac{mKT}{q} \ln \left(\frac{T}{T_0}\right) + \frac{kT}{q} \ln \left(\frac{I_C}{I_{C0}}\right) \quad (3)
\]

For now, it is necessary to remember that the relation between junction current and junction current density is explicit by equation (4) where $A_E$ is the effective area of the base emitter junction.

\[
I_C = A_E I_C \quad (4)
\]

For $I_C$ constant, $V_{BE}$ will have approximately a $-2 \text{ mV}/K$. Found a CTAT, this is compensated by a PTAT to produce the desire reference, as an amplified difference of two base-emitter junctions biased at different current densities $J_2$ and $J_1$, and the difference in their junctions’ voltages is given by equation (5) where $V_T = \frac{kT}{q}$, which represents the thermal voltage at temperature $T$, and has a temperature drift of about $2.2 \text{ mV}/K$. 

Figure 2-2 Representation of a simple BGV circuit.
\[ \Delta V_{BE} = V_2 - V_1 = \frac{kT}{q} \ln \left( \frac{J_2}{J_1} \right) \]  

(5)

The difference between the base-emitter junctions holds accuracy even when collectors’ currents are temperature dependent, considering that the density current ratio stays fixed.

It will be seen shortly that when accomplishing a BGV generator, although the output voltage is, in theory, temperature independent, the junctions’ current turn out to be proportional to absolute temperature if the resistors used are temperature independent. By assuming that the resistors are temperature independent the relation in equation (6) is described, where \( J_i \) is the current density of the collector current of the \( i^{th} \) transistor and \( J_{i0} \) is the same current density at the reference temperature.

This approximation also simplifies further derivations.

\[ \frac{J_1}{J_{i0}} = \frac{T}{T_0} \]  

(6)

Now assuming that the difference between two base-emitter voltages is multiplied by a factor of \( K \) and added to the base-emitter voltage of the junction with the larger current density. Using equations (4), (5), and (6) it is obtained the relation between temperature and reference voltage, showed by equation (7) where \( V_{BE0-2} \) is the base-emitter junction voltage of the second BJT at temperature \( T_0 \).

\[ V_{ref} = V_{BE} + K \Delta V_{BE} = V_{G0} + \frac{T}{T_0} (V_{BE0-2} - V_{G0}) + V_{BE0} \frac{T}{T_0} + \frac{mkT}{q} \ln \left( \frac{T}{T_0} \right) + K \frac{kT}{q} \ln \left( \frac{J_c}{J_{C0}} \right) \]  

(7)

To have a zero temperature dependence at a particular temperature, the equation (7) is differentiate with respect to temperature as shown in equation (8).

\[ \frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0} (V_{BE0-2} - V_{G0}) + (m - 1) \frac{kT}{q} \ln \left( \frac{T}{T_0} \right) + K \frac{kT}{q} \ln \left( \frac{J_c}{J_{10}} \right) \]  

(8)

By making \( \frac{\partial V_{ref}}{\partial T} = 0 \) at the desired temperature at \( T = T_0 \), for zero temperature dependence at the reference temperature, the equation (9) emerges.

\[ V_{BE0-2} + K \frac{kT}{q} \ln \left( \frac{J_c}{J_{10}} \right) = V_{G0} + (m - 1) \frac{kT_0}{q} \]  

(9)

The left side of equation (9) is \( V_{ref} \) at \( T = T_0 \), leading to the result represented in equation (10).
\[ V_{\text{Ref}-T_0} = V_{o0} + (m - 1)V_{T_0} \approx 1.24V \] 

(10)

It is seen that the result is independent of the current densities chosen, so, if a large current density is chosen, \( K \) must be adjusted to achieve the desired voltage output.

For a temperature different from the reference temperature, the reference voltage is given by equation (11).

\[ V_{\text{Ref}} = V_{o0} + (m - 1)V_T \left(1 + \ln \frac{T_2}{T} \right) \]

(11)

### 2.1.2 BGV circuit examples

#### 2.1.2.1 Brokaw topology

The BGV circuit invented by Brokaw [6] is an example of a BGV topology that incorporates a two classical components presented in almost of topologies that follows this one: an OPAMP and BJT. In Figure 2-3 the circuit of Brokaw topology is presented.

![Brokaw BGV circuit](image)

**Figure 2-3 Brokaw BGV circuit [12].**

The principle of functioning of this circuit starts by forcing currents \( I_1 \) and \( I_2 \) to be equal, creating a stable and controllable \( V_{BE} \), by means of an OPAMP with a large gain configured to form an inverted feedback loop, which virtually short-circuits nodes at A and B and thus making \( V_A \) and \( V_B \) equal. By selecting the resistors \( R_A \) and \( R_B \) with the same value, the current flows through \( Q_1 \) and \( Q_2 \) will be clamped to be the same by the OPAM, and thus \( I_1 = I_2 = I \). As a result of this, the currents flowing
through \( R_1 \) and \( R_2 \) will be \( 2I \) and \( I \) respectively. The reference voltage is expressed by the equation (12).

\[
V_{\text{Ref}} = V_{BB_1} + 2IR_1 = V_{BB_1} + 2\frac{R_1}{R_2}\ln(N)V_T
\]  

(12)

### 2.1.2.2 Only CMOS topologies

Still, there are conventional topologies that do not rely on bipolar transistors and use the gate-source sources as the method of temperature compensation, where \( V_{GS} \) and \( \nabla V_{GS} \) works as CTAT and PTAT components respectively. This topologies suffer from the problem of only being able to reach values of BJT lower than the ones that can be obtained using BJT, due to the finite output resistance of the MOS transistors, only alleviated through channel length modulations. In figure there is an example of a BGV circuit that use only MOS transistors [7] [8].

![Figure 2-4 An all CMOS BGV topology [7].](image)

### 2.2 Previously Proposed BGV Approach

This approach is derived from one proposed by Karel E. Kujic [9] and the circuit schematic is presented in Figure 2-5.
In the following analyze, the resistors are not considered ideal because vary with temperature and the offset of the amplifier is taken into account. By applying the Kirschoff laws to the circuit, equations (13), (14) and (15) are obtained, using a notation where $A(T)$ represents a variable $A$ that depends of the temperature.

\[
V_{\text{Ref}} = I_{D1}R_1(T) + V_{D1} \quad (13)
\]

\[
V_{D1} = V_{D2} + I_{D2}R_3(T) - V_{OS}(T) \quad (14)
\]

\[
I_{D2} = \frac{V_{\text{Ref}} - V_{D1} - V_{OS}(T)}{R_3(T)} \quad (15)
\]

The current through collector of the diode connected BJT, $I_D$, is given by equation (16) and the voltages through diode connected BJT, $V_{D1}$ and $V_{D2}$, are given respectively by equations (17) and (18).

\[
I_D = I_s \left( e^{\frac{V_D}{aT}} - 1 \right) \quad (16)
\]

\[
V_{D1} = V_T \ln I_{D1} + V_{g0} - V_T(\ln(f_1A_1) + m \ln(T)) \quad (17)
\]

\[
V_{D2} = V_T \ln I_{D2} + V_{g0} - V_T(\ln(f_2A_2) + m \ln(T)) \quad (18)
\]

Figure 2-5 Previous proposed BGV circuit approach[10].
Joining equations from (14) to (18) results in equations (19) and (20), which represents the output voltage reference.

\[ V_{\text{Ref}} = I_{D_1}R_1(T) + V_T \ln(I_{D_1}) + V_{G0} - V_T (\ln(J_1A_1) + m \ln(T)) \]  

\[ I_{D_1}R_1(T) = \frac{R_2(T)}{R_1(T)} V_T \ln \left( \frac{I_{D_1}R_2(T)}{I_{D_1}R_1(T) - V_{OS}} \right) + \frac{R_2(T)}{R_3(T)} V_T \ln \left( \frac{A_2}{A_1} \right) + V_{OS}(T) \left( 1 + \frac{R_2(T)}{R_3(T)} \right) \]  

By linearizing the logarithmic elements in equation (20) and by supposing that the OPAMP produces a low offset, as shown in equation (21), and choosing a ratio \( \frac{A_2}{A_1} = 8 \) and \( R_1 = R_2 \), the reference voltage of the BGV generator is given by equation (22). This last equation shows that this topology is largely dependent on the \( \frac{R_2}{R_3} \) ratio and on \( V_{OS} \) \([10][11]\).

\[ V_{\text{Ref}} = V_{G0} + \frac{k}{q} \left( \frac{R_2(T)}{R_3(T)} V_T \ln 8 \right) + \ln \left( \frac{1}{R_3(T)} \right) + \frac{k}{q} (1 - m) + \left( 1 + \frac{R_2(T)}{R_3(T)} \right) V_{OS}(T) \]  

2.2.1 Results

The dependence of the \( \frac{R_2}{R_3} \) ratio and on the \( V_{OS} \), pointed before, means that variations on the value of both resistors or in the offset of the amplifier can lead to values of voltage reference that are not the expected. For example, it is highly probable that during fabrication resistors do not take the desired value of resistance. There were made improvements to the circuit in order to prevent that these aspects become flaws to the point that these jeopardize the quality of the system that is inserted. The schematic of the final version of the circuit is represented in Figure 2-6.

The improvements are two: a possibility of trimming the resistors after the fabrication and a Chopped amplifier with reduced offset, which will be discussed in Chapter 3.
The performance of the circuit after trimming calibration is summarized in Table 2-1, where the minimum and maximum values corresponds to the extremes values obtained during corners simulation. This results act as a reference to surpass for the results that will be obtained in the work developed in this thesis.

<table>
<thead>
<tr>
<th></th>
<th>Supply Current [mA]</th>
<th>PSRR [dB]</th>
<th>TC [ppm/°C]</th>
<th>$V_{Ref}$ [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum</td>
<td>1.9</td>
<td>-46.95</td>
<td>0.64</td>
<td>1.21</td>
</tr>
<tr>
<td>Typical</td>
<td>2.34</td>
<td>-56-54</td>
<td>7.75</td>
<td>1.235</td>
</tr>
<tr>
<td>Maximum</td>
<td>3.35</td>
<td>-73.28</td>
<td>10.46</td>
<td>1.26</td>
</tr>
</tbody>
</table>

### 2.3 Curvature Compensation

Nowadays typical first-order BGV are no longer adequate for many high performance systems, leading to higher order references implementation, also called curvature compensation. The most common type of compensation is the 2nd order correction, where in addition of cancelling first-order term there is also an attempt to approximately cancel the nonlinear second order terms of the BJT base-emitter voltage. Essentially, the 2nd order term in the Taylor series expansion of the diode relationship is canceled, leaving only third and so on order terms that represent variations with smaller amplitude. The Taylor series expansion of the diode relation, as a base-emitter junction voltage of BJT, is represented in equation (23).

$$V_{BE}(T) = V_{c0} - BT^2 + Cf(T)$$ (23)
First order references sum a positive linear temperature dependent voltage to a base-emitter voltage to cancel the effects associated to constant $B$, equation (23), while higher-orders try to cancel the effects associated to $C$. The goal of high-order bandgap references on other hand is to sum a temperature dependent voltage exhibiting both a positive linear and a positive nonlinear temperature dependence as seen in equation (24), where $V_\text{ref}$ is the voltage generated by the reference circuit.

$$V_\text{ref} = V_{BE}(T) + V_\delta(T) = V_{BE}(T) + DT^1 + EF_2(T)$$

(24)

In next sections there are different design approaches that will be exposed, ranging from second order compensations to exact cancellation techniques.

2.3.1 PTAT$^2$

The base idea of PTAT$^2$ technique is to offset the negative temperature dependence of the logarithmic term in $V_{BE}$ with a positive parabolic term, as represented in Figure 2-7.

![Figure 2-7 Graph representing the concepts of PTAT$^2$.](image)

The lower temperature range is predominantly controlled by the base-emitter voltage and by the linear PTAT component ($V_{BE} + V_{PTAT}$). As a result, the first half of the temperature range exhibits the curvature of a first order reference. This behavior is used to cancel the increasingly negative temperature dependence of the base-emitter voltage at higher temperatures.
Figure 2-8 Brokaw circuit presented in 2.1.2.1 with PTAT\textsuperscript{2} circuit implementation.

In this design presented in Figure 2-8, the loop composed of \( Q_1, Q_2 \) and \( R \) produces the PTAT current that flows through \( R_1 \) and \( R_2 \). Second order correction is finalized when the squared PTAT current is forced to flow through \( R_2 \). Consequently, the voltage reference is given by the equation (24). An implementation can be done with a PTAT current and a first order temperature stable current in a base-emitter loop, which produces a PTAT\textsuperscript{2} current.

2.3.2 Temperature Dependent Resistor Ratio

A nonlinear component can be generated by exploiting the temperature dependence of different resistors in a given process technology. Typically, circuit designers attempt to mitigate the effects of resistors’ TC, since they are considered parasitic, but the technique here illustrated takes advantage of these resistors to compensate the voltage reference high order components. This method has the advantage of having a small overhead because the implementations can be as simples as changing or adding an additional resistor, but it depends of the technology and the mismatch between the two types of resistance must be considered.

2.3.3 \( \beta \) Compensation

The exponential temperature dependence of the forward-current gain \( \beta \) of NPN transistors can be exploited to correct the nonlinear behavior of the diode voltage, \( \beta \propto e^{-\frac{T}{T_0}} \). Current gain \( \beta \) increases exponentially with rising temperatures, which is equivalent to saying that the BJT become stronger with ascending temperatures.
The circuit in Figure 2-9 generates a negative slope regarding temperature reference. Its translation to a circuit architecture with a positive output voltage is readily achieved by designing the complement of the structure shown or by modifying another first order BGV to adopt this technique. The resultant voltage reference is presented in equation (25) where A and B are temperature independent constants.

\[
V_{\text{Ref}} = -(AT + \frac{BT}{\beta})R - V_{BE}
\]

The current sources or current sinks fall under the PTAT category, then they can be represented with a linear first order relationship. This curvature-correcting scheme reaps the benefits of being simple and achieves good overall performance with low quiescent current. The lower limit of the power supply voltage is approximately 1.5 V, which derivates from the sum of the reference voltage and the voltage across the current sources – essentially a drain-source voltage drop.

2.3.4 Piecewise-Linear Current Mode Technique

For the case of the PTAT² technique, the nonlinear compensation component has a quadratic dependence to temperature. The nonlinear current though can be alternatively exponential or even piecewise-linear. The circuit in Figure 2-10 demonstrates how a nonlinear current \(I_{NL}\) is generated which is used as the curvature-correcting component of a high order BGV.
The circuit generates current $I_{NL}$ through a current mode operation. Its resulting dependence to temperature is piecewise-linear. The technique is based on the nodal subtraction of current and on the characteristic of non-ideal transistors. Transistor $M_1$ acts like a nonideal source of current that is proportional to a base-emitter voltage, equivalent to a first order CTAT dependence. For the lower half of the temperature range, PTAT current $I_{PTAT}$ is less than the supplied $V_{BE}$-dependent current if the device actually operates in the linear region supplying only $I_{PTAT}$; thus, $M_2$ does not conduct any current. For the upper half of the temperature range, $I_{PTAT}$ becomes larger than the theoretical value of $I_{VBE}$ forcing $M_2$ to source the difference. The result current through transistor $M_3$ is nonlinear—practically zero during the first half of the temperature range and nonlinearly increasing throughout the latter half. The relationship is described by equation (26) where $K_1$ and $K_2$ are constants defined by the ratios of the mirroring transistors defining $I_{PTAT}$ and $I_{VBE}$.

$$I_{NL} = \begin{cases} 0 & I_{VBE} \geq I_{PTAT} \\ K_1I_{PTAT} - K_2I_{VBE}I_{VBE} & < I_{PTAT} \end{cases}$$

From the practical design standpoint, the temperature range is partitioned in two: the range for which the nonlinear current is zero and the range for which the nonlinear current is nonzero.

The reference voltage at the lower half of the temperature range behaves essentially like a first order BGV since the nonlinear component is zero. At higher temperatures, the behavior is similar to that of the lower temperatures but the operation is not. The nonlinear dependence of $I_{NL}$ is designed to diminish the nonlinear effects of the base-emitter voltage. Consequently, the addictions of current $AI_{VBE}$, $BI_{PTAT}$ and $CI_{NL}$ at the upper temperature range generates a curvature-corrected trace whose behavior is depicted by $V_{Ref}$. It is assumed that in a final implementation all this currents are summed to flow through a resistor.
2.3.5 Matched Nonlinear Correction

This method tries to cancel the nonlinearity of the diode voltage instead of compensate. The correcting component does not exhibit the same dependence to temperature as the nonlinear term of the diode voltage relationship. This far, the correction terms explored have not had the logarithmic relationship required to completely cancel the third term of the diode voltage relationship represented in equation (3).

![Figure 2-11 Matched Nonlinear Correction proposed circuit.](image)

The goal of the circuit in Figure 2-11 is to generate voltage that has the logarithmic temperature dependence of the diode voltage $T \ln T$. Intuitively, if the ratio of the currents flowing through a couple of diode were to be PTAT, the $V_{BE}$ of the device is proportional to $T \ln T$. The transistors $Q_1$ and $Q_2$ example this conditions where $V_{AB}$ is the voltage difference between nodes A and B, $I_{PTAT}$ has a linearly positive TC defined by temperature-independent constant $K_1$ and $I_{CTAT}$ has a linearly negative TC defined by temperature constants $K_2$ and $K_3$ ($I_{CTAT} = K_2 - K_3 T$). As a result, the term within the logarithm has a positive concave relationship with respect to temperature.

The premise for this behavior is that $I_{CTAT}$ is greater than $I_{PTAT}$ throughout the temperature range and that the junction area of $Q_1$ and $Q_2$ must match well. Resulting term $V_{AB}$ through not exactly equal does exhibit a similar logarithmic dependence to the nonlinear term of the diode relationship. As a result, the addiction of voltage $V_{AB}$ converts the circuit into a curvature corrected BGV. Multiple $V_{AB}$ voltages may be summed to the output to optimize the nonlinear cancelation. This incremental summation would ease the burden of generating a large $V_{BE}$ voltage in a single $V_{AB}$ cell. Indecently, the temperature dependence of the term contained within the logarithm can also be manipulated to more closely resemble the logarithmic component of the diode voltage. This achieves an even better approximation of $T \ln T$ component. For instance, a $T \ln T$ is generated if the collector current of transistor $Q_1$ is to be constant. This characteristics is achieved by forcing the tail current of the $V_{BE}$ cell (presently $I_{CTAT}$) to sink $I_{PTAT} + I_{constant}$. 
A first order temperature independent current ($I_{\text{constant}}$) is designed by properly summing $I_{PTAT}$ and $I_{CTAT}$, where $K_4$ is independent of temperature. Constant $K_4$ is designed such that the total tail current is equal to the PTAT current following through transistor $Q_2$ in addition to a first order temperature independent current.

### 2.4 Circuit Comparisons

The Table 2-2 contains an overview of several BGV 2nd order performances and operate as a foundation to perceive the performance potential that a BGV circuit can achieve and what are the options of design to exceed the results obtained by the circuit.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Year</th>
<th>Technology</th>
<th>$V_{DD}$ [V]</th>
<th>$V_{Ref}$ [V]</th>
<th>$TC$ [ppm/°C]</th>
<th>PSRR [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>2012</td>
<td>CMOS 0.5 μm</td>
<td>2.3</td>
<td>0.6177</td>
<td>3.9(-15°C to 150°C)</td>
<td>-</td>
</tr>
<tr>
<td>[12]</td>
<td>2011</td>
<td>CMOS 0.18 μm</td>
<td>3.5</td>
<td>1.66 and 0.825</td>
<td>48.7(-10°C to 100°C)</td>
<td>-74</td>
</tr>
<tr>
<td>[13]</td>
<td>2005</td>
<td>CMOS 0.6 μm</td>
<td>1.8 to 5.5</td>
<td>1.15</td>
<td>3(-40°C to 125°C)</td>
<td>-</td>
</tr>
<tr>
<td>[14]</td>
<td>2011</td>
<td>CMOS 0.35 μm</td>
<td>-</td>
<td>3</td>
<td>2.1(-40°C to 125°C)</td>
<td>-</td>
</tr>
<tr>
<td>[15]</td>
<td>2013</td>
<td>CMOS 0.18 μm</td>
<td>2.5</td>
<td>0.820</td>
<td>16.62(-55°C to 125°C)</td>
<td>-96.56</td>
</tr>
<tr>
<td>[16]</td>
<td>2012</td>
<td>CMOS 0.35 μm</td>
<td>5</td>
<td>1.175</td>
<td>1.5(-40°C to 120°C)</td>
<td>-</td>
</tr>
<tr>
<td>[17]</td>
<td>2010</td>
<td>CMOS 0.18 μm</td>
<td>2.5 to 4.5</td>
<td>1.24</td>
<td>8.63(-25°C to 115°C)</td>
<td>-100</td>
</tr>
<tr>
<td>[18]</td>
<td>2007</td>
<td>CMOS 0.35 μm</td>
<td>1.4</td>
<td>0.858</td>
<td>12.4(-40°C to 125°C)</td>
<td>-69</td>
</tr>
<tr>
<td>[19]</td>
<td>2002</td>
<td>CMOS 0.18 μm</td>
<td>1.8</td>
<td>1.226</td>
<td>10(-25°C to 125°C)</td>
<td>-</td>
</tr>
<tr>
<td>[20]</td>
<td>2005</td>
<td>CMOS 0.8 μm</td>
<td>3</td>
<td>2.6</td>
<td>7(-20°C to 80°C)</td>
<td>-90</td>
</tr>
<tr>
<td>[21]</td>
<td>2012</td>
<td>BiCMOS 0.8 μm</td>
<td>1</td>
<td>0.54</td>
<td>4.65(0°C to 80°C)</td>
<td>-</td>
</tr>
</tbody>
</table>

### 2.5 Conclusions

The study in this chapter was used to better understand the operation of the BGV circuit, helping the future analysis and dimensioning of the selected circuit. Comparing the results in Table 2-2 with the performance to overcome that is exhibit in Table 2-1 it is possible to add value to the project by producing a BGV circuit with better performance.
This chapter contains the designs of all the sub-circuits that complete the BGV and an introduction to the most common error sources, nonlinearities and radiation effects. First, the base BGV circuit is presented including the 2\textsuperscript{nd} order compensation that is applied and then the bias generator and the amplifier that are adopted in the design. Then, the most common nonlinearities and error sources that can be considered in BGV generators and an ensemble of techniques planned to mitigate those negative effects will be explained. For last, the full circuit is presented and a conclusion is made.

3.1 Base Circuit

The proposed circuit topology chosen to be the base Bandgap circuit is an adaption from the one proposed by Banba, et al [21], and represented in Figure 3-1. Malcovati [22] proposed a second order compensation for the base circuit in which will also be used in the work developed in this thesis. What made this circuit the candidate chosen is the above average results that where obtained, seen in the last row in Table 2-2, which are with compliance with the objectives of being superior than the previously proposed circuit. It also allows the application of techniques that can improve the quality of the BGV and also permit that some procedures that need to be taken for the circuit to work normally in a high radiation environment.

3.1.1 Analysis

One of the concerns inherited by the technology was that the use of the BJT, an usual presence in BGV circuits, needed to be PNP type and a connection to the ground. This was an imposition by the technology since the PDK that was given did not permit another implementation. So the PNP BJT collector must be connected to the ground, turning into a diode.
Analyzing the circuit though the point of view of temperature dependence, the CTAT current is achieved when forcing the voltages $V_{inP}$ and $V_{inN}$ to be equal due to the amplifier virtual short circuit, producing a current, flowing in the same value resistors $R_1$ and $R_2$, proportional to $V_{BE}$, making the equality in equation (27). From the current that passes through the both PNP transistors and by the resistor $R_0$, which is equal to $V_T \ln N$, a PTAT current is obtained, where $N$ is the relation between the emitter area of transistor $Q_1$ regarding transistor $Q_2$. As normally used in BGV circuits with BJT with different area ratios, $N = 8$.

$$I_1 = I_2 = I_3$$  \hspace{1cm} (27)

The current that occur in the PMOS mirror is, as seen in equation (28), the sum of both PTAT and CTAT current.

$$I_1 = \frac{V_T \ln N}{R_0} + \frac{V_{BE}}{R_1}$$ \hspace{1cm} (28)

This current passes through $R_3$, producing the reference voltage given by equation (29).
\[ V_{BG} = I_3 R_3 = R_3 \left( \frac{V_T \ln N}{R_0} + \frac{V_{BE}}{R_1} + V_{OS} \right) \] (29)

The current will be at least 20\( \mu \) - fact that will be explained later - the \( V_{BE} = 650mV \), \( V_T \approx 0.026 \), the offset voltage \( V_{OS} = 0 \), \( \ln N = 8 \) and \( V_{BG} = 1.25 \) and considering an \( R_0 = 5k\Omega \), we will have the resistor values presented in, which are calculated with the help of equations (28) and (29).

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Value [( \Omega )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_0 )</td>
<td>5k</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>70k</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>70k</td>
</tr>
<tr>
<td>( R_3 )</td>
<td>62.5k</td>
</tr>
</tbody>
</table>

### 3.1.1.1 Base Circuit Blocks

#### 3.1.1.1.1 Current Mirror

The current mirror is essentially a replicator of current. In this case, it is composed by MOS transistors \( M_1 \), \( M_2 \) and \( M_3 \) and is used to replicate the current to the resistor \( R_3 \) where it is transformed into the voltage reference. The mirror will be constructed with PMOS transistors that must work in saturation region so that their drain-to-source voltage can be small when the drain-to-source currents are reduced.

It is desired and extremely important for the precision of the BGV that the replications follows a scale of 1:1, so transistor \( M_1 \), \( M_2 \) and \( M_3 \) must have equal size and that be divided into smaller transistors as a layout technique that helps to preserve the matching between them.

#### 3.1.1.1.2 OPAMP: OTA

The amplifier in the design is what makes the BJT emitter currents \( I_1 \) and \( I_2 \). It was chosen a 2 Stage OTA with Miller Compensation, as shown in [23] because the as its high impedance at the input makes this amplifier topology adequate for the feedback, and because its of considerable easy implementation in a first phase of the circuit. The added 2\(^{nd} \) stage allows a higher gain and possibilities a lower voltage offset, which are the main figures-of-merit that need attention when designing this amplifier.

The Miller Compensations ensures stability in a feedback configuration and is obtained by adding a capacitor between the first and the second stage, which inserts a zero in the feedback system.

The disadvantage of this circuit is that there is difficult to achieve relatively high bandwidth. Fortunately, in the case of the BGV, there are no AC signals flowing so the bandwidth specification can be left aside.
Figure 3-2 OTA circuit schematic.

The Table 3-2 contains the intended results for the 2 Stage OTA with Miller Compensation. Because the inputs of the amplifier will be connected to the collectors of the BJT, and these have a variation in the temperature range where the circuit will work of 400mV to 850mV (in Annex A.1), the expected performance is also applied to the corner case, where the common mode voltage range is considered. The layout the input transistor $M_1$ and $M_2$ is critical, because the better their matching, lesser the offset voltage.

![OTA circuit schematic](image)

<table>
<thead>
<tr>
<th>Measure</th>
<th>Expected</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD} [\mu A]$</td>
<td>&lt;= 300</td>
</tr>
<tr>
<td>GDC ($dB$)</td>
<td>&gt;= 70</td>
</tr>
<tr>
<td>PSRR ($dB$)</td>
<td>&gt;= 60</td>
</tr>
<tr>
<td>GBW ($MHz$)</td>
<td>&gt;= 0.1</td>
</tr>
<tr>
<td>PM [$^\circ$]</td>
<td>60 to 90</td>
</tr>
<tr>
<td>VOFF [$mV$]</td>
<td>&lt;= 0.01</td>
</tr>
<tr>
<td>NO [$mV$]</td>
<td>&lt;= 0.15</td>
</tr>
<tr>
<td>SN [$mV/\sqrt{Hz}$]</td>
<td>&lt;= 0.15</td>
</tr>
<tr>
<td>SR [$MV/s$]</td>
<td>&gt;= 0.5</td>
</tr>
<tr>
<td>AREA [$\mu^2$]</td>
<td>&lt;= 15000</td>
</tr>
</tbody>
</table>

### 3.1.1.1 Bias Generator

The objective of the bias circuit is to generate the current of $20\mu A$ that will be used by the OTA and the voltage bias for the cascode stage in the mirror. There is a given $80\mu A$ that is scaled down to $20\mu A$ by using a MOS current mirror with a ratio of 1:4. For that, the $M_{B2}$ transistor $\frac{W}{L}$ ratio must be four times bigger than the $M_{B1}$ transistor $\frac{W}{L}$ ratio. For a better matching between the transistors, it was decided
that the L is fixed and that the multiplicity of the $M_{B2}$ transistor will be 4 times smaller than the W of the $M_{B1}$ transistor.

The 20$\mu$A will be generated from the mirroring by the $M_{B3}$ and $M_{B4}$ transistors, where their dimensions will be equal to correctly replicate the current in the $M_{B3}$ drain.

![Bias generator circuit](image)

**Figure 3-3 Bias generator circuit.**

This block will also provide a bias voltage used in the cascode stage, which is presented in sections 3.4.1. This voltage will be applied to the cascode MOS transistors gate to polarize them in order to work in the saturation region. This bias voltage is generated using a PMOS transistor, $M_{BV}$, which will work in the triode region in order to tune the bias desired bias voltage.

### 3.1.2.2 Components

#### 3.1.2.2.1 Resistor

All the resistors that are part of the design are of the type rpp1 and are available in the XFAB XH035 PDK. The resistors are made of polysilicon material and the main specifications can be found in Table 3-3. An approximation of the resistor area is calculated by the equation (30), where $L$ represents the length, $W$ the width and $m$ the number of blocks that the resistor is composed.

<table>
<thead>
<tr>
<th>Resistor Type</th>
<th>Name</th>
<th>$R_s[\Omega/\square]$</th>
<th>$TC[10^{-3}/^\circ\text{C}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DP}[\mu A]$</td>
<td>rpp1</td>
<td>320</td>
<td>-0.18</td>
</tr>
</tbody>
</table>
\[ \text{Area}_{\text{Res}} \approx LWm \] 

3.1.1.2.2 BJT

The BJT that are part of the design are of the type qp4 are available in the XFAB XH035 PDK. The BJT main specifications can be found in Table 3-4. An approximation of the BJT area is calculated by the equation (31), where \( n \) represents the multiplier of the transistor emitter area.

\[ \text{Area}_{\text{BJT}} \approx n \text{Area}_{\text{emitter}} \] (31)

Table 3-4 qp4 main specifications.

<table>
<thead>
<tr>
<th>BJT Type</th>
<th>Name</th>
<th>Emitter Area [( \mu m^2 )]</th>
<th>( V_{BE} [mV] )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertical PNP</td>
<td>qp4</td>
<td>100</td>
<td>745</td>
</tr>
</tbody>
</table>

3.1.1.2.1 Capacitors

The capacitors that are present in the design are of the type cdmm MIM capacitors, are available in the XFAB XH035 PDK. An approximation of the capacitor area is calculated by the equation (32), where \( A_{\text{capacitor}} \) represents the area of a single capacitor block and \( m \) represents the number of capacitor blocks.

\[ \text{Area}_{\text{Cap}} \approx n \text{Area}_{\text{emitter}} \] (32)

3.2 2nd Order Circuit

The 2nd order circuit proposed is a simple solution compared with others that use amplifiers, switched capacitors or try literally to correct the higher order terms. By following the analysis in section 3.1.1,
the circuit of the Figure 3-1 only corrects the first order of the diode equation (3). In Figure 3-4 is presented a circuit that can compensate the second order components in the BGV reference voltage and was proposed by [21], inspired in the solution introduced in [24].

This correction is of the type introduced in section 2.3.3, where the difference is that both already created CTAT and PTAT current are sampled and passed through a new BJT. The objective is to correct the non-linear term by subtracting the \( V_{BE} \) obtained from a junction with the constant current and the \( V_{BE} \) obtained from a junction with a PTAT current. As already concluded by inspecting of the circuit in Figure 3-1 it is observed that the current in \( Q_3 \) is PTAT while the current in \( M_2 \) is almost temperature independent. Therefore, if we mirror the current flowing in \( M_1 \) and we inject it into a diode connected bipolar transistor \( Q_3 \), we generate the \( V_{BE} \) with constant current. Resistors \( R_{2onN} \) and \( R_{2onP} \) will drain an additional current from \( M_1 \) and \( M_2 \), proportional to the above mentioned \( V_{BE} \) difference to balance the output curve.

### 3.3 Radiation Hardness

The project where the bandgap circuit will be integrated will have a particular attention on the BGV radiation-hardness, due to the fact that the project is to be used in an aerospace application.

One of the principles to be followed regarding methods to prevent that the radiation has a great impact in the functioning of the circuit to the point that it malfunction is considered, every branch has to be at least a current with at least 10\( \mu A \).

Deep sub-micron technology is inherently highly tolerant to radiation, mainly due to the reduce oxide thickness. However, the isolation field oxide around MOS devices are not so thick, being the dominant source of TID effects[25]. In this field oxide a pair of parasitic channels can be formed due to TID effects. To eliminate these parasitic channels, the ELT transistor was developed.

#### 3.3.1 ELT

The ELT is a different kind of transistor as a result its different geometry, shown in Figure 3-5. The gate is completely surrounded by the source of the transistor, avoiding any parasitic channels. The removal of the parasitic channels eliminates the threshold shift caused by a ionizing radiation in field oxide.
To reduce the risk of radiation triggered single event latch-up, it is also common practice to use low-
ohmic guard rings around every p-well and n-well. The ELT with guard rings in deep sub-micron
CMOS technology proved to be an extremely tolerant to radiation CMOS device [26].

The big difference in the use of this transistor is that during the dimensioning of the transistors, instead
of having width and the length of the gate as variables, we will have the $dx$, which represents the x
side, $dy$, which represents the y side, and the length, $L$, as the variables that will define the transistor
behavior. In a way, the x and y variables are the equivalent of the W of the normal transistor. The
equation (33) describes the connection between the effective $W$ that is normally dimensioned to the $dx$
and $dy$.

$$W_{\text{effective}} = 3.3055L + 2(dx + dy) - 0.4614\mu$$

(33)

For sake of lessening the burden of having three variables to dimensions, it is considerate that $dy$ is
fixed the minimum size, which is $1\mu$.

One of the problems that appear in the dimensioning of a circuit using ELT is the dependence of the
$W$ with the $L$, which limits the values of $W_{\text{effective}}$ when larger $L$ are used. For example, when using a
$L = 1.05\mu m$ and picking the minimum $dx = 1\mu m$, the $W_{\text{effective}}$ will be automatically bigger than $7\mu m$. If
it is needed a large $L$ that will produce a minimum $W_{\text{effective}}$ which is not compatible with the design
requirements, then there is a possibility to use the equation (34) to found the $dx$ that gives the desired
$W_{\text{effective}}$ when are put $n$ transistors in series, with $L' = \frac{L}{n}$.

$$dx' = \frac{1}{2}L \left(3.3055 \left(1 - \frac{1}{n}\right)\right) + dx$$

(34)
To prepare the circuit for an effective layout, there are three tips that can be executed. First, and after analyzing the layout of this transistor, it was seen that the minimum size of the vias between metal and the doped substrate that can correspond to the source or to the drain is $1\mu \times 1\mu$. It was decided that for a better conductivity and to prevent fabrication defects, these vias should have at least 2 contacts, so the minimum size for $dx$ will be $2\mu$. Second, the purpose of these transistors is to look like the normal ones – like a rectangle. So when possible, the $L$ chosen must be smaller comparing to the $dx$, as shown in Figure 3-6 where are represented a good and a bad layout. Third, it is normal activity of dividing the $W_{effective}$ into several transistors with $\frac{w}{m}$, where is the number of transistors to provide a better matching, immunity to process variations or prevention to metal strips breaking. In the case of ELT, the division is not that trivial. So, for a new $m'$, for the same $W_{effective}$, the new $dx'$ is calculated by the equation (35).

$$dx' = \frac{1}{2}L\left(\frac{m}{m'}3.3055 - 3.3055\right) + \frac{m}{2m'}(2dx + 1.5386) - 0.7693 \tag{35}$$

The area of this transistor is using the equation (36), which treats the transistor as a rectangle where the sides are the $y$ side and the $x$ side from the Figure 3-5.

$$Area = (1.7\mu + 2L + x)(2.7\mu + 2L) = 2.7x\mu + 4.59\mu^2 + L(4L + 2x + 8.8\mu) \tag{36}$$

There is another ELT, which will not be used, that has a dimensioning more similar to the typical dimensioning, which permits smaller $dx$ for a certain $L$ but is less resistant to the radiation. The equation X describes the calculation of the $W_{effective}$.

$$Area = (1.7\mu + 2L + x)(2.7\mu + 2L) = 2.7x\mu + 4.59\mu^2 + L(4L + 2x + 8.8\mu) \tag{37}$$

These transistors are included in the PDK used. The netlist correspondent to the ELT is presented in the annex, where the model is presented. Two transistors compose it, one in a normal combination and the other that models the gate section that does not belong to the ring and it is considered a parasite, where the drain is connected to the source.
3.4 Error Sources and Nonidealities

When studying the circuit, some effects are difficult to model and can provoke changes not expected, affecting largely the circuit performance. These problems were identified solutions for each one of them will be presented next. The

- **Source fluctuations and noise:** where the solution is to implement a cascode stage in current mirror, in section 3.4.1 and an output filter, in section 3.4.2, to frequency cut the noise.
- **Resistors non idealities:** where the solution is the implement an after fabrication trimming resistor, in section 3.4.3.
- **Offset voltage:** where the solution is to implement a Chopper amplifier, in section 3.4.4.

3.4.1 Cascode Mirror

Being this circuit included in a SoC is composed of analog and digital circuits, including sometimes even radiofrequency circuits, all in the same package. High frequency noise generated by digital circuits couples onto analog supply lines and steady-state DC voltage changes implies a decrease in the performance of the BGV circuit. The implementation of cascode stages generally improves the behavior of the circuit regarding those rejections of noise and variations from the source by increasing the output impedance of certain circuit.
The concept may be described by assuming an impedance divider from the power supply to ground and whose common-middle node is the voltage reference. Considering the equation (38), the PSRR will improve as the impedance of the reference voltage to the input supply increases.

\[
PSRR = \frac{z_{\text{gnd}} + z_{\text{in}}}{z_{\text{gnd}}}
\]  

(38)

In this work the cascode stage will be implement in the current mirror, and will be of the kind presented in Figure 3-7.

If talking about a normal configuration where \( M_2 \) transistor is not present, then only the channel-length modulation effect of transistor \( M_1 \) would define the output resistance. By implementing a cascode stage with transistor \( M_2 \) in series it is expected an increase in the output resistance, as shown by equation (39). The \( R_{SD1} \) and \( R_{SD2} \) are the output resistances of transistors \( M_1 \) and \( M_2 \) while \( g_m_2 \) is the transconductance of transistor \( M_2 \). If comparing the circuit with and without cascode configuration, gains of the output resistance could achieve 30 to 50dB.

\[
R_{out} \approx (1 + g_m_2 R_{SD1})R_{SD2} + R_{SD1} \approx g_m_2 R_{SD1}R_{SD2}
\]  

(39)
Figure 3-8 shows the implementation of the cascode transistors $M_{\text{cas1}}$, $M_{\text{cas2}}$ and $M_{\text{cas3}}$ in the mirror. The node “gate_cas” represents the bias voltage produced by the bias generator.

### 3.4.2 Output Filter

![Figure 3-9 Output filter circuit.](image)

The output low pass filter is made of a $R_{\text{out}} = 5k\Omega$ resistor and a decoupling capacitor $C_{\text{out}} = 100nF$, making the cut frequency of the filter around the $300Hz$. The filter is implemented outside of the circuit and the purpose is to eliminate internal noise.

### 3.4.3 Resistors Trimming

#### 3.4.3.1 Resistors Non idealities

In the Table 3-5 there are displayed the physical size values for the 1st order resistors’ estimations. Although relevant, these estimations repercussions must be treated with caution because the theoretical analysis of the circuit that was performed does not take into consideration the resistance variation with the temperature, which will deviate the output considerably from the theoretical prediction.

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Value [Ω]</th>
<th>$\text{Length [μm]}$</th>
<th>$\text{Width = 2μm}$</th>
<th>$\text{Width = 8μm}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_0$</td>
<td>5k</td>
<td>17.7</td>
<td>77.7</td>
<td></td>
</tr>
<tr>
<td>$R_1$</td>
<td>70k</td>
<td>277.7</td>
<td>1127.7</td>
<td></td>
</tr>
<tr>
<td>$R_2$</td>
<td>70k</td>
<td>277.7</td>
<td>1127.7</td>
<td></td>
</tr>
<tr>
<td>$R_3$</td>
<td>62.5k</td>
<td>247.7</td>
<td>997.7</td>
<td></td>
</tr>
</tbody>
</table>

Another issue that arises with the use of resistors are that their value can deviate from the wished due to process variations and mismatch, which can be prevented by elaborating a proper dimensioning with the layout in mind. There is the possibility to trim resistors after fabrications with the purpose to adjust the resistor value.

#### 3.4.3.2 Trimming

The trimming implies that some additional structures need to be developed by the circuit designer. The resistor needs to have a mechanism where a number of bits can control the resistor value. In Figure 3-10, there is a circuit proposal for the trimming section, where is retired a $\Delta R$ to the resistor value, that
corresponds to the value expected for the resistor to fluctuate, and \( k \) is the number of bits available. Then, an assembly of smaller resistor blocks is placed in series, with a switch bit controlled in shunt with each resistor block. The smaller resistor blocks values will dependent of the number of bits available to perform the trimming, being the trimming more accurate as more the number of bits available.

As an example, during the Monte Carlo simulations, the resistor value varies ±10\%, and for previous proposed design, the available number of bits \( k = 10 \).

Figure 3-10 Trimming Resistor.

There were chosen two possible spots to apply the resistor trimming. One is in \( R_1 \), because the matching between this resistor and \( R_2 \) influences severely the BGV, being an attempt to improve the TC.

Figure 3-11 Amplifier with adjustable gain

The other is at the output, where an amplifier assembly like the one in Figure 3-11 can be used to control the output voltage DC value, by fixing the gain represent by equation (40) when trimming \( R_B \).

\[
A_V = \frac{R_B}{R_B + R_A}
\]  

(40)
3.4.4 Chopper Amplifier

The amplifier is in a lot of topologies an essential part of the functioning of the BGV, but also could be a source of error in the reference voltage when the offset is considerable or by introducing of flicker noise. The offset is an error at the output of the voltage that could appear due mismatch of transistors or resistors during the process variations and the flicker noise can appear when the amplifier is designed with MOS transistors. These can be reduced enough by using large devices and good layout techniques, and by using special amplifiers with chopping techniques. The chopping technique, represented in Figure 3-12, is included in the DOC family techniques and by modulating a signal, amplifying it and then demodulating it is possible to reduce considerable the offset.

Supposing that the input signal has a spectrum limited to half of the chopper frequency, no signal aliasing occurs and the amplifier is ideal, with no noise of offset. The input signal is multiplied by the square-wave carries signal with period \( T = \frac{1}{f_{\text{chop}}} \). After this, the signal is transposed to the odd harmonics frequencies of the modulation signal. It is then amplified and demodulated back to the original band. What happens, assuming that the signal at the input of the chopper amplifier is a DC signal \( V_{\text{in}} \), is that the signal output at the first modulator is a square wave of period \( T_{\text{chop}} \) and amplitude \( V_{\text{in}} \).

![Figure 3-12 Chopping technique in a) Frequency Domains b) Time Domain. [27]](image)

For an amplifier with limited bandwidth and gain \( A_0 \), the signal at the output of the amplifier is a square wave with an amplitude of \( A_0 V_{\text{in}} \) containing the DC offset voltage. The output of the second is then the rectified wave containing even-order harmonic frequency components. These have to be low filtered to recover the amplified signal. Since the noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave and the signal at the output of the filter has no offset and almost none low frequency noise.

Some of the disadvantages of using this kind of technique on amplifiers are the obvious complex added to the circuit design, the reduced bandwidth, the possibility of aliasing and intermodulation and
the phase that can be introduced. The modulators can be realized by polarity-reversing MOS switches [27].

3.5 Stability

The non-linear current-voltage relationship of a diode connected BJT and a N times larger diode connected BJT with a resistor in series, used in the BGV proposed, has two crossing points that represents the two stable points. One of those points is when there is no current in the circuit, having no interest for the functioning of the circuit, the other being the one that where the circuit is desired to work. To ensure that the circuit stabilizes at the desire current and voltage values, a startup circuit was implemented.

3.5.1 Startup Circuit

The circuit that is represented in Figure 3-13 is the one implemented in the BGV developed. The current of the BGV circuit is mirrored into $M_{S2}$, thus, in case of the circuit stabilizes in the no current state, the voltage at $R_{S2}$ is at a low level. This will cause the output of the inverter $I_2$ to pull the gate to ground, making a short-circuit of the node at the exit of the amplifier to ground. This will start the mirror to flow some current, translating the stable point to the one with no current to the desired. As the current start to flow, the resistor $R_{S2}$ transforms the current into voltage, shutting the startup circuit.

![Figure 3-13 Startup Circuit.](image)

This method of startups has no influence in the voltage reference and in the currents where the dependence of the temperature must be inalterable, as there is no injection of current in the main branches.
3.5.2 Testing the Stability

Typically the stability can be tested by expecting that during the simulations, the circuit converge to the desiring working point. In DC, the simulation that pushes more the circuit to work in extraordinary conditions are the Monte Carlo simulations. A good indicator of the quality of the startup is if the all Monte Carlo simulations converge. In transient, it is always expected that when turning on, the circuit achieves the correct functioning point.

There is other test to test the DC Unique Operating Point that can be done, which consists in opening the startup control loop and entering a sweeping voltage source, as shown in Figure 3-14, which will make first turn on the startup mechanism and then turn it off. If the circuit maintains the state, it shows that it can be stable after disconnecting the startup.

A state-of-the-art method that allows to test the stability and to find the convergence DC points of the circuit is presented next.

![Figure 3-14 DC Unique Operating Point.](image)

3.5.2.1 Continuation method

The continuation method is a practical method to verify the effectiveness of a startup circuit. Instead of a transient simulations, which does not show that the startup removes the undesired stable point and it does not guarantee that after fabrications the circuit behaves correctly. This method involves the introduction of a current or voltage source that is swept to trace operating points of a circuit. This source is introduced in the a feedback loop identified in the circuit, breaking and allowing the identification of the stable points of the circuit. The most difficult part of this method is the identification of the feedback loop, which is described in [28][29].
Figure 3-15 Representations of the Continuation Method application. In a) there is represented the BGV circuit with the loops identified [31], and in b) the results of the Continuation Method [31].

[30] and [31] provide examples of practical applications of this method, being one of them a BGV generator almost identical to the one developed in this thesis. The Figure 3-15 a) shows the identified loop in the first order BGV, where node $N_1$ and $N_3$ form the so-called positive loop and $N_5$ and $N_2$ the negative loop.

In Figure 3-15 b) there are presented the results from the simulation when putting a DC voltage source in between the each one of the loops and sweeping that DC voltage source. When the output voltage crosses, $V_T$ crosses the $V_T = V_a$ line, it means that the circuit has found a stable point and the output can stabilize at that point. Analyzing the figure we see that exists 3 stable points for that BGV circuit, which does not have a startup circuit applied.

### 3.6 Power Down Mode

One usual implementation in analog IC an implementation of a power down mode, where it the circuit consumption is approximately null. This process prevents current consumptions when the circuit state is in disabled mode.

Following the project guide, the power down system is controlled by a binary signal, where high means that the circuit is enabled and it has the normal functioning. The signal is connected to circuit composed of transistor that work as interrupters and shut down MOS transistors in order to isolate the circuit from the power source. The shut down is done by connecting nodes of the circuit to the ground or $V_{dd}$, nodes that are normally gates, sources or drains of MOS, in order to close the current flow.
3.7 Conclusion

A full representation of the circuit that is proposed in this section can be found in Figure 3-16. This circuit has several upgrades regarding the one previously proposed, namely the cascode stage, trimming section and 2\textsuperscript{nd} order compensation, which will allow overcoming the previous results.

In next chapter, the dimensioning and the results obtained are presented.
Figure 3.16 Full circuit of the proposed BGV.
This chapter describes and discusses the results obtained with the proposal circuit introduced in Chapter 3. First, the role of tools utilized in the development is specified, with special focus in AIDA-C optimization tool. Then the OTA results are exposed followed by a detailed 2nd order circuit results presentation, including a deep and graphical characterization of all the key aspects of the circuit and by experiments like resistor block divisions and the substitution of the OTA by an ideal amplifier which contributes to the analysis of the circuit dimensioned. For last, a conclusion is made about the results obtained.

The starting point of the work was to dimension the OTA circuit, which worked as the entrance point to the project tools and how an analog IC project work flows. Then, a first order bandgap was dimensioned, followed by the addiction of the cascode stage, its voltage and current bias generator, the startup circuit and finally the 2nd order stage. This dimensioning process was not linear as the previous ordering may sound, but took several iterations and adjusts when new blocks were being added.

All of the circuits are tested in corners cases and with Monte Carlo simulations. The Mentor Graphics Eldo© is the simulator chosen to evaluate the circuit, which includes the graphical waveform environment EZwave™. The versions used for Eldo© and EZwave™ are the 13.1.

<table>
<thead>
<tr>
<th>Table 4-1 Typical and Corner conditions.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistors</td>
</tr>
<tr>
<td>Min.</td>
</tr>
<tr>
<td>Typ.</td>
</tr>
<tr>
<td>Max.</td>
</tr>
</tbody>
</table>

*worst power
worst speed
worst one
worst zero
The corners values are identified in Table 4-1, including the usual PVT evaluation plus current minimum and maximum values applied, which does not represent all values for current as different values are used for each corner case.

4.1 Tools

During the design of an analog IC, there is a collection of tools that help the designer to achieve the final objective. Especially for this work, there were two tools that played a major role in the development of BGV, which were the Cadence® Virtuoso - Schematic Editor + Simulation Environment and specially the AIDA-C, an optimization tool. The Cadence® version used was the IC6.1 and the AIDA-C was the 2.1.3957, as a tester.

4.1.1 Cadence

Cadence® tools were essentially used to draw the circuits, using the Schematic Editor. The simulator environment of Cadence® was used in parallel with Eldo© especially for sweeping simulations that were easier to set up in Cadence®. The weak point in Cadence® ambient was that it was not set up neither for Corners or Monte Carlo statistical simulations.

4.1.2 AIDA C

AIDA-C is an optimization tool that targets the sizing of the devices in analog circuits. It is based in multi-objective multi-constraint optimization techniques and addresses robust design requirements by taking into account worst cases corners. The utilization of the tool follows some user steps, which will be explained sequentially with examples from a 1st order BGV and OTA circuit in following subsections.

4.1.2.1 Setup

The first step when using the AIDA-C the tool which consists in create a netlist of the circuit, design the netlist of the testbench and define the XML setup file. The netlist of the circuit can be easily obtained by exporting the created netlist from the circuit drawn in the Cadence® Schematic Editor. These circuit netlist needs to be properly parameterized, usually applied to the sizes of the components. In Figure 4-1 there is the circuit netlist for the 1st order BGV.
The netlist of the testbench creation is not so trivial, because it must be written using the simulator language and although it can be extracted from Cadence® Virtuoso®, it can’t include every measure and extraction from the circuit performance and characteristics due to software limitations. Those measures that are needed for the AIDA-C to run are obtained using Eldo®'s .measure/extract commands. To generate corners evaluations a file containing the alternative simulations corresponding to each corner is also needed, using the Eldo®.alter command. The Figure 4-2 contains the netlist for the testbench used for the circuit in Figure 4-1.

**Figure 4-1 Circuit netlist of a simple BGV 1st order circuit.**

The XML file setup will contain the parameter values used in the optimization and their ranges, the design constraints, like overdrives and saturation margins of the transistors or desired minimums for certain circuit performance, and finally the optimizations objectives. The Figure 4-3 holds an example with a setup configuration for DC and AC, including corners cases.

**Figure 4-2 Testbench netlist for a 1st order BGV circuit.**
Figure 4-3 XML setup file for the optimization of the 1st order BGV circuit.

4.1.2.1 AIDA-C GUI

In the GUI, partially presented in Figure 4-4, it is possible to manage the previous designs and optimizations runs, by loading or saving, and set and update the specifications after defining the XML setup file.
Although not mandatory, it is possible to start the simulator using an initial solution, by adding the set of parameters variables in the solution browser setting. In this area it is possible to perform sweeping simulations, which adds to AIDA-C more versatility by becoming a tool that can also perform not-automatic dimensioning and performance verification after an optimization, everything in the same background.

Figure 4-5 Solution Browser Setting.

4.1.2.1 Outputs

The evolutions of the solutions, feasible or not, are found in a graph mapped regarding the objectives selected and can be seen during and at the end of the optimization. When the solutions fulfill all the constraints, they are listed in Figure 4-4 c) and graphically represented in a Pareto Optimal Front.
where the feasible tradeoffs between the different optimizations objectives are presented. In Figure 4-6 there is an example of a POF for a 1st order BGV circuit optimization and an example of a POF for the OTA optimization.

4.2 OTA

Besides an essential element in the BGV circuit, the design and dimensioning of the OTA was also used a learning case to the software and the workflow of the development for the several different blocks. The many testbenches used and the results of the dimensioning obtained are here presented.

4.2.1 Testbenches

The testbenches are divided into type of assembly.

4.2.1.1 DC, AC and Noise Simulation in a Closed-Loop Assembly

In this assembly, where the output is connected to the negative input, a voltage source with a null voltage drop is connected in the feedback loop to be possible to perform the loop stability analysis, available in Eldo®, which provides the Bode Plots of magnitude and frequency. Noise simulations are also performed.

From the DC operating point it is possible to extract the following measures:

- Current Consumption \( I_{DD} \) - Current that is passing through the DC analog voltage source. It is measured in Amperes, A.
- Voltage offset \( V_{offset} \) - Difference between the DC voltage at the output and the common mode voltage. It is measured in volts, V.
- Device area \( AREA \) - Area correspondent to the transistors and to the capacitor. It is measured in \( \mu m^2 \).

From this AC simulation, it is possible to extract the following measures:
• Power Supply Rejection Ratio \( [\text{PSRR}] \) - It is measured by doing an AC analysis considering an AC voltage source at the supply source.

From the loop stability simulation, it is possible to extract the following measures:

• Open loop DC gain \( [\text{GDC}] \) - Gain of the amplifier when no feedback is applied, measured in \( dB \).
• Gain Bandwidth \( [\text{GBW}] \) - It is the product between the gain and the amplifier bandwidth, measured in \( Hz \).
• Phase Margin \( [\text{PM}] \) - The difference between the phase introduced by the OTA and 180°, measured in degree.

From the \( .NOISE \) command, the following measures are attain:

• Output Noise \( [\text{NO}] \) - The root-mean-square value of the noise, measured in \( mV \).
• Signal Noise \( [\text{SN}] \) - The noise at the frequency when the gain is unitary, measured in \( mV/\sqrt{Hz} \).

### 4.2.1.2 Transient Simulation, in a Closed-Loop Assembly

The transient simulation allow the measure of:

• Slew Rate \( [\text{SR}] \) - It is obtained by picking the slope of the output voltage when the input common mode voltage goes from null to the desired common mode voltage, and it measures the speed of the response of the OTA. It is expressed in seconds.

### 4.2.2 Dimensioning

In Table 4-2 the dimensioning of the OTA is exhibit. It is necessary to take into consideration that the transistors in the mirror stage were divided to achieve a total length of 2.8 \( \mu m \), with two equal transistors in series. The effective width field in the table corresponds to a single transistor.

<table>
<thead>
<tr>
<th>Active Load</th>
<th>Differential Pair</th>
<th>2(^{nd}) Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>x_al[( \mu m )] l_al[( \mu m )] m_al Effective Width[( \mu m )]</td>
<td>x_dp[( \mu m )] l_dp[( \mu m )] m_dp Effective Width[( \mu m )]</td>
<td>x_2s[( \mu m )] l_2s[( \mu m )] m_2s Effective Width[( \mu m )]</td>
</tr>
<tr>
<td>6.1 3.65 2 25.8</td>
<td>10.8 2.9 7 32.7</td>
<td>13.9 1.8 6 35.3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mirror</td>
</tr>
<tr>
<td>x_b[( \mu m )] l_b[( \mu m )] m_1b m_2b m_b Effective Width[( \mu m )]</td>
</tr>
<tr>
<td>3.5 1.4 5 14 2 13.2</td>
</tr>
</tbody>
</table>
4.2.1 Results

The Table 4-3 sums up the results of the OTA respecting the dimensioning presented in Table 4-2.

<table>
<thead>
<tr>
<th>Measure</th>
<th>Expected</th>
<th>Typical</th>
<th>Worst Case</th>
<th>Best Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{dd} [\mu A] ) &lt;= 300</td>
<td>211.95</td>
<td>240.75</td>
<td>184.54</td>
<td></td>
</tr>
<tr>
<td>GDC( [dB] ) &gt;= 70</td>
<td>102.94</td>
<td>99.081</td>
<td>105.68</td>
<td></td>
</tr>
<tr>
<td>PSRR( [dB] ) &gt;= 60</td>
<td>86.574</td>
<td>72.044</td>
<td>89.914</td>
<td></td>
</tr>
<tr>
<td>GBW( [MHz] ) &gt;= 0.1</td>
<td>4.3354</td>
<td>3.2434</td>
<td>5.9151</td>
<td></td>
</tr>
<tr>
<td>PM( [\circ] ) 60 to 90</td>
<td>62.493</td>
<td>59.804</td>
<td>65.308</td>
<td></td>
</tr>
<tr>
<td>VOFF( [\mu V] ) &lt;= 100</td>
<td>0.33826</td>
<td>12.6074</td>
<td>0.24646</td>
<td></td>
</tr>
<tr>
<td>NO( [mV] ) &lt;= 0.15</td>
<td>0.052107</td>
<td>0.060973</td>
<td>0.044293</td>
<td></td>
</tr>
<tr>
<td>SN( [mV /\sqrt{Hz}] ) &lt;= 15</td>
<td>12.443</td>
<td>16.823</td>
<td>0.90068</td>
<td></td>
</tr>
<tr>
<td>SR( [MV/s] ) &gt;= 0.5</td>
<td>4.4162</td>
<td>2.5468</td>
<td>5.9494</td>
<td></td>
</tr>
<tr>
<td>AREA( [\mu m^2] ) &lt;= 15000</td>
<td>13528</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4.3 BGV

4.3.1 Testbenches

The testbenches that were used are presented in following subsections and are divided into type of simulation: AC, DC and TRAN. The circuit testbench is represented in Figure 4-7, where the only alteration for the different simulations is the use of different voltage sources types.

![Figure 4-7 Generic testbench for testing the BGV circuit.](image)
4.3.1.1 DC simulations

There are two different kinds of DC simulations: one which simply evaluates the DC operating point swept from -25°C to 125°C and the other where a voltage source is inserted at the control input of the startup circuit and swept from 0 to 3.3 V in order to check the unique operation point of the circuit. The measures are the following:

- Output Voltage

The output voltage analysis reveals the quality of the BGV output regarding the temperature variations and if it is approximately the 1.25 V at 25°C required. The TC is the figure of merit that measures the stability during temperature variations. It could be required a more balanced output in a way that the curvature of the voltage has its minimums (or maximums, depending of the concavity of the curve) at the same voltage.

![Figure 4-8 TC measurement by interval.](image)

For that, the TC can be measured by equation (41), where \( n \) represent each interval. An interval can be defined by the temperature length in which the curve maintains the same monotony. An example of a BGV with \( 1^{\text{st}} \) order compensation is depicted Figure 4-8. In the case of \( 2^{\text{nd}} \) order compensations, more complex curvature could arise and this measurement will be separated in more intervals.

\[
TC_{\text{Ref}_n} = \frac{1}{\text{Reference}} \frac{\partial \text{Reference}_n}{\partial \text{Temperature}_n} \times 10^6 \text{[ppm/°C]}
\]  

(41)

To measure if the value of the BGV output is close to the desired 1.25 V, the DC value at 25°C, which is the typical temperature, is compared to the 1.25 V, as represented in equations (42).

\[
VOFF25 = |1.25 - V_{\text{ref@25°C}}| [V]
\]  

(42)
• **Supply Current**

The way to measure the power consumptions of the circuit is done by measuring the current of the analog voltage source at 25°C.

• **Current Control**

Considering the imposition that the circuit current in every branch much be higher than 10μA, and that the lowest current branch is the $R_9$ branch, this branch was managed to have no less than 10μA. This current is PTAT, so the voltage value that is supervised is the one at −125°C.

4.3.1.2 **AC simulations**

The only purpose of the AC simulation is to measure the influence that noise in power supply has in the reference voltage generated, by measuring the PSRR. The PSRR is measured by doing an AC analysis considering an AC voltage source in series with the supply source and it is measured after the output low pass filter formed by a 5kΩ resistor and 100nF capacitor.

4.3.1.3 **Transient Simulations**

There are two kinds of transient simulations used to test the circuit, one to simulate the power down mode and other to test the stability of the circuit. The measures are the following:

• **Power Down**

Power down allows to disabled the circuit in order to have almost zero current consumption when it not desirable. This simulation will allow to analyze the current and voltage behavior during enable mode, disable mode and during the transition of modes.

• **Unique DC Operating Point**

This is verified by opening the loop between the output voltage of the OTA and startup input. By replacing the startup input with a DC source that can be swept from 0 to 3.3V it can be shown if the startup circuit is sufficient to initiate the BGV, that it has only one operating point and that the influence of the startup is null in the output voltage.

4.3.1.4 **Area**

For each of the components, it was chosen that the area of the transistors is represented by equation (37), the area of the resistors by the (30), the area of capacitors by equation (31) and the BJT by equation (32). This is only an estimative of the true value of the area, which will differ from the value after layout due to the calculations do not take into account the space between components, routing and pads, and because the equations by itself are not exact.
4.3.2 Results

4.3.2.1 2nd Order Results

The results obtained are summarized in Table 4-4. The Worst case and Best Case corresponds to the corners simulations results obtained, where the corner correspondent to that evaluation is in the #Corner column. The $l_{min}$ value corresponds to the minimum value of the current obtained in a branch of the circuit, except for the 2nd order correction branches.

<table>
<thead>
<tr>
<th>Measure</th>
<th>Expected</th>
<th>Typical</th>
<th>Worst Case</th>
<th>#Corner</th>
<th>Best Case</th>
<th>#Corner</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD} [\mu A]$</td>
<td>&lt;= 3000</td>
<td>737</td>
<td>962</td>
<td>2</td>
<td>570</td>
<td>7</td>
</tr>
<tr>
<td>$I_{min} [\mu A]$</td>
<td>&gt;= 10</td>
<td>10.45</td>
<td>9.65</td>
<td>5</td>
<td>11.39</td>
<td>1</td>
</tr>
<tr>
<td>$TC [\text{ppm/\text{C}}]$</td>
<td>&lt;= 10</td>
<td>2</td>
<td>10.991</td>
<td>1 to 8</td>
<td>&lt;= 2</td>
<td>9 to 20</td>
</tr>
<tr>
<td>$V_{Ref} [V]$</td>
<td>= 1.250</td>
<td>1.249</td>
<td>1.274/1.251</td>
<td>1 to 4/5 to 8</td>
<td>&lt;= 1.249</td>
<td>9 to 20</td>
</tr>
<tr>
<td>PSRR [dB]</td>
<td>&gt;= 60</td>
<td>84.406</td>
<td>81.926</td>
<td>3</td>
<td>87.445</td>
<td>6</td>
</tr>
<tr>
<td>Area</td>
<td>&lt;= 30000</td>
<td>26356</td>
<td>(resistor area 16672) (capacitor area: 1437)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In the next sections there will be shown the characteristic waveforms of the BGV designed circuit.

4.3.2.1.1 Output Voltage

The output voltage for typical results is present in Figure 4-9. The waveform that was obtained presents the expected 2nd order aspect, where the voltage range is equivalent $0.1 \text{mV}$, from 1.2949 V to 1.2489 V.

![Figure 4-9 Output BGV Voltage waveform in the typical conditions.](image)

In Figure 4-10 the corners output waveforms are represented. For corners with values 1, 2, 4 and the curve is descendant, and to the corners with values 5, 6, 7 and 8 the curve is ascendant. These cases correspond to the corners where the components are in worst power and worst speed mode, respectively.
Figure 4-10 Output BGV Voltage waveform in: a) All corners b) Upper Corners c) “Middle” Corners d) “Lower” Corners

In Figure 4-11 there are represent the Monte Carlo simulations results, with Gaussian $3\sigma$ distribution. The total numbers of runs are 1000, considering that parameters of different devices have some degree of correlation – LOT/DEV option. These results show that the output voltage will fall into a value between 1.32V and 1.15V.

The Figure 4-12 shows the Statistical Analysis of Monte Carlo simulations results. The mean value for the temperature coefficient is 23.29 ppm/°C, with a standard deviation of 17.63 ppm/°C.
Figure 4-11 Output BGV voltage waveforms for Monte Carlo simulations.

Figure 4-12 Statistical Analysis of Monte Carlo simulations results.

4.3.2.1.2 Stability

Although the Continuation Method presented in 3.5.2.1 looked like an interesting and precise way to analyze the stability of the BGV circuit, it was not possible to take conclusions through the that method
because the waveform resulted would not lead to any conclusion. So, the approach chosen to evaluate the stability of the circuit is the unique DC point and by observing the Monte Carlo simulation results and see if all of them converge to a voltage around 1.25\(V\). The unique DC operating point simulations results for corners are Figure 4-13 and it shows that that by turning off the startup, it goes to the desired point of functioning, without affecting the output.

![Graph](image1.png)

**Figure 4-13 a)** Output BGV voltage for the Unique DC Operating Point simulation **Output b)** Voltage source at startup input sweep in corners conditions.

The dimensioning of the resistor \(R_{\text{st}}\), which controls the startup mechanism, was done by sweeping the resistor value until the circuit becomes stable and the value achieved for the resistor was 47\(k\Omega\).

### 4.3.2.1.3 Power Down

The Power Down simulations are done by starting with the Power Down in Enabled Mode, meaning that the circuit is off, to then change the Power Down mode to disabled. The signal that controls the Power Down goes from Disabled to Enabled in 100\(ms\), to be changed again from Enabled to Disabled after 2.5 seconds.
The output BGV voltage is shown in Figure 4-14, and where all corners voltage values land at the approximated 1.25\(V\), the 2.4\(s\) and 2.5\(s\). There are no limitations for the startup time, so this can be considered an acceptable value.

![Figure 4-14 Output BGV voltage for Power Down simulation in corners conditions.](image)

4.3.2.1.4 Current Consumption

In Figure 4-15 a) can be observe that the values of the current consumed vary a lot from corner to corner. After analyzing all the blocks, the one that presented the largest variation was the startup circuit, as can be seen in Figure 4-15 b), more specially the first invertor in the startup mechanism, as can be seen in Figure 4-15 c). The reason for this misbehavior is that the invertor is not well dimensioned for the different ranges of voltage that the startup resistor produces, for the several corners, putting the invertor in a middle working stage that causes the abnormal current consumption.

In Figure 4-16 there are represented the current consumption in typical of startup circuit, bias generator and full circuit when the Power Down is in Disable mode, showing that are still current being consumed – almost 20\% of the consumption in Enable mode. There is also observable some leakage current during the invertor inversion of state.
Figure 4-15 Current consumptions at a Full Circuit), b) Startup Circuit and c) First Inverter in Startup Circuit in corners conditions.

Figure 4-16 Current transient waveforms, where the blue represents the startup circuit consumption, yellow the bias voltage generator consumption and orange the total current consumption in Power Down mode.
The PSRR typical and corners simulation results are shown in Figure 4-17.

![PSRR simulation in corners conditions.](image)

**4.3.3 Dimensioning**

The dimensioning of the transistors is presented in Table 4-5, and the resistors in Table 4-6.

**Table 4-5 Dimensioning of the BGV circuit.**

<table>
<thead>
<tr>
<th>Mirror</th>
<th>Mirror Cascode Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>(x_m) [(\mu m)]</td>
<td>(l_m) [(\mu m)]</td>
</tr>
<tr>
<td>9.3</td>
<td>1.75</td>
</tr>
</tbody>
</table>

**Bias Generator**

| \(x_{\text{ig}}\) [\(\mu m\)] | \(l_{\text{ig}}\) [\(\mu m\)] | \(m_{\text{ig}}\) | Effective Width [\(\mu m\)] | \(x_{\text{im}}\) [\(\mu m\)] | \(l_{\text{im}}\) [\(\mu m\)] | \(m_{\text{im}}\) | Effective Width [\(\mu m\)] | \(x_{\text{bv}}\) [\(\mu m\)] | \(l_{\text{bv}}\) [\(\mu m\)] | \(m_{\text{bv}}\) | Effective Width [\(\mu m\)] |
| 2.4 | 2.75 | 1 | 15.43 | 4.8 | 1.9 | 3 | 52.36 | 2.5 | 3.15 | 2 | 33.9 |

**Startup Invertors Power Down**

| \(x_{\text{s1}}\) [\(\mu m\)] | \(l_{\text{s1}}\) [\(\mu m\)] | \(m_{\text{s1}}\) | Effective Width [\(\mu m\)] | \(x_{\text{inv}}\) [\(\mu m\)] | \(l_{\text{inv}}\) [\(\mu m\)] | \(m_{\text{inv}}\) | Effective Width [\(\mu m\)] | \(x_{\text{pd}}\) [\(\mu m\)] | \(l_{\text{pd}}\) [\(\mu m\)] | \(m_{\text{pd}}\) | Effective Width [\(\mu m\)] |
| 10 | 10 | 3 | 117.18 | P | N | 1 | P | N | 1 | 0.350 | 1 | P | N |

| 12 | 2 | 2 | 1 | P | N | 32.14 | 12.14 | 1 | 1 | 4.69 | 4.6 |
### Table 4-6 Dimensioning of the BGV resistors.

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Value [Ω]</th>
<th>Length [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_0$</td>
<td>3.518k</td>
<td>54</td>
</tr>
<tr>
<td>$R_1$</td>
<td>31.643k</td>
<td>504</td>
</tr>
<tr>
<td>$R_2$</td>
<td>31.643k</td>
<td>504</td>
</tr>
<tr>
<td>$R_3$</td>
<td>35.330k</td>
<td>563</td>
</tr>
<tr>
<td>$R_{20P}$</td>
<td>12.143k</td>
<td>192</td>
</tr>
<tr>
<td>$R_{20N}$</td>
<td>13.705k</td>
<td>217</td>
</tr>
</tbody>
</table>

#### 4.3.1 Comparison with 1st Order Results

When comparing a 1st order with a 2nd order BGV, it is possible to see the improvements that are faced. The 1st order BGV, dimensioned in a first phase of this project, has a TC of 10.28 ppm/℃. The expected different curvature can also be observed, where the 1st order output has a quadratic form and after the 2nd order compensation, no longer presents the 2nd order appearance, looking like a 3rd order function.

![Normalized curves at their voltage at 25°C.](image)

#### 4.3.2 PTAT, CTAT and Correction terms observation

In Figure 4-19 it is possible to observing the curves correspondent to each of the terms that summed comprise the generated voltage, where the red curve corresponds to the CTAT current flowing through $R_0$, the yellow curve to the PTAT current flowing through $R_1$ and $R_2$, the orange curve to the current flowing through the resistor $R_3$, the blue curve to the current flowing though the BJT in the 2nd order
branch, the green curve and the purple curve to the current flowing through the resistor \( R_{20P} \) and \( R_{20N} \) correspondingly.

It is possible to conclude that the resistors have a large impact on the output voltage when inspecting the current that flows through \( R_3 \). It was expected that this current had the BGV characteristic curve, but instead it is a ascendant curve. Only when combined with the \( R_3 \) negative TC it produces the desired voltage curve stable over the temperature variations.

One of the limitations imposed initially through the circuit was the need of at least a current of \( 10 \mu A \) in each of the branches of the circuit. It happens that the second order compensation curves don’t comply with that, having a current of about \( 1.5 \mu A \).

![Figure 4-19 a) Current that make the BGV variations with temperature, b) close up of second order compensation currents.](image)

### 4.3.3 Ideal Amplifier

One of the initial objectives was to dimension a chopping amplifier in order to decrease the effects of the OTA voltage offset in the BGV voltage reference. The ideal amplifier used, present in the Cadence© library had no offset and a 100dB gain. In Figure 4-20 is presented the waveform of the output BGV voltage, with a TC of 3.6 \( ppm/\degree C \), which is a worse result from the obtained with the OTA amplifier. This can be justified because the dimensioning of the resistors itself eventually compensates the offset voltage and by changing the amplifier, it ends in a decompensating the correction and the output waveform is affected. This can not be secured as the offset can have variations that are not related with the resistors and can increase the error of the BGV output.
4.3.4 Resistor Splitting

The resistors lengths dimensioned are in order of the hundreds of $\mu m$ of continuous polysilicon filaments, but their layout implementation is against the good layout practices usually followed to prevent that during the process these filaments broke and affects the circuit. One of the ways to turn around this obstacle is to divide the resistors in smaller blocks and connect them in series to reach the resistor value firstly dimensioned. Preferably, the size of these blocks is equal to all of the resistors in the circuit, in order to apply matching layout techniques, which helps to diminish the effects of process variations during fabrication.

In Table 4-7 there are the values used for the simulation where the results are presented in Figure 4-21. The size of the single resistor block is $9\mu m$, which translates to a resistor of $705\Omega$. 

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Nº of Blocks</th>
<th>Length</th>
<th>Relative error(resistors)</th>
<th>Value [kΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_0$</td>
<td>6</td>
<td>54</td>
<td>0</td>
<td>3.518</td>
</tr>
<tr>
<td>$R_1$</td>
<td>56</td>
<td>504</td>
<td>0</td>
<td>31.643</td>
</tr>
<tr>
<td>$R_2$</td>
<td>56</td>
<td>504</td>
<td>0</td>
<td>31.643</td>
</tr>
<tr>
<td>$R_3$</td>
<td>62</td>
<td>558</td>
<td>0.89</td>
<td>35.018</td>
</tr>
<tr>
<td>$R_{20N}$</td>
<td>21</td>
<td>189</td>
<td>0.46</td>
<td>11.955</td>
</tr>
<tr>
<td>$R_{20P}$</td>
<td>24</td>
<td>216</td>
<td>1.56</td>
<td>13.643</td>
</tr>
</tbody>
</table>
The results obtained when doing the resistor splitting were not satisfactory, with the TC being 11.26 ppm/°C for typical condition. This happens because the division of the resistors in blocks did not match the dimension sizes and due to the possible variation of the TC of the resistor itself, which already has proved to be crucial in the BGV dimensioned value.

An alternative can be use different single resistor blocks for the different resistors, or to use a resistor in a serpentine configuration, which it was not explored during the development of the thesis.

### 4.4 Conclusions

Although the first reaction to the overall performance of the circuit was positive when compared with previous proposed circuit results in Table 4-8, for corners and typical, after a deeper analysis there are still some smaller fixes that are needed to advance to the next step of the project – the layout. Starting by the result comparison table, although considered a relatively relaxed constrain when comparing with others FOM, the circuit has a slow starting when compared, considering that the testbench is the same, which was not possible to ascertain.
Table 4-8 Results comparison between the previously proposed design and the design presented in the thesis.

<table>
<thead>
<tr>
<th>Measure</th>
<th>My Design Typical</th>
<th>My Design Worst Case</th>
<th>Previous design Typical</th>
<th>Previous design Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DO}[mA]$</td>
<td>0.737</td>
<td>0.962</td>
<td>2.34</td>
<td>3.35</td>
</tr>
<tr>
<td>$TC$ [ppm/°C]</td>
<td>2</td>
<td>10.991</td>
<td>7.75</td>
<td>10.46</td>
</tr>
<tr>
<td>$V_{ref}[V]$</td>
<td>1.249</td>
<td>1.274/1.251</td>
<td>1.235</td>
<td>1.21/1.26</td>
</tr>
<tr>
<td>$PSRR[dB]$</td>
<td>84.406</td>
<td>81.926</td>
<td>56.54</td>
<td>646.95</td>
</tr>
</tbody>
</table>

In the evaluation of the output voltage over time in Corner Cases, section 4.3.2.1.1, shown that when the components change to worst power and worst speed modes, the output voltage differ more than others corners situations. The Monte Carlo simulations proved that it is possible that after fabrication the circuit behavior could be far from the intention, being essential incorporate a trimming section – the development of this section was initiated but due to time constrains there was not possible to reach a conclusion.

In section 4.3.2.1.2, the stability subject is addressed. This was one of the critic points during the simulation and dimensioning of the circuit, as it involved understating the simulator behavior, where simulator settings like imposing starting values to the DC voltages of the circuit were used at some stages of this work. In my opinion, it is truly necessary to validate the stability of the circuit and the startup used in this work overcome almost all the tests, accepts in Cadence environment where it was not consistent with simulations in plain ELDO environment.

In relation of the dimensioning of the circuit, some parts must need a rework in order to diminish the current consumption, as stated in 4.3.2.1.4 and a general rework of the values of the resistors must needed if the “current over 10$\mu$A” constraint must not be broken in the special case of the compensation current, as stated in 4.3.2. Doing a rough estimate, to reproduce the same effect all the currents needed to be at least higher by factor of 7 but the resistors will also grow by that factor to keep the output voltage at the same value and the current consumption could get to 5mA. A possible conclusion is that with this compensation, the 2nd order currents cannot be higher than 10$\mu$A.

The thesis here presented was greatly influenced by the use of the circuit optimized developed in the group work $\textit{AIDA-C}$. The tool helps to cut a considerable amount of time in the dimensioning phase, especially in the $\textit{trimming}$ segment where minor changes in sizes where done to achieve the best possible performance. In my experience, this is normally the most fatigued stage in developing an analog IC. The usual workflow used was to pre-dimension the circuit in $\textit{Cadence© Virtuoso}$ and then use $\textit{AIDA-C}$ in an iterative way, starting with relaxed constrains when comparing with the results wanted and by altering optimization with manual simulations. The pre-dimensioned was essential to not let the optimizer converge to a solution that was not desirable.

Although it looks like the $\textit{AIDA-C}$ does all the designer work, it is far from the truth as the designer must still do a lot of work and must have a great care with the definition of the measures. For example,
when the measures of the transistors overdrives and voltage deltas were made with an absolute value of the characteristics of the MOS transistors, and a good final dimensioning of the circuit was obtained where the transistors were not working in the saturation region.
CONCLUSION

In this thesis, the developed BGV was presented, including a dimensioning of the several circuits and the results of the developed testbenches. The chapter presents the closing remarks, and the future directions for continuing the development of the circuit.

5.1 Conclusions

The circuit developed achieved the principal objective of accomplish a complete BGV with a 2\textsuperscript{nd} order correction, with a better performance that suits the specification and the corners cases used in the project, including Monte Carlo analysis when needed.

Besides implementing the BGV core, a two stage OTA with Miller Compensation, a startup circuit, a bias voltage and current generator were also implemented. As a means to achieve the goal, was suggested the use of a chopped amplifier and a trimming section but both those suggestions were not implemented. A development of a trimming section was also initiated with the architecture suggested in this thesis, but there was not possible to draw a conclusion about the character of those trimming section.

\textit{AIDA-C} proved to be an useful tool that can easily be integrated in the workflow and can even be considered a central point in the dimensioning of the circuit without replacing the role of the designer in the development of an IC. It is principal effective in the moments where the sharpening of the circuit it is performed, which can be tedious and not glorifying. The tool also settled as a great environment for manual dimensioning, where it is possible to perform parametric sweep simulations and verify the constraint infractions for each parameter value, after running an optimization.
5.1 Future Work

The intention is that the work in this thesis is to be continued and for that this document will also work as guide to lead who will extend the developed circuit. For that, as a suggestion, next will be presented some of the objectives for the future work.

1. During the final analysis of this work some abnormal situation were detected, as for example current consumption in power down mode. These situations are well detailed in the section 4, to the point of indicating how to fix the error. It is suggested that as a starting point to run all simulation here presented to verify the results;

2. The verification of the stability of the circuit can be an interesting point to prove because although the circuit has passed all the tests, it is not objectively proved that there are no other stable points outside the desired. A method to prove it is presented in section 3.5.2.1.

3. Implement the trimming section is the key to believe that the circuit can still have a high performance after the fabrication, especially for the TC parameter. The actual circuit status still leaves some doubts about the behavior after process.

4. Depending of the analysis of the trimming section, two things can happen: if the TC is satisfactory for all the simulations, then an implementation of a chopper amplifier can be done. This kind of amplifier effectively decreases the noise and the offset and by integrated it in the BGV design, a more stable output voltage can be conquest. If the TC values are still not acceptable, then some alternatives must be chosen between second order correction, by either changing the one that is used actually or by adding another compensation atop the existent.
A.1 BJT Collector Voltage Variation through temperature, for a Current Variation of 10μ to 20μ

The graph in Figure A-1 displays the results of the simulation of the limit values of the BJT qP4 collector voltage used in the design. The collector of the BJTss is connected to the OTA amplifier inputs, so the limit values were used as corner values for the common mode voltage of the OTA.

Figure A-1 BJT collector voltage variation through temperature, for a current variation of 10μ to 20μ.
A.2 SPECTRE ELT MOS MODEL

The Spectre™ ELT model, Figure A-2, were developed to include them when Spectre™ was the only simulator available in Cadence® environment.

A.3 ELT CALCULATOR

In order to translate the dimensioning of the transistor from the $x$ and $y$ dimensions of the ELT to the typical $w$ Width of the MOS transistor, the calculator sheet represented in Figure A-3 was used.

A.4 BGV Final Circuit
**A.5 Corner Cases for the 2nd Order BGV Circuit.**

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<th>Temperature [°C]</th>
<th>Source [V]</th>
<th>Bias [mA]</th>
<th>Corner Case</th>
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<td>max.</td>
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Table A-1: Corners Cases for 2nd Order BGV Circuit.
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REFERENCES


[10] Previous Proposed Bandgap Report


