AIDA-PEx: Accurate Parasitic Extraction for Layout-Aware Analog Integrated Circuit Sizing

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Abstract— This paper presents a new parasitic extractor (PEx) embedded in an automatic layout-aware IC synthesis tool, AIDA, and has the main goal of providing accurate parasitic estimates to lead and accelerate the layout/parasitic-aware optimization of the circuit. Finding a circuit sizing solution that fulfills all specifications after circuit layout is a time-consuming task that requires non-systematic iterations between electrical and physical design steps, which increases the design time of analog integrated circuits (ICs). The performance of automatic layout-aware IC sizing methodologies is heavily dependent on the promptitude of the iterations. The in-loop circuit evaluation encompasses three main steps: circuit simulation, layout generation and parasitic extraction. The proposed approach, unlike previous approaches, it estimates the parasitic capacitances and resistances from a simplified layout that include the floorplan and a non-detailed routing, using an empirical method supported by the data from the process design kit (PDK) files. Experimental results are presented for the UMC 0.13μm process and compared with the industry standard Mentor Graphics’ Calibre®.

I. INTRODUCTION

The behavior of analog ICs is extremely sensitive to layout induced parasitics that affect the circuit’s performance, often rendering it non-functional. Traditionally, the circuit synthesis step is followed by layout generation and the steps are carried out independently from each other. Then, a verification step that checks if the desired performance goals are still achieved in post-layout simulation, i.e., in the presence of layout parasitics, follows. If the post-layout circuit’s performance meets the specifications, the design is complete; otherwise, the design goes back to the circuit synthesis or layout generation steps. This iterative approach is extremely time-consuming and no structured feedback from previous runs can be readily used in the circuits’ re-design. Therefore, layout-aware synthesis approaches where layout generation and parasitic extraction are included in the automatic sizing loop, to consider the parasitic effects earlier in the design flow, have emerged [1].

This work focuses on the parasitic extraction step of the layout-aware sizing loop, as shown in Fig. 1. There are several existing commercial tools to accurately extract the circuit parasitics (ANSYS Q3D®, StarRC®, QRC®, Calibre®, etc.). The problem using these extractors, in the sizing loop, is either the setup time required to have the entire DRC and LVS-clean layout coded in a procedural generator, which should also be flexible to accommodate different placement and routing layouts, or the execution time required to obtain the complete full layout design using a custom generator, which is one of the most time consuming tasks on the automatic analog layout flow [2]. A special customized tool is then of utmost relevance to a correct and fast parasitic estimation.

The automatic flow in [3] shows the advantages of the layout-aware approach using a simplified layout description, but designers’ trust is in industry “standard” extraction tools, hence it is important to have high accuracy, even in the simplified extraction procedure. The developed AIDA-PEx module is able to run accurately not only over the complete layout, but also over the incomplete layout, which has only the non-detailed routing, and is used in the optimization loop to accelerate the process.

This paper is organized as follows, Section II presents an overview of the related work and contributions. Section III describes the chosen approach to compute the layout parasitic. Then, in Section IV the experimental results are discussed and finally, in Section V, the conclusions are drawn.

Fig. 1. Layout-aware loop in optimization-based sizing.

II. RELATED WORK

The inclusion of layout-related data is crucial to achieve a first-time-right design at the end of the optimization loop, trimming down the impact of parasitic devices in analog circuits’ performance and providing accurate geometrical layout properties, e.g. area, aspect ratio, etc. [4].

A. State-of-the-Art on Layout-aware Sizing

In Table I a revision of the state-of-the-art layout generators and parasitic extractors used in layout-aware analog sizing

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approaches is presented. In [5] a 1/2-D model is chosen but only applied for the area and fringing capacitance of the metall and poly stripes of the circuit’s critical nets, which makes the estimation quick, but loses accuracy and needs user intervention to identify the critical nets. This can lead to errors, if, depending on layout, less critical nets became problematic.

In [6][7][11][12] analytical polynomial models with predictor variables, such as diffusion area/perimeter or even voltages/currents from circuit simulation are used, yielding a very fast estimation of the parasitic impact on circuit’s performance without post-layout simulation. Still these values are just predictions and can have a large error. In [8] analytical models are also used, but the predictor variables related to the transistors’ stress effects, which are distances between components, do require some post-layout analysis.

In [9][10] an external extractor is used which guarantees accurate results for the parasitic estimation. Although the parasitics obtained by using these techniques are very accurate, their inclusion in the optimization loop either forces the creation of a custom parameterized layout, which adds considerable setup time, or using custom full layout generator, which is prohibitively slow to be inside the loop.

B. Contributions

The main contributions of this work are:
1) AIDA-PEx, the proposed extractor, removes the need for the detailed routing, greatly simplifying the in-loop layout generation. In addition, most approaches where parasitic accuracy is high require the detailed layout generation at each iteration, and for that reason, rely on procedural generators that lack the flexibility to handle change, i.e., changing the topology can discard most or all the previous setup work.
2) AIDA-PEx ensures high accuracy when compared to standard industry tools, even when running over the simplified layout, by considering accurate models for the technology dependent parameters and a complete parasitic capacitances extractor.

III. TDK TABLES

This extractor implements an empirical-based approach, where values from the Technology Design Kits (TDK) are used to compute the parasitic components. Although these data is precise, it needs further processing to ensure the less error addition possible. The problem with this data is the small range of values for the look-up variables, which only include four different values of width, and eight different values of space for each one of those widths. Linear interpolation and linear-by-segments interpolation were tested to choose the best one to approximate the table’s data. The results showed that the data had an exponential/logarithmic like function, so a linear-by-segments interpolation revealed to be the best to replicate the TDK data.

IV. PARASITIC EXTRACTION

When avoiding an external extractor it is of the utmost importance to derive reliable estimates for the parasitics. The estimated parasitics in [3] showed consistent approximation for a wide range of tested layouts. But some discrepancies were found in the capacitance estimation for complex layout modules (e.g. interdigitated or common centroid). This work complements the work presented in [3] with a more accurate parasitic capacitance extraction procedure that is closer to commercial tools’ results.

The chosen approach is an empirical-based technique, where several realistic 3-D effects (e.g., coupling capacitances between two interconnects, crossings in different conductors, etc.) are modeled as a combination of 2-D structures, for a 2.5-D modulation of the problem [13]. But the technology-dependent parameters obtained from the PDKs tables are better modeled, and the procedure to calculate the wire and substrate capacitances was revised. Three types of values can be extracted from the technology data: area capacitance ($C_A$), fringe capacitance ($C_F$) and coupling capacitance ($C_C$), as shown in Fig. 2.
A. Substrate Capacitance ($C_s$)

$C_s$ is the conductor’s intrinsic capacitance and is computed by the sum of the area and fringe capacitance components between the conductor (device terminal or wire) and the plane below, i.e., substrate, well or active area, according to (1), where the area capacitive component $C_A$ and fringe capacitive component $C_F$ are obtained by interpolation of the technology-dependent data provided in the foundry’s PDKs as a function of the conductor’s width, and then computed over its length. The space factor in $C_F$ refers to the space between the conductor and the closest shape in that same layer.

$$C_s = (C_A(\text{width}) \times \text{lenght}) + (2 \times C_F(\text{space}) \times \text{length})$$  \quad (1)

B. Interconnect Capacitance ($C_i$)

$C_i$ is the capacitance between two conductors on different layers or in the same layer. If the conductors are in the same layer the fringe components are scorned, and only $C_c$ is considered, as shown in (2), where $C_c(c_{\text{space}})$ is the coupling capacitive component obtained by the interpolation in conductor’s width and $c_{\text{space}}$ (space between conductors) of the PDK values, and $\text{parallel}_\text{lenght}$ is the length in which the two conductors laterally overlap.

$$C_i = (C_c(c_{\text{space}}) \times \text{parallel}_\text{lenght})$$  \quad (2)

If the conductors are in different layers the interconnect parasitic capacitance depends on the area and fringe components between the two conductors according to (3), where $C_A$ is a function of the width on which the two conductors overlap $\text{overlap}_\text{width}$, as shown in Fig. 3 (a).

$$C_i = (C_A(\text{overlap}_\text{width}) + 2 \times C_F(\text{space}) \times \text{parallel}_\text{lenght})$$  \quad (3)

If the conductors do not overlap, (4) is used instead, where only $C_F$ is considered to compute the capacitance, as illustrated in Fig. 3 (b). In this case, the space between conductors must be considered as well, and the value of $C_F$ decays approximately linearly with $c_{\text{space}}$, as presented in Fig. 4. This decay is controlled by $\delta$, which is a technology dependent parameter that is fitted for each layer-pair from the PDK’s data.

$$C_i = 2 \times C_F(\text{space}) \times (1 - \delta \times c_{\text{space}}) \times \text{parallel}_\text{lenght}$$  \quad (4)

Other geometrical considerations to ensure the correctness of the parasitic capacitances of the interconnections are also considered, for example, if the space between shapes is filled by some other shapes, that occupied space is not considered in the determination of the capacitance. Also important, is to ensure that passive devices are properly considered as they can appear as wires.

C. Parasitic Estimation over the Simplified Layout

To increase efficiency of the layout-aware synthesis, AIDA-PEx is used derive the parasitics in a layout that does not have the detailed routing; only an overall routing layout is available. In this scenario, the proposed approach is to assume all routing paths are implemented in the first metal layer, and compute the corresponding parasitics. In standard tools this approach would lead to DRC and LVS errors, but in our approach the routing shapes are associated to the wires, hence is easy to detect unwanted overlaps. In the case of minimum distance violation, which would correspond to design rule violation, the minimum value allowed is considered. In the case of “illegal” overlaps, which would correspond to a short-circuit if implemented, the capacitance is computed assuming that one shape in the first metal and other in the second. This approach is slightly conservative as it always assumes the largest capacitive coupling between shapes, or between shapes and substrate.

V. EXPERIMENTAL RESULTS

A. Single Ended 2-Stage Amplifier

The single ended 2-stage amplifier circuit presented in Fig. 5 (a) was used to compare the results of the parasitic extraction between AIDA-PEx and Calibre®. The circuit was optimized for maximum gain and minimum area using AIDA [14], resulting in the Pareto optimal front (POF) that is illustrated in Fig. 5 (b). The simplified and detailed layouts of the solution with the smallest area showing a DC gain around 50dB are
shown in Fig. 5 (e) and (d), respectively, and the layouts for a solution showing a DC gain of around 75dB are shown in Fig. 5 (e) and (f). The solution with the largest gain was not selected because it was difficult to clearly identify either the simplified or the detailed routing over the layout.

A direct comparison of the extracted capacitances for the 50dB solution is shown in Table II, the values obtained with AIDA-PeX refer to the simplified layout, whereas the values obtained with Calibre® were obtained from the detailed layout. As illustrated in Fig 5, only the routing wires differ, so the results are fairly accurate. Table III shows the post-layout performance for the two circuit implementations. These performance comparisons confirm the precision of the approach and its suitability to be applied in the optimization loop, avoiding the need for in-loop detailed routing.

### TABLE III. PRE/POST-LAYOUT SIMULATION

<table>
<thead>
<tr>
<th>Specs</th>
<th>50 dB</th>
<th>75dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gdc</td>
<td>AIDA-PeX</td>
<td>Calibre®</td>
</tr>
<tr>
<td>Gbw ≥ 50 dB</td>
<td>50.9</td>
<td>50.9</td>
</tr>
<tr>
<td>Area</td>
<td>AIDA-PeX</td>
<td>Calibre®</td>
</tr>
<tr>
<td>Gbw ≥ 200 MHz</td>
<td>204.29</td>
<td>206.30</td>
</tr>
<tr>
<td>Gbw ≤ 200 MHz</td>
<td>74.27</td>
<td>73.54</td>
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<tr>
<td>Gbw ≤ 55 dB</td>
<td>75.44</td>
<td>75.45</td>
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<tr>
<td>Gbw ≤ 5 mV</td>
<td>4.39</td>
<td>4.39</td>
</tr>
<tr>
<td>Gbw ≤ 600 V/m</td>
<td>301.2</td>
<td>305.9</td>
</tr>
<tr>
<td>Gbw ≤ 100 V/m</td>
<td>16.17</td>
<td>16.32</td>
</tr>
</tbody>
</table>

### A. 2-Stage Folded Cascode Amplifier

In this second example, the goal is to demonstrate how a layout-aware approach with accurate parasitic estimations can be valuable for a correct sizing of the circuit that fulfills all the specifications. The circuit used in the optimization process is the two-stage folded cascode amplifier of Fig. 6, where the circuit was sized using the traditional simulation-based optimization and the layout-aware synthesis optimization. In Fig. 7, both traditional simulation-based optimization and layout-aware synthesis POFs are presented, where the circuit sizing solutions that resulted from the traditional one were tested with parasitic effects to evaluate the post-layout performance. From the resulted layouts, only one held the fulfillment of all the specifications (represented by a circle O), and all the other sizing solutions became unfeasible, with one or more specifications not fulfilled (represented by a cross X). The layout-aware POF, although obtaining layouts with a worse performance, guarantees the entire specification fulfillment for all the resulted circuit sizing solutions.

The results for the traditional and for the layout-aware optimization are presented in Table IV, where the performances for the resulted layouts are simulated using the netlist extracted both from AIDA-PeX and from Calibre®. In the traditional simulation-based optimization the parasitic effects are not accounted for, and for that reason, when the layout result is simulated with the inclusion of circuit’s parasitics, the GBW specification is no longer met (whether the circuit is tested on Calibre® or on AIDA-PeX).
without detailed routing for the 75dB solution; (f) Layout with detailed routing (checks DRC and LVS) for the 75dB solution. Note that the layouts of the two circuits are not in the same scale.

Fig. 6. 2-stage folded cascode amplifier

Fig. 7. Traditional and layout-aware optimization POFs

VI. CONCLUSIONS

The proposed lightweight built-in extractor estimates the impact of layout parasitics for both device terminals and simplistic routing without requiring a detailed layout, greatly reducing overall evaluation time in layout-aware optimization. The analog building blocks synthesized for the UMC 130nm shown, in the different experiments that took place, the overall accuracy of the proposed approach.

VII. REFERENCES


### TABLE IV. TRADITIONAL Vs LAYOUT-AWARE POST-LAYOUT SIMULATION

<table>
<thead>
<tr>
<th>Spcs</th>
<th>Traditional</th>
<th>Layout-Aware</th>
<th>Traditional</th>
<th>Layout-Aware</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iss [mA]</td>
<td>5.35</td>
<td>5.62</td>
<td>402.07</td>
<td>392.33</td>
</tr>
<tr>
<td>Gdbw ≤ 400 MHz</td>
<td>408.05</td>
<td>408.2</td>
<td>73.53</td>
<td>73.53</td>
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<tr>
<td>Gdc ≤ 70 dB</td>
<td>73.53</td>
<td>73.53</td>
<td>57.97</td>
<td>57.97</td>
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<tr>
<td>Area ≥ 20k µm²</td>
<td>12.09k</td>
<td>16.49k</td>
<td>59.48</td>
<td>59.48</td>
</tr>
<tr>
<td>Nc ≤ 500 µVrms</td>
<td>197.05</td>
<td>195.37</td>
<td>59.48</td>
<td>59.48</td>
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<tr>
<td>Dv ≥ 55 °</td>
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<td>195.16</td>
<td>59.48</td>
<td>59.48</td>
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<tr>
<td>Dv ≥ 50 mV</td>
<td>50.61</td>
<td>50.48</td>
<td>50.61</td>
<td>50.48</td>
</tr>
<tr>
<td>Dv ≥ 100 mV</td>
<td>105.37</td>
<td>105.06</td>
<td>105.37</td>
<td>105.06</td>
</tr>
</tbody>
</table>

* Performance for the netlist excluding parasitics. ° - Overdrive voltage – Saturation voltage