Title: How Computational Intelligence is Shaping the Art of Analog Layout Synthesis?

Abstract: On today’s semiconductor industry, the integration of complex systems-on-a-chip with analog/radio-frequency (RF) components, multimillion transistor digital processors and dense memory blocks is a widespread practice, and, is only possible due to the continuous advances on electronic design automation (EDA) tools. Still, the degree of analog design automation lags behind its digital counterpart and is expected to reach 50% only by 2020, reflecting negatively in the development costs of analog/RF blocks. While some commercial EDA solutions finally begin to establish on some steps of the analog IC design flow, the process of constructing layouts has stubbornly defied all attempts of automation, even after almost 30 years of research efforts. Therefore, designers continue to use traditional editing environments to manually lay out every device and shape, in an iterative, error-prone and hardly reusable process. This talk, after introducing the “art” of analog layout, digs into the complexity of automating it, the curse of aesthetics, and, revisits previous efforts proposed by the research community. To bypass the failures of the past, the most recent solutions – empowered by modern computational intelligent techniques – promote a gigantic all-inclusive optimization loop, promising to finally close the gap between electrical and physical design steps. However, as analog EDA is starting to move slowly below the 65-nanometer integration technologies new challenges arise, and, existent tools must be prepared for them. Finally, by looking forward, the role of deep learning on speeding-up design cycles in a near future is discussed.

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