Single Inductor Multiple Output (SIMO) integrated DCDC converter control

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Abstract

Mixed-signal system-on-chip designs integrate a variety of subsystems into a single nanometric-scale CMOS chip, each typically requiring a dedicated power supply. However, generating these power supplies requires the use of several bulky external passive components, leading to higher material costs, an increased number of package pins, and more complex and larger circuit designs.

The design of Single Input Multiple Output (SIMO) converters requires a balance between minimizing cross-regulation, maintaining design simplicity, and adapting to a wide range of loads. This work presents the design of a SIMO buck converter using control based on Pulse Width Modulation (PWM).

The design and analysis were carried out using TSMC's 180nm technology with the Synopsys Custom Compiler tool. Two control topologies were developed and evaluated: Multiple Energizing and Single Energizing Control. It was concluded that neither topology is superior to the other, as both exhibit strengths and weaknesses.

Finally, a comparative analysis was conducted between the proposed SIMO converter with Single Energizing Control and conventional buck converters. The results indicate that the SIMO converter achieved highly satisfactory performance, with a maximum voltage rise of 15mV and a maximum voltage drop of 7mV. This demonstrates that it is a viable solution for applications requiring low load currents, on the order of 10mA.

Keywords: DC-DC Converter, SIMO buck Converter, Cross-regulation, Multiple Energizing Control, Single Energizing Control

1. Introduction

The master thesis focuses on developing a control system for an Single Inductor Multiple Output DC-DC converter, an essential component in power regulation for electronic devices such as smartphones and laptops. Voltage regulators (VR), critical in ensuring stable DC voltage, come in two main types: Linear Voltage Regulators (LVR) and Switched-Mode Power Supplies (SMPS), each with specific advantages and drawbacks. LVR, particularly Low-Dropout Regulators (LDO), offer simple designs but are limited by inefficiencies under heavy loads and a single output. In contrast, SMPS are more efficient but require bulkier inductors and generate more switching noise.

To overcome the limitations of these traditional regulators, SIMO converters offer an innovative solution by using a single inductor to support multiple outputs as depicted in **Figure 1**, thus reducing footprint and increasing efficiency [5]. However, SIMO designs are not without challenges. They suffer from issues like cross-regulation [3], where changes in one output affect others and lower power efficiency than regular SMPS due to additional circuitry. Despite these complexities, SIMO converters can extend battery life in portable devices and simplify power management.

The thesis aims to develop a complete control system for a DC-DC SIMO converter in collaboration with Silicongate.

Since developing a SIMO requires more than just a control system, the work will also involve designing essential components like the power and switching blocks to ensure the converter operates effectively.

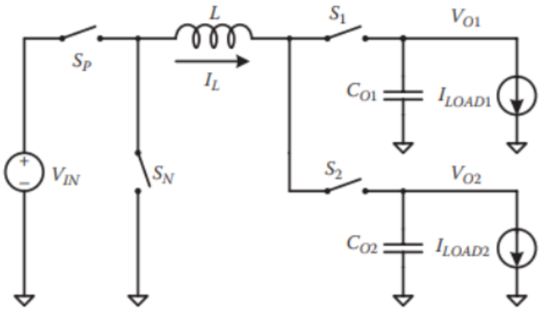


Figure 1: Typically SIMO Buck converter with two outputs from ([1])

Therefore the main challenges/objectives not counting the development of blocks external to the control as indicated above (power, switching) to be achieved in this thesis will be to develop the control that provides:

- The best efficiency for the converter
- Minimum interferences due to cross-regulation
- Good flexibility especially in terms of load conditions
- The lowest possible level of complexity

The objective is to develop two control methods for the SIMO converter: Multiple Energizing and Single Energizing. This will help analyze their advantages and disadvantages to determine if one is more effective. After developing a SIMO converter and completing the control analysis, another goal is to compare the SIMO converter and traditional multiple buck converters. This study aims to highlight the differences between the two approaches and identify scenarios where the SIMO converter is a preferable option.

2. Background

In terms of background, the thesis focuses on the fundamentals of SIMO converters, exploring their operational modes, types, and control methods. The SIMO converter stands out for its ability to supply multiple outputs using a single inductor, making it more efficient and compact compared to conventional methods.

2.1. Single Inductor Multiple Output Conventional Operation Modes

It begins by analyzing the three main operational modes with which this type of converter operates: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Pseudo Continuous Conduction Mode (PCCM). Each mode affects the inductor current differently, influencing the converter's efficiency and performance.

CCM keeps the inductor current flowing continuously facilitating the transfer of the desired power from the input to the corresponding output as depicted at [10]. DCM introduces a dead-time between phases as depicted at [12] where the current is zero, thus limiting the cross-regulation problem, however, it faces challenges related to efficiency and load range. Finally, PCCM helps reduce ripple by maintaining the inductor current above a specific value using a freewheeling switch as shown in [8], however, a crucial consideration involves the selection of the free-wheel switching current level, Idc, to prevent cross-regulation.

2.2. Types of Single Inductor Multiple Output Converters

Regarding the types of SIMO converters, two main types have been studied: Multiple Energizing SIMO and Single Energizing SIMO.

Multiple Energize SIMO as the one presented in [9] operate as a combination of multiple sub-converters, they manage each output with its own energizing cycle, which improves the system's time multiplexing but increases complexity.

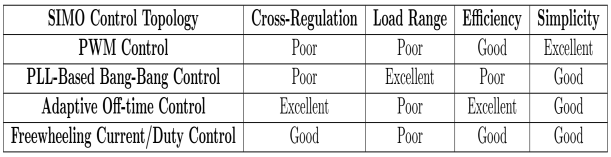
Single Energizing converters like the one in [11], on the other hand, energize the inductor once per cycle and distribute energy to multiple outputs, balancing efficiency and simplicity.

2.3. Single Inductor Multiple Output Conventional Controls

Finally, different control strategies for SIMO converters were explored, including PWM control, PLL-based bang-bang control, adaptive off-time control and Freewheeling Current/Duty Control.

These control techniques are essential in optimizing the performance of SIMO converters, especially in complex load scenarios.

Using the data provided by the articles on which the study was based, it was possible to compare the different topologies and formulate the **Table 1**.



SIMO Control Topology	Cross-Regulation	Load Range	Efficiency	Simplicity
PWM Control	Poor	Poor	Good	Excellent
PLL-Based Bang-Bang Control	Poor	Excellent	Poor	Good
Adaptive Off-time Control	Excellent	Poor	Excellent	Good
Freewheeling Current/Duty Control	Good	Poor	Good	Good

Table 1: Summary of SIMO Designs Discussed in Terms of Performance

The analysis of diverse SIMO converter topologies reveals that no single design is universally optimal, as each offers specific strengths in cross-regulation, efficiency, simplicity, and load range. Choosing the best topology thus depends on application-specific needs.

PWM control was selected for SIMO buck development due to its relative simplicity. The goal was to create a PWM-controlled SIMO that handles a wide load range while minimizing cross-regulation, balancing efficiency with simplicity to achieve robust and versatile performance across various applications.

3. Implementation

Designing a SIMO converter requires balancing cross-regulation, simplicity, and load accommodation. This work introduces a SIMO design that achieves these goals, emphasizing always the simplicity. After evaluating converter types, the buck configuration was chosen for its suitability in portable applications.

In the pursuit of creating the most streamlined converter, the approach began with the development of a PWM-controlled Single Inductor Dual Output (SIDO), leading to the use of a fixed-frequency system for its inherent simplicity.

As mentioned the development began with a SIDO model at 1.2V and 1.6V for the outputs, and later added a third 1.8V output, transforming it into a SIMO system.

The control strategy was adapted to manage all outputs, requiring continuous comparison of voltage drops to prioritize regulation. Initially designed for Multiple Energizing Mode, the system was later restructured to operate in Single Energizing Mode, which is expected to enhance ripple reduction. This comprehensive approach completes the SIMO converter's development, with further details and results to be explored in subsequent sections.

3.1. Single Inductor Dual Output Converter

Firstly the design process for a SIDO buck converter was conducted, with an emphasis on establishing a robust system capable of handling diverse load currents while minimizing output ripple. The initial goal was to develop a functional SIDO as a foundation, addressing output stability and control challenges specific to multi-output converters.

The SIDO design integrates a closed-loop control architecture as depicted in **Figure 2**, with several critical components that support precise operation. A key part of this design is the Comparator, responsible for comparing each output voltage to its specific reference. This comparison generates control signals, specifically 'Cmphyst' and 'Cmphyst2', which help direct the switching sequence and manage the connection to the required outputs.

Another essential component, the Feedback Compensator, implements slope compensation to stabilize the converter's response to rapid load changes, thus improving overall transient responses. This compensator works by maintaining the inductor current's stability during variations in output demand, which is crucial for balancing the two outputs effectively without causing interference between them.

The switching mechanism, driven by feedback, enables precise time multiplexing of the inductor's charge across both outputs. This approach optimizes power distribution by assigning appropriate duty cycles to each output according to its load requirement. Such multiplexing is carefully managed to ensure each output receives adequate energy without generating excessive ripple, balancing efficiency with output stability.

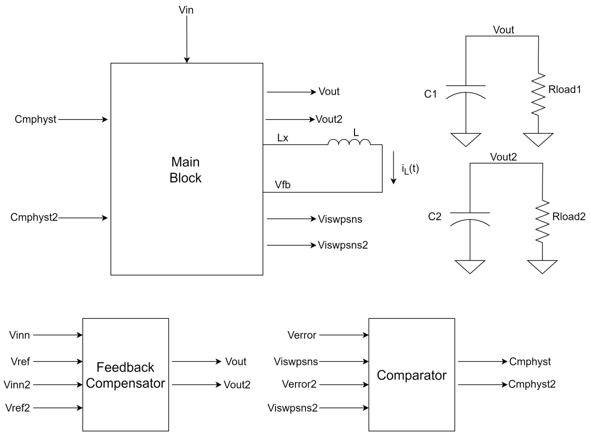


Figure 2: SIDO buck converter developed.

Overall, the design of the SIDO converter focuses on efficient power sharing and stability under variable loads, setting a foundation for expanding into a more complex SIMO system in subsequent stages.

3.2. Single Inductor Multiple Output Converter

3.2.1 Multiple Energizing Control

Following the successful creation of a SIDO system, this project's focus shifted towards achieving a fully functional SIMO system. The primary aim became adapting the control system to accommodate an additional output, thus allowing a single input to manage three outputs efficiently. This adaptation required reevaluating the control system design to enable a third output's integration within the converter's structure.

To implement the third output, the control mechanism's foundational modification involved adjusting the voltage drop comparison process to prioritize the correct output. In the previous SIDO system, a single voltage comparison sufficed, however, with three outputs in the SIMO system, a more comprehensive comparison was necessary, involving three comparative evaluations to prioritize outputs based on voltage drop. The specific comparisons were defined as follows:

- $(Vout\text{-}Vref1) < (Vout2\text{-}Vref2)$
- $(Vout\text{-}Vref1) < (Vout3\text{-}Vref3)$
- $(Vout3\text{-}Vref3) < (Vout2\text{-}Vref2)$

This expanded comparison setup allowed for accurate prioritization, identifying the output under the greatest strain when the swn signal dropped.

As demonstrated in **Figure 3**, Output 1 showed the highest need for attention, guided by a logical comparison mechanism. At the moment when the signal swn falls, each comparator activates, performing a voltage comparison across outputs. For instance, given the values Vout1 = 1.15V, Vout2 = 1.59V, and Vout3 = 1.78V, with references *Vref1=1.2V*, *Vref2=1.6V*, and *Vref3=1.8V*, the resulting voltage differences calculated as -0.05V, -0.01V and -0.02V confirm Output 1's priority.

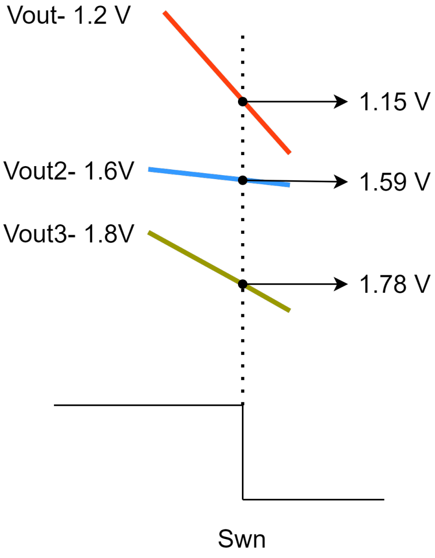


Figure 3: Graph illustrating the process of comparing the voltage drops at the different outputs of the converter, to select the one most in need.

Adjustments in the control system followed, necessitating modifications to accommodate three outputs. Signals were introduced based on these comparisons, specifically cmpdeltav1v3, cmpdeltav1v2, and cmpdeltav3v2, serving dual purposes: resetting and setting signals across outputs.

These signals assessed relative voltage drops between outputs as already mentioned, which subsequently triggered reset signals (‘resetso1‘, ‘resetso2‘, and ‘resetso3‘) for the outputs needing deactivation, **Figure 4**. The reset signals were set based on logical combinations of these comparison signals and were represented visually in diagrams that helped streamline control and eliminate timing conflicts.

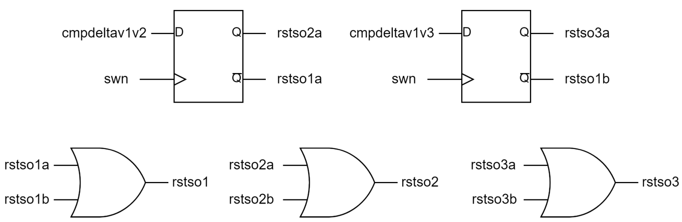


Figure 4: Demonstration of the logic behind the resets

Regarding the logic behind the output set signals, in this configuration, the set signals rely directly on the state of the corresponding reset signals, reducing complexity and improving the overall efficiency of the control system. This direct use of reset signals eliminates the need for extra comparisons, ensuring quicker and more reliable output selection.

This streamlined approach, illustrated in **Figure 5**, shows the logic applied to set the first output.

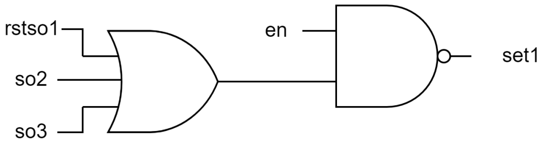


Figure 5: Logic developed to set the first output (so1) in the Multiple Energizing control.

An auxiliary switch (‘saux‘) was also revised, being responsible for providing a path to the current when switching between outputs occurs, initially requiring three separate signals, it was consolidated into one ‘saux‘ signal. as depicted in **Figure 6** to streamline the system, activating only when a change was necessary. This simplification facilitated switching control among outputs based on priority without excess signaling.

Initiasignalling of the three-output control system exposed unexpected race conditions in simulations. These timing conflicts arose from simultaneous state changes in opposite polarity signals used in reset logic. For example, reading cmpdeltav3v2 and its negation, cmpdeltav3v2z, too closely could lead to incorrect resets, resulting in unintended active outputs. Modifying the reset logic to remove negations and employ only three core signals, cmpdeltav1v2, cmpdeltav1v3, and cmpdeltav3v2, resolved this issue by reducing race condition vulnerabilities.

A fault prevention system was also incorporated, introducing a faultcondz signal that defaults to Output 1 in cases where all outputs are reset simultaneously, ensuring operational continuity despite potential voltage comparison errors.

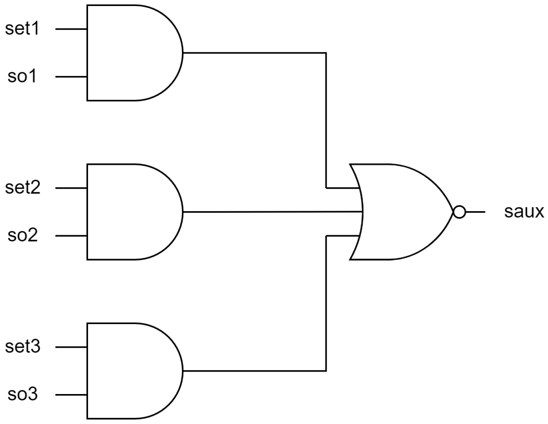


Figure 6: Logic behind the set saux signal, which will activate the saux switch, thus providing a path for current to flow during switching between outputs.

Further adjustments were made to refine the SIMO converter's components. Reviewing capacitor and inductor values from existing converters led to an increase in the inductor value to 10uH and output capacitors to 22uF, allowing operation at maximum loads up to 100mA. Simulation results following these modifications, when compared to those reported in [6], [4], [7], and [2], showed favourable performance outcomes, confirming the stability and effectiveness of the enhanced SIMO converter design.

3.2.2 Single Energizing Control

The development of the SIMO converter progressed from a Multiple Energizing control system to a new Single Energizing configuration aimed at comparing performance metrics such as ripple, cross-regulation, and response speed between the two control types. The Single Energizing SIMO control was designed with an innovative approach, differing from standard methods.

Distinct from traditional controls, which typically limit output switching to either the energizing or discharge phases, the new system allows continuous switching during both. Instead of sequentially energizing and discharging all outputs, this system actively monitors the voltage drop of each output and selects the one with the greatest need. This mechanism is visualized in **Figure 7**, illustrating the operational dynamics and advantages of this control method.

The control method monitors each of the converter's outputs, continuously identifying the one with the greatest voltage drop compared to its reference value. This output is then selected for activation until another output experiences a more significant drop. Each power-up cycle (when either 'swp' or 'swn' is high) restricts switching actions to a maximum of two transitions, optimizing converter efficiency and reducing unnecessary energy loss.

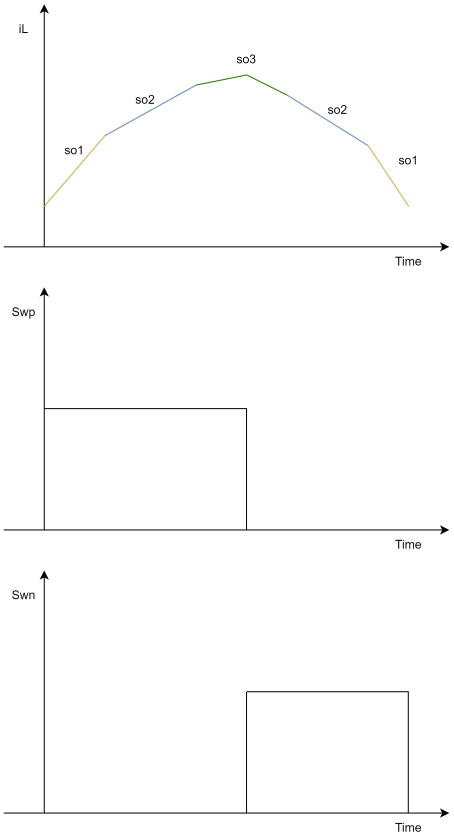


Figure 7: Basic operation behind the Single Energizing control to be developed in this work.

This dynamic approach was chosen to address limitations in conventional controls, such as sequential output analysis, which can result in delays and potentially misprioritize outputs. For example, if the system focuses on an output below its reference but does not represent the most critical need, it might ignore another output with a more significant voltage drop due to sequential analysis. By prioritizing outputs based on real-time voltage drops, the developed control system ensures the converter remains responsive and effective.

As **Figure 8** illustrates, sequential analysis can fail to address the most critical output needs if a later output in the sequence experiences a greater voltage drop. The new approach ensures simultaneous monitoring, thereby avoiding delays and enhancing responsiveness, selecting the output with the greatest need consistently.

In summary, this new control strategy mitigates delays associated with sequential analysis and enhances converter efficiency by ensuring that the output with the most significant voltage drop receives immediate attention.

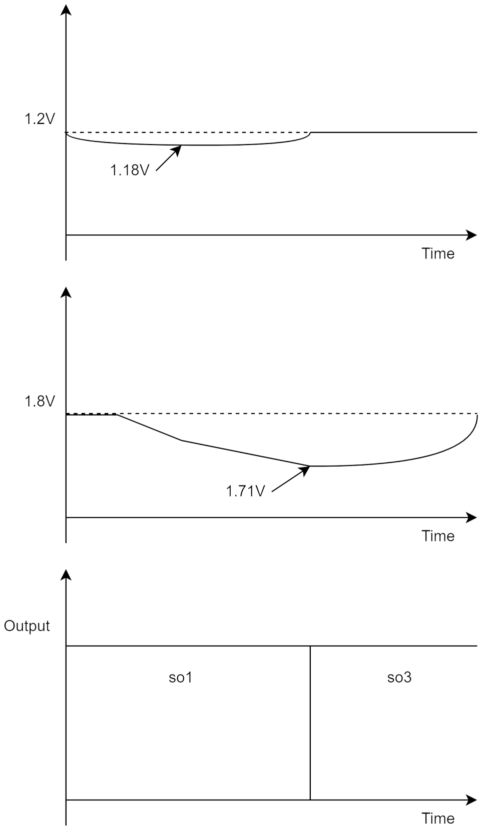


Figure 8: Demonstration of the problem behind the serial methodology in the output set in Single Energizing mode.

After developing the initial control component, we focused on creating a mechanism to reset an output that had been switched off during the remaining duration of its energy cycle. This feature is designed to ensure that the number of switches within the same energy cycle, whether for energization or de-energization, remains limited to a maximum of two. This limitation is essential for optimizing the converter's efficiency. To implement this control system, we introduced six control variables: 'rst1n' and 'rst1p', 'rst2n' and 'rst2p', and 'rst3n' and 'rst3p'. Each output is associated with two variables, one for the energization period (when 'swp' is HIGH) and one for the de-energization period (when 'swn' is HIGH).

To clarify this setup, we focused on the logic behind the 'rst1n' variable. This variable functions as the output of a flip-flop, storing information on when the signal for output 1 transitions to LOW during the 'swn' period. By this mechanism, once the 'so1' signal goes LOW in the de-energization phase, it remains inactive until the end of that discharge period, reducing unnecessary switching. Once the 'swn' cycle ends, the 'rst1n' variable resets, allowing the 'so1' output to become selectable in the next energization cycle, when 'swp' is HIGH.

Building on these variables, we introduced additional variables for the next control component: 'rst1', 'rst2', and 'rst3', 'enrstso1', 'enrstso2', and 'enrstso3'. The 'rst' variables signal whether any output has reset during 'swp HIGH' or 'swn HIGH' periods, facilitating the tracking of output states throughout the cycle. Meanwhile, the 'enrstso' variables serve as reset enable signals, governing whether an output can reset. This structure prevents scenarios where two outputs have already reset while a third remains active but is also in reset. Such cases would result in no output selection, compromising stability in the CCM operation of the converter, which requires at least one active output for consistent performance.

Following the creation of reset enable variables, we moved to the next control component, critical for identifying the output with the most significant voltage drop. This component's main control logic leverages comparison variables—'cmpdeltas', 'cmpdeltav1v3', 'cmpdeltav2v1', and 'cmpdeltav3v2'—which assess each output's voltage drop against its reference, enabling prioritization based on regulatory needs. This logic includes three latches, one for each comparison signal. Each latch produces two reset signals for every output, derived from the comparative results. For instance, output 1 uses 'cmprst1a' and 'cmprst1b' as its primary reset signals.

Figure 9 illustrates the latch designed for the first comparison signal, 'cmpdeltav1v3', a component that determines which output requires the most immediate attention by retaining output states based on the comparison. If 'cmpdeltav1v3' is HIGH, for example, this means the voltage drop on 'so1' surpasses that on 'so3'. Consequently, the 'cmprst3a' signal is set to HIGH, elevating the 'cmprst3' signal. Reset signals are thus generated for each output based on these comparison results. Specifically, 'cmprst1', 'cmprst2', and 'cmprst3' represent the reset signals for outputs 1, 2, and 3, respectively, based on combinations of corresponding 'cmprsta' and 'cmprstb' signals.

To guarantee that each output undergoes appropriate reset processes, the 'cmprst3a' signal remains LOW, initiating a reset for output 3. Additionally, the negation of 'cmpdeltav1v3' resets the latch, maintaining the desired states of 'cmprst3a' and 'cmprst1a' throughout the control block's operation. The reset process for each output, like 'cmprst3a', includes interactions with variables such as 'rst1z' and 'enrstso3', which ensure only necessary resets take place. For instance, 'rst1z' prevents 'cmprst3a’ from deactivating ‘so3’ if ‘so1’ has already reset. This mechanism is crucial, as once an output resets, the comparison involving that output becomes irrelevant; the system will only consider active outputs for subsequent regulations.

An essential OR operation involving ‘rst3’ maintains the ‘cmprst3a’ signal HIGH, signifying that output ‘so3’ has already been reset and should remain inactive until the next cycle. With these mechanisms in place, the control system identifies which output experiences the largest voltage drop, using variables like ‘cmpsetso1’, ‘cmpsetso2’, and ‘cmpsetso3’ for definitive output resets.

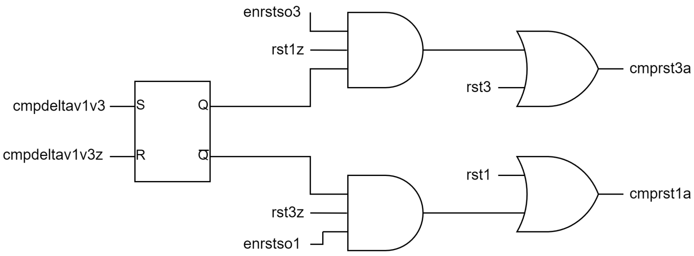


Figure 9: Logic developed to identify which of the cmpdeltas is the most needed output. It is through this system that we will know in this case which of the so1 or so3 outputs should be reset and which should remain ON.

By referencing **Figure 10** for output 1, it’s clear that ‘cmpsetso1z’ represents the negation needed to reset and set this output. This signal reflects the intersection of reset signals from outputs 2 and 3 and will only activate output 1 if these reset signals are HIGH. The latch reset depends on the ‘cmprst’ signal specific to each output, such that whenever ‘cmprst1’ is HIGH, ‘cmpsetso1z’ also goes HIGH to hold output 1 in a reset state.

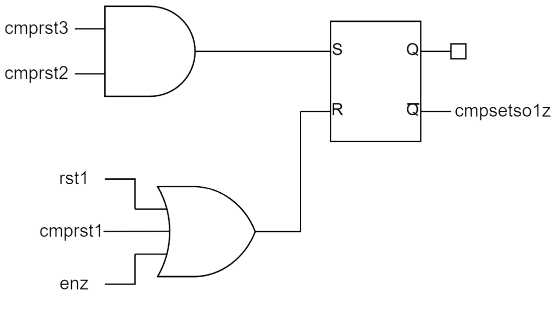


Figure 10: Logic developed to create the cmpsetso1z variable, which will be essential for both resetting and setting (in the event of its negation) the so1 output.

Additional variables, such as ‘rst1’, which goes HIGH when output 1 resets, and ‘enz’, which initializes the latch, play key roles in maintaining a known reset state when the system powers up. These refinements, ensuring that output 1 remains active by default, provide continuity when the enable signal is LOW, thus maintaining a regulated output through transitional periods.

In more complex cases with simultaneous load transients, the control system encountered a scenario where all outputs rose above their reference values after transient removal. Here, only one output was selected, with the others dropping to reference values due to load current rather than active regulation. This behaviour highlighted a need for new variables that respond not only to voltage drops but also to rises, to ensure all outputs receive regulation post-transient. Six control variables were thus introduced, three acting as inversions of the ‘cmpdelta’ variables to detect voltage rises, and three (‘cmpso1’, ‘cmpso2’, ‘cmpso3’) identifying outputs below reference values.

The final control structure incorporates multiplexers to select between two sets of variables: ‘cmpdelta “a”’ variables for the largest voltage drop and ‘cmpdelta “b”’ for the most significant voltage rise. A comparator and flip-flop system involving ‘iloutlow’ and ‘ilneg’ variables was created to monitor inductor currents and determine when the ‘cmpdelta “b”’ variables should take precedence.

With these enhancements, the control system can dynamically adjust to load changes, responding appropriately to both voltage drops and rises, which enhances regulation across all outputs and improves overall converter performance. Following these adjustments, simulations confirmed that the system efficiently managed load transients, regulating outputs to the desired levels even after transient recovery. The improvements enabled the control system’s successful application in the SIMO Multiple Energizing converter, thereby validating its efficiency in both Single and Multiple Energizing configurations. This development phase culminates the methodology used in designing a highly effective SIMO converter control system.

4. Results

This section will summarize the simulations and analyses conducted on the results obtained during the development of the SIMO buck converter controls. It will examine the impact of the number of outputs on this type of converter by comparing the responses of the SIDO and SIMO designs. Additionally, it will evaluate the two types of control developed to highlight their respective advantages and disadvantages. Finally, the section will demonstrate that this type of converter is an excellent choice for applications requiring multiple voltage levels with low loads.

4.1. Single Inductor Dual Output vs Single Inductor Multiple Output

The first step is to analyze the influence of having one more output needed in this type of converter. To this end, and as already mentioned, the responses obtained between the SIDO and SIMO developed were compared.

In this situation, both the SIDO and SIMO converters operate under the same conditions as shown in **Figure 11**, however, a load transient is applied to the third output of the SIMO converter simultaneously with the transients at the first and second outputs.

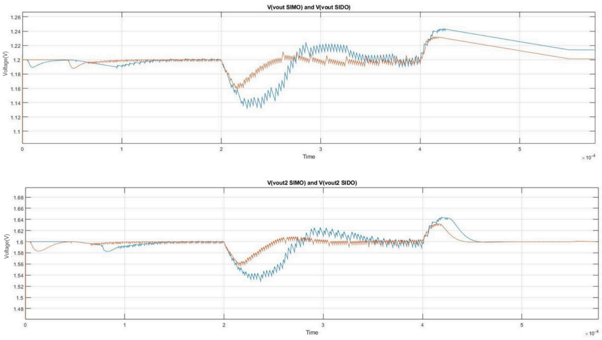


Figure 11: Simulation of SIDO vs SIMO with three load transients applied simultaneously, from 5 to 100mA.

In the first figure in fluorescent magenta we have the voltage on the first output of SIDO and in greenish blue we have that of SIMO. The second figure, in fluorescent magenta, shows the voltage at the first SIDO output and the SIMO output in greenish blue.

In terms of analyzing the responses obtained from the first and second outputs, it is evident that the presence of an additional output requiring attention from the converter has a significant impact. Unlike the results obtained previously, this time we observe a maximum voltage drop of approximately 60 mV at the outputs of the SIMO converter. In comparison, the SIDO converter exhibited a maximum voltage drop of around 40 mV, indicating an increase of 20 mV in the voltage drop at the SIMO outputs.

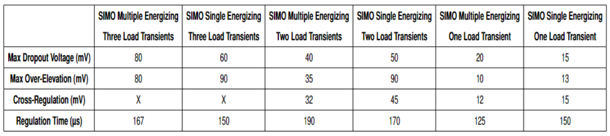
Furthermore, regarding the regulation time, there is a noticeable increase in the SIMO case. The SIDO converter achieves a regulation time of approximately 150 µs, whereas the SIMO converter demonstrates a longer regulation time of 200 µs, resulting in an increase of 1.33 times in the regulation time.

From this analysis, it is clear that as the number of outputs in this type of converter increases, the quality of the responses deteriorates. This degradation occurs due to two main factors: the increased influence of the cross-regulation effect and the heightened frequency at which the converter must switch between outputs with different voltage levels. This not only leads to a higher ripple in the responses but also contributes to a slower regulation process and a reduction in overall efficiency.

4.2. Multiple Energizing vs Single Energizing

Several simulations were then carried out on both the Multiple Energizing and Single Energizing controls to compare them. These simulations always took into account maintaining the same conditions for both controls to obtain a fair analysis.

The final results are depicted in **Figure 12**, concluding that there is no clear superiority between the two types of control developed.



	SIMO Multiple Energizing Three Load Transients	SIMO Single Energizing Three Load Transients	SIMO Multiple Energizing Two Load Transients	SIMO Single Energizing Two Load Transients	SIMO Multiple Energizing One Load Transient	SIMO Single Energizing One Load Transient
Max Dropout Voltage (mV)	80	60	40	50	20	15
Max Over-Elevation (mV)	80	90	35	90	10	13
Cross-Regulation (mV)	X	X	32	45	12	15
Regulation Time (µs)	167	150	190	170	125	150

Figure 12: Data obtained from the different analyses applied to the results obtained from the operation of the two types of control developed, Multiple Energizing and Single Energizing.

As can be analyzed from the obtained data, it is true that in terms of cross-regulation and overshoot, the Multiple Energizing control outperforms the Single Energizing control. This outcome was expected, as with Multiple Energizing, only one output is serviced per energy period, and there are no switching events within each energy period. This significantly helps reduce the effects of cross-regulation.

Regarding overshoot, it is somewhat related to the cross-regulation effect since nearly all the results—if not all—are caused by the overshoot at the end of the load transients. These overshoots have a significant cross-regulation component. Therefore, we can conclude that the maximum overshoot values obtained are indeed connected to the cross-regulation effect.

Beyond this, in the remaining two evaluation criteria, it is possible to observe a certain dominance by the Single Energizing control. However, this dominance is not absolute.

For instance, in the case of maximum voltage drop, the SE control falls short compared to the Multiple Energizing control in the second simulation. Similarly, in terms of regulation time, Single Energizing also performs worse than Multiple Energizing in the third simulation.

From this, we can conclude that neither of the developed control systems is universally superior. However, each control method performs better in specific evaluation criteria. No absolute conclusions can be drawn, as the superiority of a control system depends on the characteristics of the simulation. A control that generally excels in one criterion may not necessarily be the best in all scenarios.

4.3. Single Inductor Multiple Output vs Multiple buck converters

To demonstrate that the SIMO converter can achieve results comparable to those of multiple independent buck converters (industry standard for multiple voltage levels), the simulation depicted in **Figure 13** was done using the Single Energizing control method.

The comparison involves two scenarios: one where only a single output is under active regulation, mimicking the behaviour of a conventional buck converter, and another where a load transient is applied simultaneously across all three outputs, reflecting the multi-output nature of the SIMO converter, however, the load transients applied to the SIMO were 10mA while for the buck converter was applied a 100mA load.

In terms of voltage drop, the SIMO exhibits a drop of approximately 7mV, whereas the buck converter reaches 15mV. For the overshoot following the load transient, both systems show similar performance, with overshoot values around 15mV.

However, in terms of response time, there's a significant difference between the two. The SIMO demonstrate a slower response (170µs) compared to the multiple buck converters (70µs), resulting in a consistent delay of around 100µs when compared to conventional buck converters.

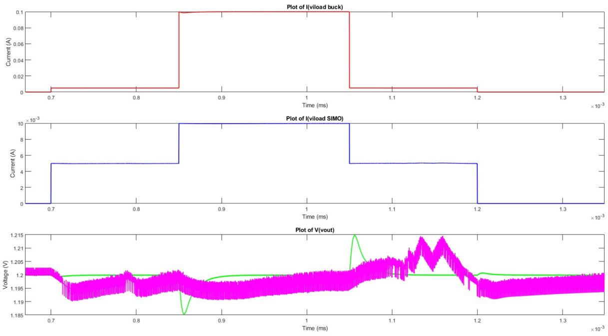


Figure 13: Simulation comparing the response of multiple buck converters and a SIMO for three simultaneous load transients, from 5 to 100mA on the conventional buck converters and 5 to 10mA on the SIMO.

The first figure shows the load transient applied on the buck converter, while the second figure shows the load transient applied on the SIMO converter. In the third figure, we have the voltage at the SIMO first output in purple and the buck converter's output in green.

Thus, the comparison highlights that while the SIMO achieves a comparable performance in terms of voltage regulation under low-load transients, its response time remains a key limitation. The final results of this analysis are summarized in **Table 2**, which contrasts the performance of multiple buck converters against the SIMO architecture.

	3 Conventional Buck Converters (100mA)	SIMO 3 output Converter (100mA)	SIMO 3 output Converter (10mA)
Max over-elevation(mV)	15	80	15
Max dropout voltage(mV)	15	65	7
Regulation Time(µs)	70	170	170

Table 2: Data obtained from the different analyses applied to the results obtained from the operation of the two types of approaches, multiple buck converters vs a SIMO converter.

From this analysis, two key conclusions can be drawn.

Firstly, regarding regulation time, a SIMO converter will never achieve response times as fast as those of a conventional buck converter. Therefore, in scenarios where rapid regulation is a critical requirement, the SIMO architecture may not be the best choice.

Secondly, for lower load current values, in the range of 10mA, the SIMO performs exceptionally well, yielding results that are comparable to or even better than those obtained from multiple individual buck converters.

In summary, the SIMO converter is a highly viable option under specific conditions: where regulation time is not a decisive factor, and the load currents involved are low, typically around 10mA as previously mentioned. When these criteria are met, the SIMO offers an efficient and practical solution for multi-output power conversion applications.

5. Conclusions

In summary, this thesis reflects the comprehensive work undertaken on SIMO converters, focusing on various aspects from applications and control methods to detailed simulations. The main objectives included integrating a third output into an existing SIDO converter, developing a new Single Energizing control model, and creating an automatic PWM/PFM switching system. Although the latter objective was not achieved due to prioritizing the SIMO implementation and control systems, significant progress was made.

The research demonstrated that both the Multiple and Single Energizing control methods are viable, but their effectiveness varies depending on the simulation scenario. As a result, it was not possible to identify one method as universally superior. The analysis also revealed trade-offs between SIMO converters and conventional buck converters. While SIMO converters may have disadvantages under certain conditions, they perform well in low-load applications (1̃0mA) and unlike multiple buck converters, they have a much more optimized silicon area.

Suggestions for future work include improving output response, conducting more in-depth studies of control methods, and moving towards real-world implementations to evaluate the practical performance of the developed systems.

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