A Low Dropout Voltage regulator with a Supply Ripple Cancellation technique

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***Abstract*—Due to their sensitive nature, analog circuits need a supply voltage bereft of voltage ripples. For this end, Low Dropout Voltage regulators (LDO) with high Power Supply Rejection (PSR) are implemented so as to feed these analog blocks.**

This work proposes a Supply Ripple Cancellation (SRC) technique LDO voltage regulator designed in a 16nm CMOS process technology. This technique consists in inverting input voltage ripple and summing it to the input once more, effectively cancelling it This LDO regulates voltages for an output of 0.9 V and for 1 mA of load current and 1pF of load capacitance.

Through simulations, the proposed LDO is shown to be competitive among state-of-the-art architectures, offering excellent PSR in low frequencies (-113 dB20).

Process, Voltage, and Temperature (PVT) corner simulations and Monte Carlo analysis are performed in order to prove the design's robustness, and that it complies with ISO 26262 standard.

***Index Terms*—CMOS, Low Dropout Voltage Regulator, LDO, Supply Ripple Cancellation, PSR**

I. Introduction

Despite the abrupt silicon shortage entailed by a worldwide pandemic, 2021 saw an increase in smartphone shipments, summing a total of up to 1.35 billion units [1]. Although that trend has slowed down recently due to an inflation rise and the many consequences of an on-going war between Russia and Ukraine [2], the demand for low-powered devices has never seen such heights.

To keep up with this ever-growing need, more and more investment has been poured into the manufacturing process industry and R&D for new and more efficient solutions (US CHIPS act and European Chips Act [3]). This includes research on device power management, a facet of evermore importance due to the increasing number of transistors on a single chip.

Voltage regulators are used in a wide array of applications, such as wearable bioelectronics, Systems-on-a-Chip, or other portable electronics. More specifically, dozens of LDO's may be found within a mobile phone to support the many different blocks it can have (camera, USB, memory...). Thus, the need for a design of such a device that minimizes power loss and improves PSR is critical.

Analog circuits usually need a fixed power supply voltage; let's say 1.2 V as an example. The conversion from V_{bat} to V_{DD} V is usually performed by a dc-dc switching converter, which results in a large ripple voltage that affects the performance of subsequent analog circuits. To replace this with only an LDO instead would also be inefficient: as its name implies, an LDO should only be used for low voltage drops, as their efficiency is close to V_{out}/V_{in}. To avoid this, the switching converter would rather take V_{bat} down to a regulated $V_{DD} = 1.4$, and then use the LDO to convert V_{DD} to $V_{\text{LDO,out}} = 1.2$, suppressing the ripple voltage coming from the switching converter.

In Figure 1, we can see a basic implementation of multiple LDO blocks in an SoC: they provide a stable voltage to each of the circuits' input, ideally bereft of noise.

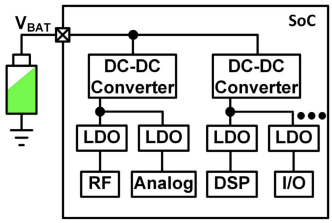

Fig. 1: Typical power management solution for an SoC. [4]

A. Objectives

The main scope of this article will be the study, design and implementation (in a simulation environment) of different variants for the same technique and also propose an alternative that presents better results for a specific parameter. The goal is to design an LDO with a high Power Supply Rejection (PSR) [1] (any variation in the power supply should reflect the least possible on the output), and small quiescent current with an Supply Ripple Cancellation (SRC) regulation technique, thus allowing for stable and clean power supply. The regulator should, of course, be able to provide enough current to the load with specified accuracy under worst-case conditions.

A regulator will be proposed so that it can correct medium to high frequency noise at around 1.5 MHz by action of the SRC technique. Large load current range, low dropout voltage and small overshoot/undershoot will also be targeted for. A bulky external capacitor will be avoided, in order to minimize circuit area and to make the LDO suitable for SoC applications.

SoCs work in sleep-mode in most time of a period; LDOs require low-power loss at no load current and fast transient

[1] Also known as Power Supply Rejection Ration (PSRR).

responses to turn ON the system from the sleep-mode immediately. Thus, the LDO should have an optimized trade-off between low power consumption, high PSR, fast transient response and compact area.

The general design of the LDO will be composed of the three following parts: an error amplifier (EA), an output stage with a power transistor, and the SRC block. Its principal parameters may be seen on table I. For this case, the input voltage V_{in} will come from the high voltage supply V_{ph}.

TABLE I: LDO specifications.

Symbol	Min.	Typ.	Max.	Units
V_{ph}	1.030	1.200	2.030	V
V_p	0.646	0.800	0.985	V
ΔV	-	300	-	mV
V_{out}	-	0.9	-	V
V_{ref}	-	0.45	-	V
t_{on}	-	< 1	-	µs
I_{ref}	-	5	-	µA
C_L	-	1	-	pF
I_L	-	1	-	mA
PSR@1.50 MHz	-	$<$ -40	-	dB

B. Document outline

The different sections in this article are outlined as follows: in the introduction, a broad contextualization of the work' theme, outline, goals, and structure are delivered; in the second section, the basic theory of the regulators, as well as their relevant parameters, are presented; next, two different papers proposing a similar or relevant technique are examined; after carefully studying the fundamentals of the LDO and the current state-of-the-art in the previous chapters, a core design is proposed, and an alternative using the same principles of the techniques is proposed; finally simulation results are presented, the work is summarized, and future work is referenced.

II. LDO OVERVIEW

LDOs are DC linear voltage regulators that provide a stable power supply voltage independent of input-voltage variations, load impedance, temperature, and time, while being able to suppress ripple voltage from the noisy input. The dropout voltage is the difference between the input and output voltages, and typical dropout voltages can range from 100 mV to 1.5 V [5].

In its most basic form, an LDO is primarily composed of a reference voltage, a means of scaling the output voltage so it can be compared with the reference (the feedback network), an Error Amplifier (EA), and a pass transistor, whose gate-source voltage is controlled by the amplifier. This can be seen on Figure 2.

V_{out} is scaled down by the feedback network, in most cases a voltage divider R_1 in series with R_2, and compared to the reference voltage V_{ref}, the latter being supplied by a bandgap reference, which is a DC voltage that has small dependency on supply, temperature, and process parameters. This bandgap reference also provides the bias current of the EA.

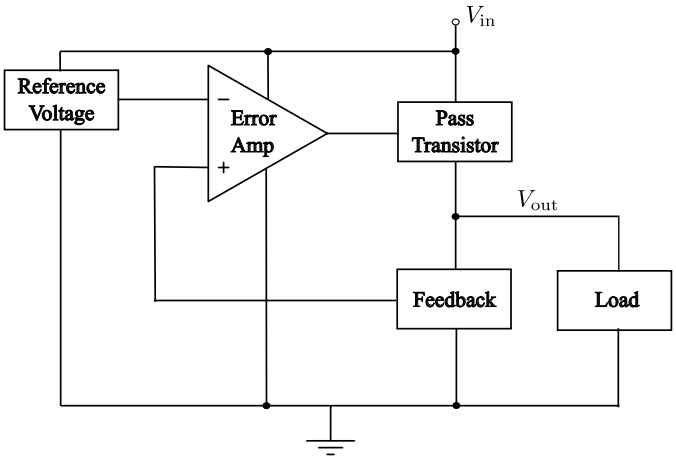

Fig. 2: Block diagram for a generic LDO.

A. Critical Parameters

Although an LDO has many relevant parameters to be taken into consideration when designing such a device, the following are those that usually serve as goalpost for any LDO's design [6]:

- **Power-supply rejection ratio**
  PSRR, or PSR, is defined as the variations in the output voltage over the input voltage $\partial V_{\mathrm{out}}/\partial V_{\mathrm{in}}$. Also known as line regulation, this is the consequence of the ripple voltages coming from the input, and it goes through two paths, the supply of EA and the pass transistor.
- **Output noise**
  The LDO itself produces this output noise $V_{n,\mathrm{out}}$, even in the absence of input noise.
- **Load regulation**
  Defined as $\partial V_{\mathrm{out}}/\partial I_L$, this effect depends on the LDO's output impedance. Transient currents from the load circuits can cause serious voltage ripples at the LDO's output. This effect is more significant at higher frequencies.
- **Power consumption and area**
  In SoCs that make use of several LDOs, these two parameters are of great importance.
- **Stability**
  As the LDO employs a feedback loop, its Phase Margin (PM) should be acceptable enough so as to prevent the degradation of the aforementioned parameters.

B. Pass Transistor

The pass transistor can serve as a controlled current source (PMOS) or as a source follower (NMOS), each implementation having its advantages and drawbacks in terms of circuit parameters and performance. It can also serve as a controlled resistor, but this leads to PSR degradation amongst other negative results, which is why it isn't a usual choice [6].

has in fact higher PSR than its PMOS counterpart, as the drain voltage variations don't affect the source voltage if channel-length modulation is neglected [6].

The transistor has practically no Miller effect; it has a quick transient response. It works almost as a common gate amplifier. As the load voltage V_{out} increases, the source's increases, V_{GS} is reduced, which pumps less output current, and in turn less output voltage. It has a "natural" negative feedback.

However, for the same dropout voltage, and since the gate voltage is $V_{\text{out}} + V_{\text{th,PPT}}$, a higher supply voltage ($> V_{ph}$) would be needed for the EA in order to keep it in a good operating point.

Thus, this structure may only be possible if an additional charge pump is placed to the EA's supply, which in turn compromises area overhead, power efficiency, and startup times. This is why, in practice, few examples of NMOS LDOs are encountered, and why it won't be a subject of analysis for this article.

An EA paired with a PMOS pass transistor operating in the saturation region form a voltage-controlled current source. The dropout voltage, which is the source-drain voltage of the transistor $|V_{DS}|$, is minimized by selecting a wide transistor [6]. In Figure 3, a basic LDO with a controlled current source can be observed.

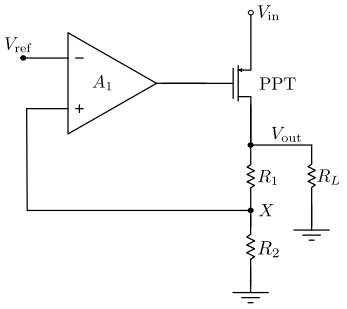

Fig. 3: Conventional LDO using a PMOS transistor, with a load resistance.

The output voltage V_{out} is equal to $V_{\text{ref}}/\beta = V_X/\beta$, where β is the resistor string ratio $R_2/(R_1 + R_2)$, and V_X is the feedback voltage coming from the voltage divider.

To determine the load and line regulation expressions, the loop gain A_{LG} must first be found. For now, it is assumed that the amp has a gain A_1 and infinite supply rejection. To find the expressions for $\partial V_{\text{out}}/\partial V_{\text{in}}$ and $\partial V_{\text{out}}/\partial I_{\text{L}}$, the feedback loop will be needed to be broken somewhere arbitrarily; this will done so at the feedback network, the point X on Figure 3. By assuming a certain small-signal resistance R_L to the load, the following equation can be obtained:

$$A_{LG} = A_1 g_{m,PPT} \left[R_L \parallel (R_1 + R_2)\right] \frac{R_2}{R_1 + R_2}. \quad (1)$$

From this, it can be stated that the amp's gain amplifies that of PPT. To find the PSR expression, a small-signal model is needed to be built, as in Figure 4. From here, it is observed that the gate-source voltage of the pass transistor is:

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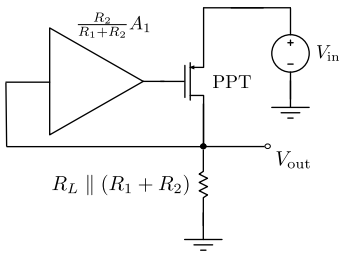


Fig. 4: A model for finding PSR. [6]

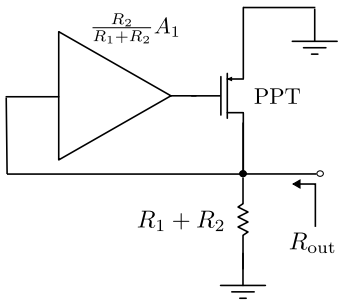


Fig. 5: A model for finding the output resistance. [6]

needed to be built, as in Figure 4. From here, it is observed that the gate-source voltage of the pass transistor is:

$$V_{GS,PPT} = \frac{A_1 R_2}{R_1 + R_2} V_{out} - V_{in}, \quad (2)$$

and so the small-signal current flowing through the pass transistor is:

$$I_{D,PPT} = g_{m,PPT} \left(\frac{A_1 R_2}{R_1 + R_2} V_{\text{out}} - V_{\text{in}} \right). \quad (3)$$

This current then flows into the equivalence output resistance $R_L \parallel (R_1 + R_2)$, and so:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{m,PPT} \left[R_L \parallel (R_1 + R_2)\right]}{1 + A_1 g_{m,PPT} \left[R_L \parallel (R_1 + R_2)\right] \frac{R_2}{R_1+R_2}} \quad (4)$$

$$= \frac{g_{m,PPT} \left[R_L \parallel (R_1 + R_2)\right]}{1 + A_{LG}}. \quad (5)$$

As $A_{LG} >> 1$:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{A_1}, \quad (6)$$

which means that the line regulation can be enhanced by increasing the amp's gain A_1.

It can also seen that load regulation $\partial V_{\text{out}}/\partial I_L$ is the output impedance R_{out} of the LDO. This means that drawing the circuit as in Figure 5:

$$R_{\text{out}} = \frac{1}{g_{m,PPT} A_1 \frac{R_2}{R_1+R_2}} \parallel (R_1 + R_2). \quad (7)$$

As the first term of the parallel combination is much inferior to the second:

$$R_{\text{out}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{g_{m,PPT} A_1}. \tag{8}$$

So as it was for the line regulation, for the load regulation high A_1 will be needed.

The PMOS pass transistor has an output resistance $r_{o,\text{PPT}}$, which allows V_{in} to pass to V_{out} and degenerate the PSR. This degradation worsens if the transistor passes from saturation to the linear region, which is one of the reasons why it needs to be guaranteed that the output transistor has enough saturation margin.

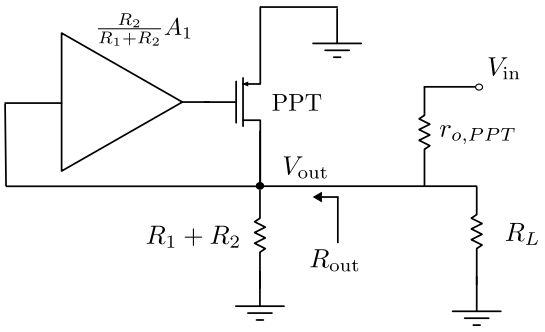


Fig. 6: The effect of transistor output resistance on PSR. [6]

From Figure 6, this can be seen as a simple voltage division between $r_{o,\text{PPT}}$ and R_{out}:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_{\text{out}}}{r_{o,\text{PPT}} + R_{\text{out}}} \tag{9}$$

$$= \frac{1 + R_1/R_2}{g_{m,PPT} r_{o,\text{PPT}} A_1 + 1 + R_1/R_2}, \tag{10}$$

assuming $R_L >> R_{\text{out}}$. As 9 is much lower than 6 (by a factor of $g_{m,PPT} r_{o,\text{PPT}}$), the former equation can be discarded, but only when the transistor works in saturation, as previously mentioned.

If ripples exist at high frequencies at either input or output, then the equations (6) and (8) need to be revisited. This is mainly because the amp will have at least one pole, rendering:

$$A_1 \rightarrow \frac{A_0}{1 + \frac{s}{\omega_0}}, \tag{11}$$

and so the previous PSR equation changes to:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{A_0} \left(1 + \frac{s}{\omega_0}\right), \tag{12}$$

while the output impedance turns into:

$$R_{\text{out}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{g_{m,PPT} A_0} \left(1 + \frac{s}{\omega_0}\right). \tag{13}$$

With this in mind, the LDO's frequency response to supply noise (PSR) and output impedance can be sketched, as in Figures 7 and 6: beyond ω_0, PSR and load regulation degrade. This is where this work's proposed design should develop on.

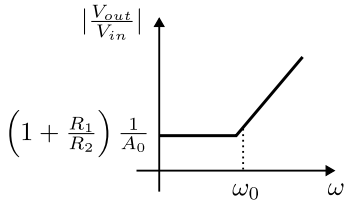


Fig. 7: LDO PSR frequency response for a one-pole amp.

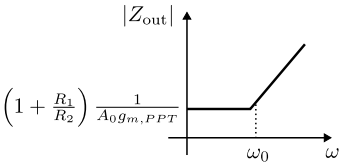


Fig. 8: LDO output impedance frequency response for a one-pole amp.

C. Error Amplifier

For the EA, as we're connecting the output to a PMOS gate, we shall implement a single-ended Operational Transconductance Amplifier (OTA): these blocks are meant to drive capacitive or high impedance loads (unlike opamps, which drive resistive or low impedance loads).

For a single-stage OTA, there are many possible architectures: among these, the most simple and most familiar to us is a differential pair with an active load. However, this topology doesn't offer nearly enough gain needed for this context.

Another possibility would be to use cascode topologies: among these, the telescopic and folded-cascode architectures are a possibility. Although the voltage headroom is very low due to the stacked transistors (5 in the telescopic and 4 in the folded-cascode), these usually offer high gain for a given bandwidth.

As can be seen on table II, the many amp topologies offer different tradeoffs.

TABLE II: Comparison of performance for various amps. [7]

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-boosted	High	Medium	Medium	High	Medium

As for an LDO, the key component is a wide bandwidth for a given gain [6], which is why a cascode topology will be selected. As a high supply voltage is on the table, the voltage headroom will not be so easily exceeded. A one-stage topology also avoids the compensation issues that appear in two-stage configurations. A telescopic architecture would nevertheless be too close for even a high supply voltage (5 stacked transistors). Input and output common-mode (CM) levels can also be the same without limiting output swings, and they have wider input CM range. And so, it is the low voltage folded-cascode that will be implemented for this work, as seen on Figure 9,

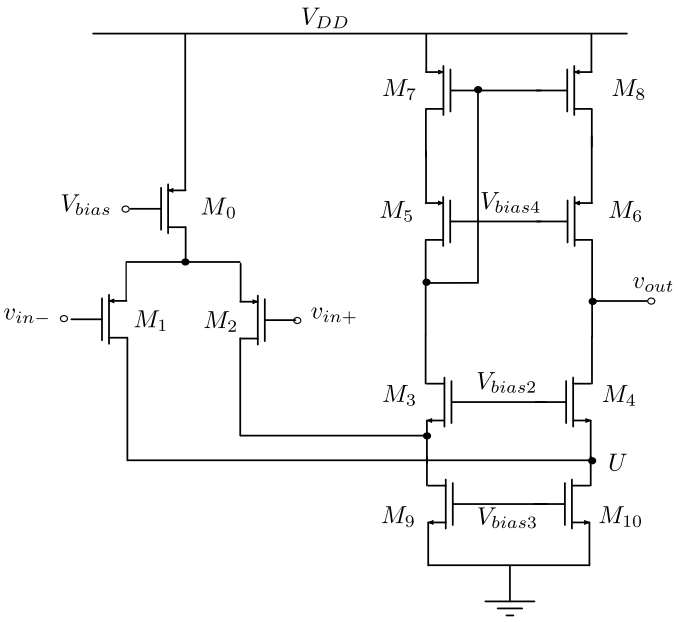


Fig. 9: Schematic for a single-output low voltage folded cascode amp.

The first matter to evaluate in this amp is the current biasing: to put it simply, the current that flows in M_9 will be the same that flows through M_7 and M_8, and double of that for each remaining transistor: $I_0 = 2I_{1,2} = 2I_{3,4,5,6,7,8} = I_{9,10}$.

To simplify matters, symmetry will be assumed, with $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$, $M_7 = M_8$, and $M_9 = M_{10}$.

Its input impedance $R_{i,EA}$ being obviously very large (so much so that $R_{id} = \infty$ can be considered), the analysis moves to its output impedance.

It can be easily seen that $R_{o,EA}$ will be the parallel of the two nets branching from the output. From the branch coming from M_1 to the node U, the equivalent resistance would be $r_{o1} \parallel R_{o10}$; this in turn would be multiplied to $g_{m4}r_{o4}$. On the upper output branch, it is simply $g_{m6}r_{o6}r_{o8}$. The following equation can be formulated:

$$R_{o,EA} = [g_{m4}r_{o4}\,(r_{o1} \parallel r_{o10})] \parallel [g_{m6}r_{o6}r_{o8}] \tag{14}$$

And so, the total voltage gain of this structure will be:

$$A_{EA} = g_{m1}R_{o,EA} \tag{15}$$

The following dominant pole defines the GBW product:

$$\text{GBW} = \frac{g_{m1}}{2\pi C_L} \tag{16}$$

and the second pole

$$f_{nd} = \frac{g_{m3}}{2\pi C_n} \tag{17}$$

where

$$C_n \approx C_{GS3} + C_{DB2} + C_{DB9} \approx 3C_{GS3} \tag{18}$$

This amp can have high GBW, which will mater for this work's case, as maximum gain and bandwidth are needed in order to increase overall PSR.

It has the drawback of necessitating more transistors than other amp topologies, which undermines voltage headroom and power consumption. These points will be taken into consideration when designing the amplifier.

III. State-of-the-art

The study of LDOs is the core of many papers; it isn't hard to find different applications and techniques regarding this subject. In this chapter, a broad view is taken at selected state-of-the-art LDOs from the last years and compare their overall performance and parameters. These papers were selected for implementing some form of supply ripple cancellation on their architecture and using a PMOS pass transistor. Here, two alternative designs are briefly explored; the basis of this work's SRC design is then developed in the next section.

A. Body Ripple Injector

The LDO [8] is an external capacitorless regulator that provides high PSR at all frequencies. Not using an external capacitor can be a great advantage due to the sheer size it can occupy in circuit area. To compensate for the instability of a design with no capacitor, the electronic designer places a dominant pole at the gate of the pass transistor. Because of this design choice, the LDO must also make use of an adaptive supply-ripple cancellation technique (ASRC) to suppress the PSR hump of conventional gate-pole-dominant LDOs: this allows to cancel supply ripples through g_{ds} as well as through g_m of the transistor. High PSR is firmly maintained thanks to the ASRC continuously optimizing the magnitude of injecting ripples, despite PVT variations as well as during changes of I_L and V_{DO}. A block diagram of this circuit can be seen in Figure 10.

This paper proposes injecting the supply ripple to the pass transistor's body terminal through a Body-Ripple Injector (BRI). The g_{ds}-to-g_{mb} sensor (GTGS) determines the necessary magnitude needed for v_{SRC} to compensate for the supply ripple, hence the 'adaptive' on the paper's title 'Adaptive Supply Ripple Cancellation'.

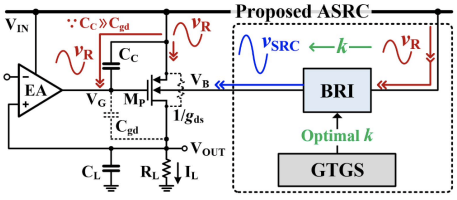


Fig. 10: Conceptual block diagram of the LDO with ASRC. [8]

B. Reference buffer

In short, the LDO [9] makes use of a buffer for the reference voltage which reverses the supply voltage ripple. Summed

with the normal-phase PSR from the EA, this allows for great supply ripple subtraction on DC (-59.8 dB) and frequencies up to 1 MHz.

The buffer has two symmetric branches, and in each one there is a supply ripple amplifier (M_{R1} and M_{R2}; M_{L1} and M_{L2}). Its output is connected to the gate of a transistor (M_{R3}; M_{L3}) which will generate a small-signal current with negative phase (when the design is such that $g_{m,R2} > g_{m,R1}$; $g_{m,L2} > g_{m,L1}$).

The DC PSR of this buffer is thus defined by:

$$PSR_{BUF} = -\frac{(g_{m,R3} + g_{m,L3})\left(\frac{g_{m,R_2}}{g_{m,R_1}} - 1\right)}{2g_{m,F1}g_{m,F3}r_{ds,F1}}. \tag{19}$$

The LDO PSR is at its peak when:

$$PSR_{BUF} = -\frac{1}{g_{m,P}g_{m,A1}R_oR_{o,EA}} \tag{20}$$

Furthermore, the buffer relies on adaptive biasing currents so that it may hold high PSR on a wide load current range.

Moreover, it employs a common-gate feedback (CGFB) loop, which enhances the DC gain of the EA. It also implements a pole-tracking compensation (PTC) technique to maintain a high PM over a wide load current range. A current-controlled nulling resistor tracks the operating points of the power transistor through linear, saturation and even subthreshold regions.

A schematic of this circuit can be seen in Figure 11. The simulated PSR results from the paper can be seen in Figure 12: here, we can see how the buffer effectively enhances the PSR, practically doubling it.

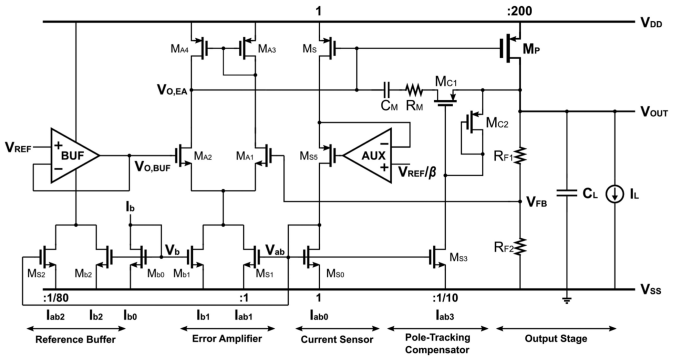


Fig. 11: LDO with phase-reversed PSR buffer and PTC. [9]

C. Comparisons

The first LDO presents high PSR at high frequencies, whereas the second shows admirable PSR but with low quiescent current I_q and highest load regulation. For this work, the second state-of-the-art LDO will be implemented and elaborated on the following section.

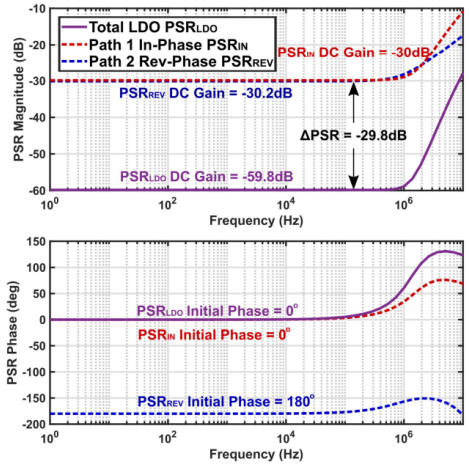


Fig. 12: Simulated PSR frequency response for LDO and the two opposite PSR paths with 20 mA load current. [9]

IV. Supply-Ripple Cancellation LDO

The SRC technique is based on suppressing as much as possible input ripples by replicating it, inverting its phase, and summing it to the original ripple.

Going back to eq. (5):

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{m,PPT}\left[R_L \parallel (R_1 + R_2)\right]}{1 + A_{LG}} \tag{21}$$

$$= \frac{K}{1 + A_{LG}} \tag{22}$$

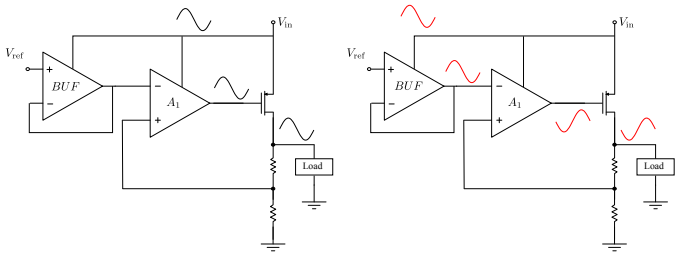
For this technique, it can be gathered that a K_{psr} factor is needed so that multiplied with (21), PSR is improved as much as possible. To make this possible, a secondary path for the ripple is necessary, as seen from the previous state-of-the-art LDOs; in this case, a buffer will be placed on the reference voltage path, in which the ripple will be injected and then reversed.

Considering an example where there's a small increase on the supply voltage, this forces an increase on $V_{SG,PPT}$ in the original PSR path, which results in an increase in output current, and so in output voltage as well. The proposed reference buffer takes this supply variation and inverts its phase, then injects it into the reference voltage. This causes a small decrease on the buffer output; the amp has to compensate this decrease on the non-inverting input, and so in turn decreases voltage on the output, compensating for the original ripple path. Another way to see this is as the buffer output decreases, the amp output increases, which in turn decreases the pass transistor source-gate voltage, and compensates the increase at the output. This is illustrated on Figure 13.

Considering the two paths, the total PSR in dB is defined as:

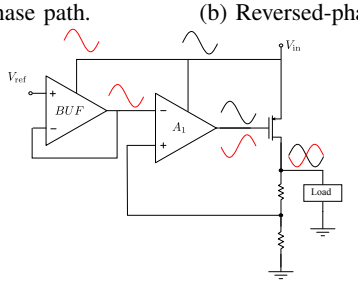
$$PSR = PSR_{in} + PSR_{rev} \tag{23}$$

where PSR_{in} is the ripple in phase with the input ripple, and PSR_{rev} is the reversed-phase ripple, with



(a) In-phase path.

(b) Reversed-phase PSR path.



(c) The two PSR paths summed together.

Fig. 13: Diagram of the two opposite-phase PSR paths in the proposed LDO with the reference buffer.

$$PSR_{rev} = PSR_{buf}(s)\frac{A_{LG}(s)/\beta}{1 + A_{LG}(s)} \tag{24}$$

If:

$$PSR_{DC6} = \frac{K \cdot K_{psr}}{1 + A_{LG}} \tag{25}$$

then:

$$K_{psr} = 1 + A_0 g_{m,PPT}\left[R_L \parallel (R_1 + R_2)\right] \cdot PSR_{buf,DC} \tag{26}$$

The overall maximum PSR in DC is achieved if $K \cdot K_{psr} = 0$, or:

$$\frac{\partial V_{\text{ref}}}{\partial V_{ph}} = \text{PSR}^{\text{max}}_{\text{BUF,DC}} \tag{27}$$

where

$$\text{PSR}^{\text{max}}_{\text{BUF,DC}} = -\frac{1}{A_{EA} g_{m,PPT}\left[R_L \parallel (R_1 + R_2)\right]}. \tag{28}$$

This buffer is implemented as illustrated on Figure 14. It's constituted of a simple PMOS input differential pair $M_{1,2,3,4}$ with its bias current supplied by M_b. This buffer takes the reference voltage at the gate voltage of M_1 and delivers it at the gate voltage of M_2.

M_5 and M_6 form a supply ripple amplifier with the supply voltage as input and V_{G7} as output. M_7 takes these variations and forms a small-signal current when $g_{m6} > g_{m5}$. This current will have an inverted phase compared to the input ripple, and is injected into the differential pair, where it flows to the buffer output V_{buf} and to the EA's inverting input.

M_5 and M_6 are biased from the bandgap reference voltage and are in saturation.

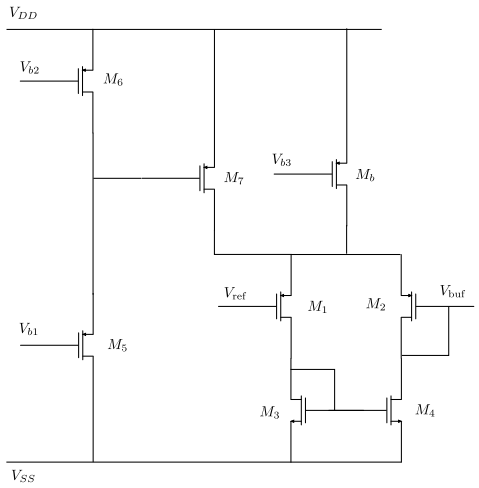


Fig. 14: Reference buffer schematic.

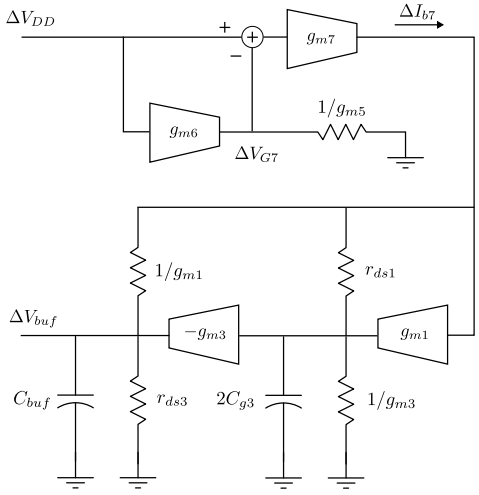


Fig. 15: Small-signal model of the reference buffer

Analysing Figure 15, the following PSR analysis are obtained:

$$PSR_{bufDC} = -\frac{g_{m7}\left(g_{m6}/g_{m5} - 1\right)}{2 g_{m1} g_{m3} r_{ds1}} \tag{29}$$

$$p_{1,buf} \approx -\frac{g_{m1}}{C_{g,A1}} \tag{30}$$

$$p_{2,buf} \approx -\frac{g_{m3}}{2C_{g3}} \tag{31}$$

$$z_{1,buf} \approx -\frac{1}{r_{o,buf} C_{o,buf}}, \tag{32}$$

where

$$\frac{g_{m6}}{g_{m5}} > 1 \tag{33}$$

and $r_{o,buf}$ and $C_{o,buf}$ are the output resistance and capacitance of the buffer.

V. Results

The main operating point simulation results in the typical corner for the SRC LDO are shown in Table III.

TABLE III: Some OP measurements from LDO simulations.

Parameter	Value
V_{fb}	450.001 mV
V_{out}	900.002 mV
I_q	264.047 µA
I_L	1 mA

After implementing the reference buffer, the overall quiescent current suffered an increase of 56 µA relative to the buffer-less LDO.

A. DC Behavior

1) Dropout voltage: A parametric sweep over the input voltage was performed on the typical corner, as seen on Figure 16 so as to establish the necessary V_{in} for this LDO to start correctly regulating for $V_{\text{out}} = 0.9$. From this analysis, it can seen that the minimum V_{in} is 946 mV, resulting in a minimum dropout voltage ΔV of 46 mV.

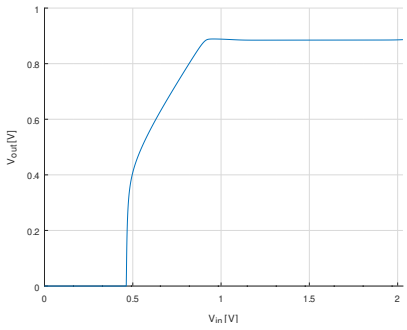


Fig. 16: Dropout voltage simulation.

2) Line regulation: A line regulation analysis can also be extracted from this result if analysed for the input range 1 V to 1.4 V, where a regulation delta of around 0.12mV is obtained. This can also be measured in voltage percentage by dividing this value by the nominal output voltage, giving a line regulation of $0.01\%/\text{V}$.

3) Load regulation: The simulation for the load regulation was performed by running a parametric sweep of the load current from 0 mA to 1 mA, as can be seen on Figure 17, for a V_{in} of 1.2 V. From this analysis can be defined the load regulation delta, set around 1.4 mV, or $0.16\%/\text{V}$.

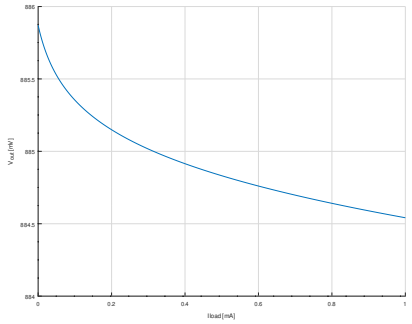


Fig. 17: Load regulation simulation results.

4) Efficiency: With minimum input voltage of $V_{ph} = 946$ mV for a $V_{\text{out}} = 0.9$, and $I_q = 264.047$ µA, and $I_L = 1$ mA, then the LDO's efficiency can be computed as follows:

$$\eta = \frac{1 \times 10^{-3} \times 0.9}{(1 \times 10^{-3} + 264.047 \times 10^{-6}), 0.946} = 75.26\%, \tag{34}$$

which is around 20% below the maximum efficiency possible for this LDO ($V_{\text{out}}/V_{\text{in}} = 0.9/0.947 = 95.04\%$).

In the following subsections, simulations in select PVT corners were run.

B. Transient Behaviour

1) Startup: The following simulation quantifies the power up of the LDO. As seen on Figure 18, for an error band of 2%, the measured settling time is about $t_{\text{on}} = 4.74$ ns.

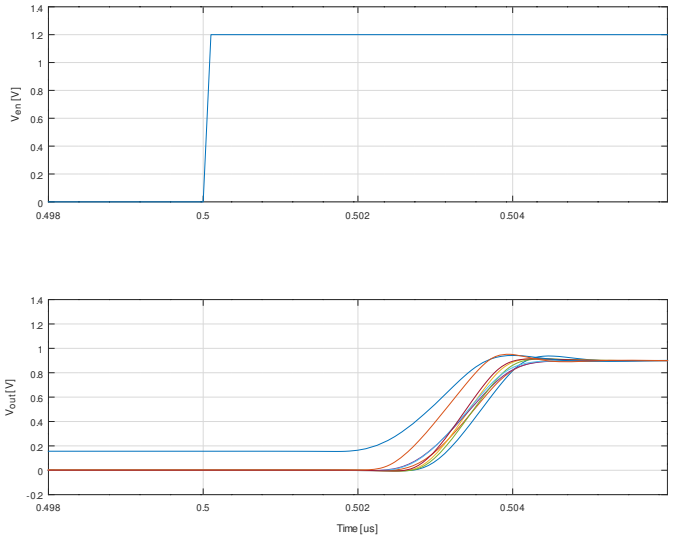


Fig. 18: Startup PVT simulation results.

2) Load transient: The load transient behaviour was simulated with load current variations from 0 to 1 mA with rise and fall times of 1 ns. This is represented in Figure 19, which shows an overshoot and undershoot of 0.18 and 0.21 V respectively.

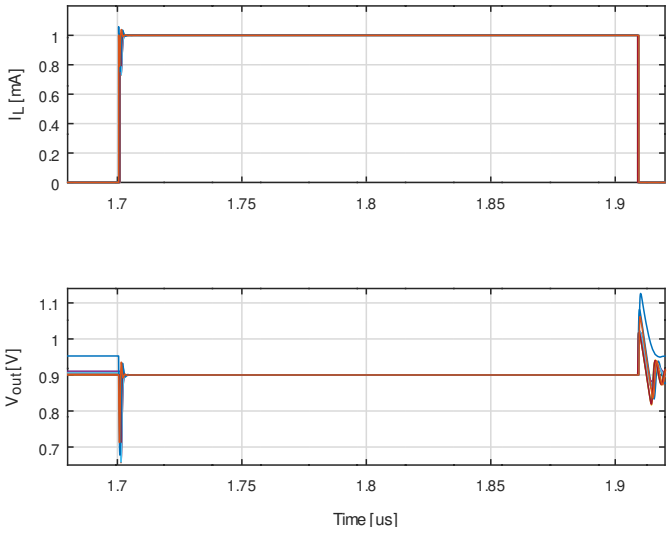


Fig. 19: Load transient PVT simulation results.

3) Line transient: The line transient behaviour was simulated with input variations of $+/-10\%V_{ph}$, with rise and fall times of 1 ns. From Figure 20, the overshoot and undershoots can be extracted, which are 31 mV and 34 mV respectively. There is a failed corner for which the LDO could not properly regulate for an increase in supply voltage.

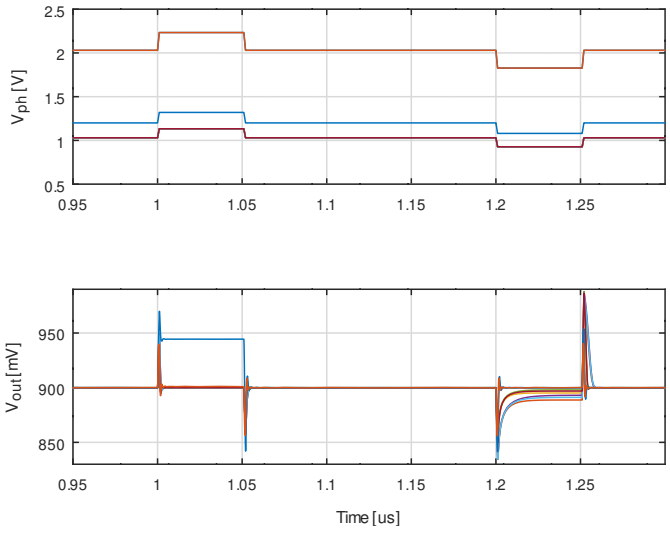


Fig. 20: Line transient PVT simulation results.

4) FoM: From Rincon-Mora's equation [10] and the previous results, the LDO's FoM can be extracted:

$$\text{FoM} = \sqrt{\frac{2 \times 1 \times 10^{-12} \times 21 \times 10^{-3}}{0.764 \times 10^{-3}/0.4 \times 10^{-9}}} \frac{264.047 \times 10^{-6}}{1 \times 10{-}3} \tag{35}$$

$$\approx 39.16 \text{ ps} \tag{36}$$

C. AC Analysis

As with the basic design for the LDO, an AC and PSR analysis was performed, presented on Figures 21 and 22.

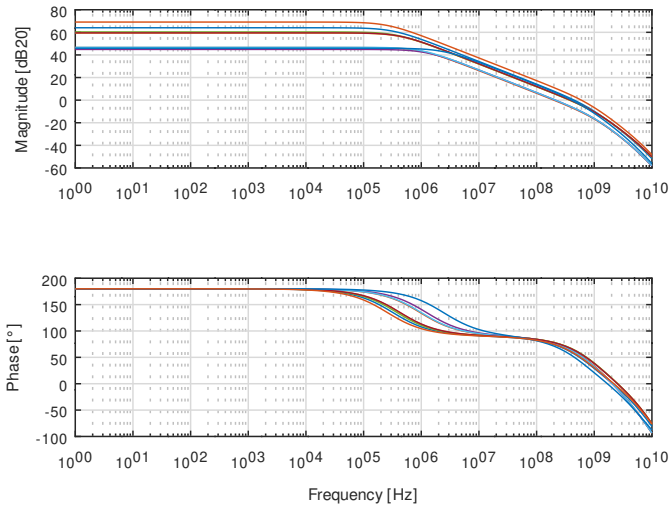


Fig. 21: AC PVT simulation results.

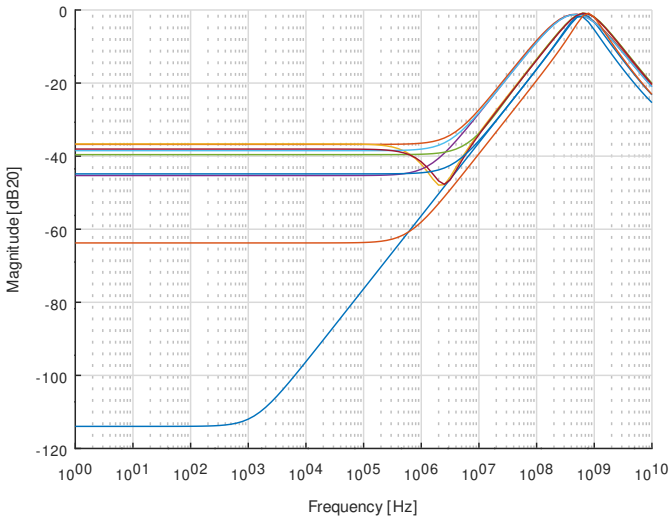


Fig. 22: PSR PVT simulation results.

From these figures, it can be extracted that the amp has, in the typical corner, an open loop gain of 61.3 dB20, bandwidth 321 kHz, and phase margin of 56°. The PSR is substantially increased with the reference buffer: in the typical corner, at DC, it is around -113 dB20, and -55 at 1.5 MHz.

In Figure 22, some variation between corners can be seen, mostly explained by the fact that the voltage bias for $M_{5,6}$ in the reference buffer was supplied by an ideal voltage source, which means it wouldn't properly track the necessary voltage to bias these PMOS as their supply voltages vary. This should be resolved by replacing the ideal voltage sources by a bias voltage generator [11].

D. Monte Carlo Analysis

Monte Carlo analysis was performed on the worst PVT corners for each analysis. In order to comply with ISO26262 safety and reliability standards, the measured device should have a maximum of 1000 *dppm* [12], (defective parts per million), which corresponds to a 3.09 sigma deviation. To cover a yield percentage of 99.997%, or 3.4 dppm, Monte Carlo simulations were run with a 4.5 sigma for 330 iterations.

As with the PVT simulations, there are large standard deviations on the PSR MC analyses, in Figure 23. As it was for PVT, this is explained by the fact that the bias voltage is not properly tracked for the $M_{5,6}$ transistors in the reference buffer. Nevertheless, large medians for PSR in low-to-medium frequencies can be verified for what is the worst PVT corner.

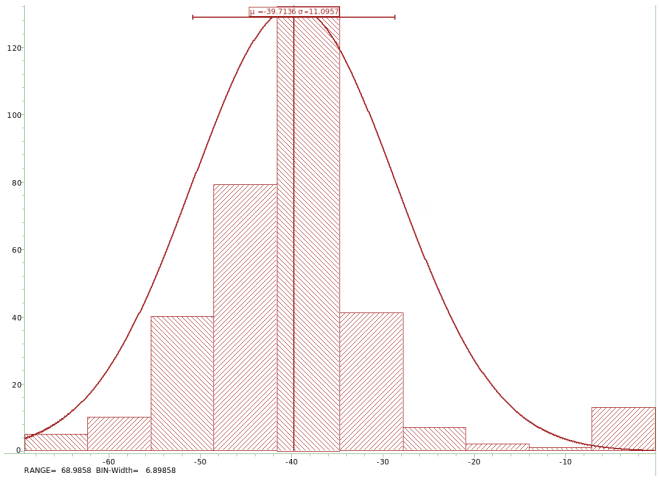


Fig. 23: Worst case PSR Monte Carlo simulation results at 1MHz.

VI. Circuit Validation and Datasheet

From the previous simulation results, a datasheet of the proposed Supply Ripple Cancellation LDO is presented on Table IV.

TABLE IV: Datasheet of the electrical characteristics for the SRC LDO.

Symbol	Min.	Typ.	Max.	Units
V_{in}	0.946	1.2	2	V
V_p	646	800	985	mV
ΔV	0.046	0.3	1.1	V
V_{out}	899.88	900	902.11	mV
V_{ref}	-	0.45	-	V
t_{on}	-	4.74	-	ns
I_q	-	264.047	-	µA
Load reg.	-	1.4	-	mV/mA
PSR@1.5MHz	-37.8	-55.4	-58.6	dB20
Efficiency	-	75.26	-	%
FoM	-	39.16	-	ps

VII. Conclusion

This work introduced the concept of an LDO, its most relevant parameters, and alternative LDO topologies, highlighting advantages and disadvantages for each design.

After careful research and consideration on state-of-the-art LDOs, a Supply Ripple Cancellation technique was applied, in which the supply ripple is sensed, inverted, and finally summed to the original supply ripple. PSR cancellation is achieved with the tradeoff of PSR bandwidth. PVT results in PSR, overshoot, and undershoot line transients were presented.

VIII. Future Work

To further build upon this design, current optimization could be applied in order to increase power efficiency. A thorough PVT/MC analysis should be realized to shave off outlier cases. To further improve the LDO's performance, an impedance attenuation technique buffer [13] could be implemented, so as to push the pole at the gate of the PPT beyond the UGF of the loop, increasing PSR bandwidth.

Acknowledgment

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