Injection-locked Ring Oscillator

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***Abstract*—Many electronic circuits rely on an oscillator for different applications. CMOS ring oscillators are a natural choice when it comes to low power consumption, small die area, and ease of implementation, although lacking in some performance metrics such as noise or quality factor, which leads the designers to resort to PLLs with crystal and LC oscillators. This work builds upon a known injection lock technique to couple two ring oscillators with a non-multiple number of phases. This technique consists of stacking two ring oscillators reusing the current of the first to drive the second. A layout of the circuit is designed using oscillators with seven and nine phases working in the MHz range, with a 3 dBc/Hz improvement to phase noise when coupled compared to the free-running oscillators. The output frequencies are precisely related by a fractional constant, which means that this method can be used as a fractional frequency synthesizer.**

***Index Terms*—Ring oscillator, phase noise, injection lock, frequency synthesizer.**

I. Introduction

Oscillators are circuits capable of generating a periodic signal. Their use in electronics is widespread, with several applications such as clock generating circuits for synchronous systems or as frequency synthesizers used in radio frequency (RF) and audio.

The pursuit of small area and low power systems favors the use of fully integrated circuits. For that, ring oscillators (RO) are a feasible choice in detriment of relaxation or LC oscillators, since they are easy to implement, occupy a small die area, and can work with low supply voltages.

In its basic form, a ring oscillator uses an odd number of phases (N) implemented with CMOS inverters (Fig. 1), and its oscillation frequency is given by

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_d} \tag{1}$$

where t_d is the delay of each stage. For oscillators with a rail-to-rail output voltage swing, the average power consumption can be estimated using [1]

$$P = I_{avg} \cdot V_{DD} = N \cdot f_{osc} \cdot C_l \cdot {V_{DD}}^2 \tag{2}$$

where C_l denotes the output switching capacitance.

For applications that demand a precise frequency or ratio of frequencies, some kind of coupling mechanism is used to ensure synchronization. This is achieved using injection lock methods such as a phase locked loop (PLL) from which a fractional frequency synthesizer can be obtained [5] or using current-based injection lock for low-frequency applications [3], to generate output signals with frequencies related by an integer number [2], or to obtain signals in antiphase [6]. In all cases, phase noise (PN) also improves due to synchronization.

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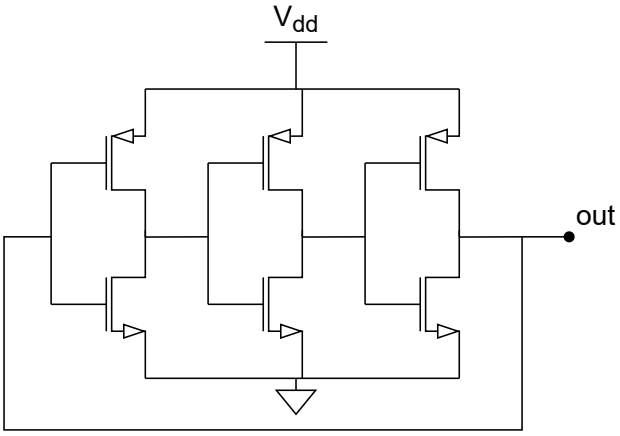

Fig. 1. Basic CMOS ring oscillator.

The stacking of oscillators described in [2], [3], and [6] is a passive coupling mechanism that relies on the supply current signature to achieve the lock. By using identical inverters, the supply voltage is divided equally between each oscillator, while the current of the first oscillator is reused to drive the second one.

A CMOS inverter has no static power consumption since either the NMOS or the PMOS transistor is in the cut-off region, however, during the transition of logic state both transistors are in saturation during a small interval, causing a current spike. In a ring oscillator, inverters are constantly switched, resulting in a periodic waveform of the supply current. Due to the inverter time delay, there are only a few inverters in transition at the same time, which means that the current signature of the oscillators is independent of the number of phases.

When two oscillators are stacked, the switching of an inverter in the top RO permits the current to pass through it which in turn allows for the switching of an inverter in the bottom RO, and it is this synchronism that locks the two frequencies. This method is detailed in [7], stacking oscillators with the same number of phases or a numbers that are multiple

of each other. In this case, the inverters in the top RO are always synchronized with the same inverters in the bottom RO, and the two oscillator signals share some harmonics between them. However, since the locking of the oscillators relies solely on the injection of current and not on their output voltages, the purpose of this work is to demonstrate that it is possible to use this method to achieve the lock of ROs with a non-multiple number of phases. The main factor here is having one inverter from the top RO and one from the bottom RO switching at the same time, and it is not important if the top inverters are synchronized with their respective bottom inverters or if this synchronization is scrambled. The resulting output frequencies of the oscillators will then be precisely related by a fractional constant.

In this paper, two ROs with a non-multiple number of phases are connected in stacked topology. The coupling of the oscillators results in an improvement in phase noise while the output frequencies are related by a fractional constant. The circuit design is detailed in Section II. In Section III, the results of the simulations are presented including power consumption, operating frequency, and phase noise, with a visualization of the oscillator's output. Section IV shows the new results taking into consideration the changes and effects added by the layout of the circuit. Finally, in Section V conclusions are drawn and insights are given about future work.

II. Detailed Circuit

The ring oscillators are implemented using TSMC 65nm technology, with basic CMOS inverters. With the purpose of designing a circuit for proof of concept and forthcoming manufacturing, the intended working frequency is in the MHz range given the limited bandwidth of oscilloscope probes. For that, the transistors have large dimensions employing $W_p = 10\ \mu m$, $W_n = 3\ \mu m$ and $L_{p,n} = 1\ \mu m$. Large transistors also have the benefit of being less impacted by process and mismatch effects that can introduce significant differences to the circuit causing the loss of coupling [3]. The difference in widths between the PMOS and NMOS ensures a symmetrical voltage transfer characteristic. An important aspect is to guarantee the synchronism between the inverters of the top and bottom ROs when they are stacked. To ensure this, each stage needs to have enough settling time before their input signal starts switching again. This delay is achieved by adding more stages to the loop, thus oscillators with seven and nine phases are used.

The oscillators are simulated individually with a supply voltage of 600 mV while the stacked oscillators share a supply voltage of 1.2 V, each of them operating with 600 mV as seen in Fig. 2.

III. Results

The simulation results are presented in Table I. The FOM used is the one shown in (3).

$$FOM = \mathcal{L}_{meas}(\Delta f) + 10\log\left(\left(\frac{\Delta f}{f}\right)^2 \frac{P_{DC}}{P_{ref}}\right) \quad (3)$$

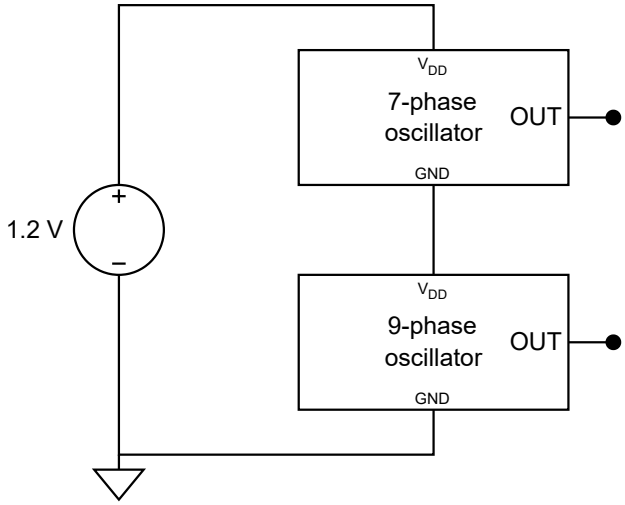

Fig. 2. Injection-locked ring oscillators in stacked topology.

The first two lines in the table regard the stand-alone oscillators and it is first noticed that power consumption remains constant while the number of phases increases. As explained before, this effect is due to the inverter time delay since there is only a small number of inverters in transition at the same time which keeps the average current value constant. In fact, a discrete Fourier transform (DFT) of the supply current of both oscillators is shown in Fig. 3, where we can see that their frequency specters are identical, and it is this phenomenon that allows the locking through current.

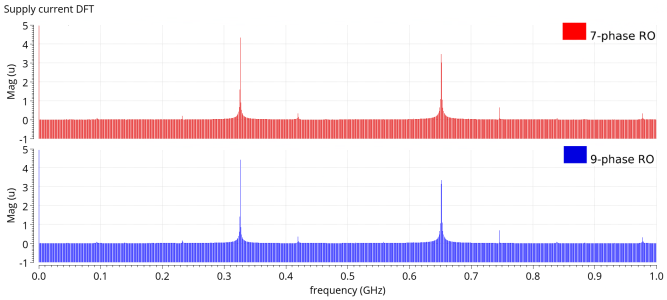

Fig. 3. DFT of the supply current of both stand-alone oscillators.

With respect to the stack of oscillators with a non-multiple number of phases, generically, consider two ring oscillators, one with N inverters and a second one with M inverters, and M is greater than N. If the oscillators are locked, it is expected that their frequencies are related by a factor of M/N, meaning that $f_N = \frac{M}{N} f_M$. This implies that, in the interval of time that takes for the faster oscillator to go through M cycles, the slower will make N cycles. This is precisely what happens in the last simulation. The coupling of the 7-phase oscillator with the 9-phase one achieves the lock. Their frequencies are related through $f_7 = \frac{9}{7} f_9$ like a fractional frequency synthesizer, and it obtains the same 3 dBc/Hz improvement in phase noise compared to their free-running counterparts when stacking oscillators with a multiple number of phases as reported in

TABLE I
RESULTS FOR STAND-ALONE AND INJECTION-LOCKED OSCILLATORS.

Phase Number	Supply Voltage [V]	Average Current [A]	Power [W]	Frequency [MHz]	PN [dBc/Hz]		FOM
					@ 100 kHz	@ 1 MHz	@ 100 kHz
7	0.6	27.1	16.3	46.7	-94.8	-115.3	-166.1
9	0.6	27.1	16.3	36.3	-97.1	-117.5	-166.2
7	1.2	27.2	32.6	46.5	-97.9	-118.0	-166.1
9				36.2	-100.0	-120.1	-166.0

[2]. In Fig. 4 it is possible to observe their time behavior. The top oscillator has a voltage swing between 0.6 V and 1.2 V, while the bottom one oscillates between 0 V and 0.6 V. At the start of the plot the oscillators have their descending flanks aligned. After this, the faster 7-phase RO goes through nine cycles while the 9-phase RO goes through seven and their flanks realign. This pattern repeats through time.

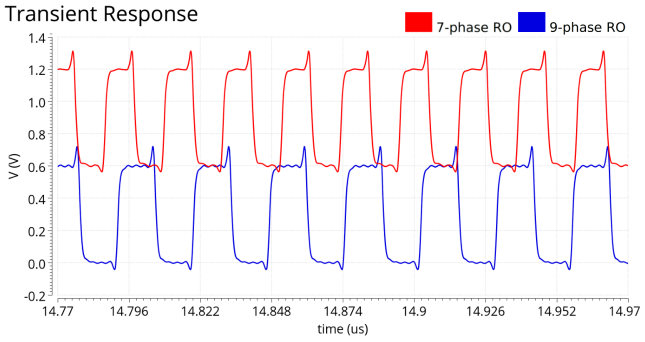

Fig. 4. Transient response of the stacked oscillators with 7 and 9 phases.

Although the average current value is very close, the power consumption is double compared to a stand-alone oscillator since the supply voltage also doubled. This, together with the phase noise improvement leads to no significant difference in the FOM.

IV. POST-LAYOUT RESULTS

To further add to this work, a layout of the circuit is designed for future manufacturing with the intent of obtaining the same results in a physical chip. It is thus necessary to add buffers to observe the oscillator's output given the high capacitance of oscilloscope probes.

The buffer consists of a chain of inverters that get progressively larger by a factor of 2. The addition of the buffer to the output node significantly increases its capacitance, which disrupts the coupling mechanism. To solve this problem, the first two stages of the buffer are added to the output of all the oscillator's stages, as seen in Fig. 5. The output of the dummy buffers is left unconnected. This way, the load capacitance of each stage is balanced.

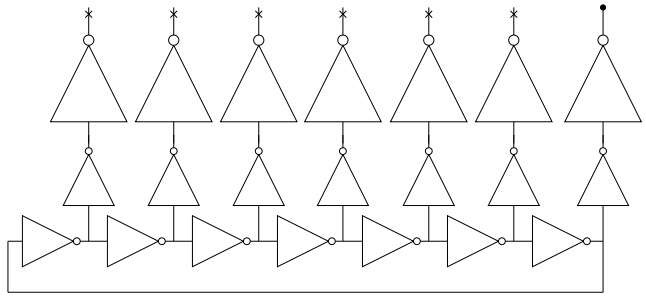

Fig. 5. 7-phase RO with dummy buffers.

The layout includes a stack of the 7-phase and 9-phase ring oscillators as well as their stand-alone counterparts for comparison. The stacked circuit is shown in Fig. 6, where the oscillators are placed in close proximity to reduce possible mismatches. These and the dummy buffers are placed inside a guard ring, that has a wider active area toward the output buffers. This is because, since the output buffers include transistors that are much larger than the ones used in the oscillators, they generate higher current spikes which can disrupt the coupling of the oscillators that so heavily relies on the same effect.

Post-layout simulations are done to take into account the changes introduced and the parasitic effects, and the results are presented in Table II.

With this, injection locking is still achieved and the improvement to phase noise is still close to 3 dBc/Hz at an offset of 100 kHz compared to the free-running oscillators. The stacked oscillator's outputs are identical to the ones shown in Fig. 4, but with a lower frequency resulting from the added capacitance by the dummy buffers.

V. CONCLUSIONS

In this work, a know injection lock method for ring oscillators is applied in a new way. It is shown that the successful