Design of a 16MHz LC Oscillator integrated into a CMOS 130nm technology for Space Applications

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***Abstract* — This work addresses the design of integrated oscillators for space applications. An oscillator is an important block in electronic devices which work on the principle of oscillation. The oscillators can be designed from a wide range of well-known topologies. However, not all types of the oscillators can be integrated. The crystal oscillator is one of the oscillators which is impossible to integrate into CMOS technology. In this work, an LC oscillator with the central frequency of 1.024 GHz is designed and with the frequency divider, an output of 16 MHz is obtained to replace an equivalent crystal oscillator. As the oscillation frequency changes with temperature, a voltage controller connected to varactor was the technique selected to compensate the frequency variation. In order to compensate variations at PVT corners, a calibration structure is considered. A temperature sensor will generate the reference voltage to use as a voltage controller and will control the oscillation frequency. The designed LC Oscillator dissipates 27.8mW while exhibiting ±256ppm frequency error over a process, ±10% variation in the power supply voltage and from -10 to 90** °C. **The design was done using a 130 nm CMOS Technology node.**

Keywords—Analog Integrated Circuit Design, LC Oscillator, CMOS Technology, Temperature Sensor, Voltage Control, Varactor

I. INTRODUCTION

Electronic devices make our life easier. In general, an electronic device is a combination of different blocks of the circuit within analog and digital circuits. The oscillator represents an important block in a communication system because tuning a radio, checking the time, use of cellular phone or picking up a portable receiver relies on a properly working oscillator [1]. An oscillator is an important block in electronic devices, being used for example to produce periodic oscillating signals such as sine or square wave. In this paper, an oscillator will be designed as an integrated circuit using a CMOS technological node.

An oscillator is a relevant component of electronics and is widely used in many systems, e.g., communication systems, digital systems, and test equipment. To name a few, the television and radio need to broadcast signals from the transmitters and all these signals are being generated by the oscillator. There are many benefits of implementing the oscillator as part of the integrated circuit. Integrating the oscillator into CMOS Technology will reduce the size, power, and cost as well as improved reliability. The quartz crystal (XTAL) resonator and crystal oscillator (XO) are widely used as a frequency reference in numerous applications [2]. Despite XTALs and XO being excellent frequency references due to the intrinsic high quality (Q) factor, high frequency accuracy and low frequency temperature coefficient (f_{TC}), both the oscillators blocks are difficult to integrate. The alternative solution is to use high-Q MEMS resonators integrated in a microelectronic process technology, which will replace XTAL [2]. However, it is still challenging to integrated into a CMOS technology due to difficulties in packaging and process integration, poor power handling, limited frequency trimming and large f_{TC} [2].

Considering those challenges, a design of an integrated oscillator, which will replace crystal oscillator, was proposed as work for this paper with the specification in Table 1. The output of the integrated oscillator must be 16 MHz with a duty cycle of 50%. The accuracy in terms of total frequency error must be ± 500 ppm. The functional temperature of the components must be within the range of -55 and 125ºC. The performance temperature range for this circuit must be -10 to 90ºC and the power supply is 3.3 V.

The implementation of a circuit will be done in CMOS UMC 130 nm technology.

Table 1 – Specification.

Output freq.	Total freq. error	Supply Vtg. (V)	Funct. Temp.(ºC)	Perform. Temp.(ºC)
16MHZ	± 500ppm	3.3	-55 to 125	-10 to 90

II. BACKGROUND & STATE OF THE ART

The schematic of the double cross coupled oscillator, DCCO is shown in Figure 1. For same bias current consumption, it will have more transconductance than a only NMOS structure.

The frequency of *LC* Oscillator (LCO) considering the coil loss is given by

$$\omega_o = \sqrt{\frac{1}{LC}\left(1 - \frac{C R_L{}^2}{L}\right)} \tag{1}$$

R_L is the real loss. Therefore, the shape of f_{TC} is negative. With the varactor which is the temperature-dependent voltage for the reactive compensation, the (1) becomes

$$\omega_o = \sqrt{\frac{1}{L[C_f + C_v(v_{ctrl}(T))]}\left(1 - \frac{[C_f + C_v(v_{Ctrl}(T))]R_L{}^2(T)}{L}\right)} \tag{2}$$

where C_f is the fixed capacitance, C_v is the variable capacitance and $v_{ctrl}(T)$ is the temperature-dependent linear voltage [2].

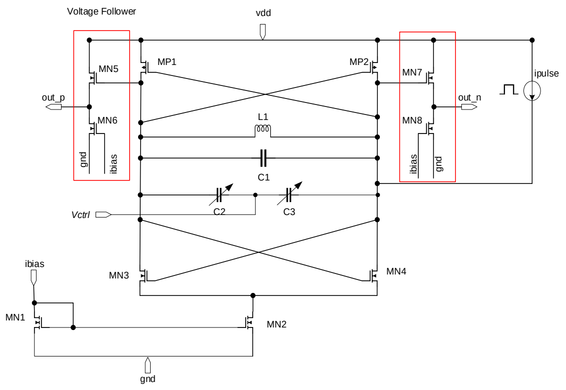

Figure 1 - Schematic of DCCO.

The oscillator is designed to have minimum phase noise and a minimum power consumption for the given oscillation frequency. When low power consumption is required, the bias current needs to be small which result in large parasitic effects in the circuit and increase the phase noise. Furthermore, to have low phase noise, high output voltage swing is required which will result in increasing the power consumption. Therefore, this tradeoff is shown in Equation 3, where ω_0 is the oscillation frequency, P_{dc} is the DC power consumption, $\Delta\omega$ is the offset from the output frequency and $L(\Delta\omega)$ is the oscillator phase noise. The oscillator phase noise is given by Equation 4, where Q is the loaded quality factor of the oscillator, k is the Boltzmann's constant, T is the absolute temperature, p_{sig} is the oscillation output power, F is the noise factor of the amplifier and $\Delta\omega_1/f_3$ is the corner frequency between ω_1/f_2 and ω_1/f_3 portion of the phase spectrum [3].

$$FOM = L(\Delta\omega) + 10\log\left[\frac{P_{dc}}{1mW}\cdot\left(\frac{\Delta\omega}{\omega_0}\right)^2\right] \tag{3}$$

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{p_{sig}}\left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1 + \frac{\Delta\omega_1/f_3}{|\Delta\omega|}\right)\right\} \tag{4}$$

The oscillation condition for Figure 1, should fulfill Equation 5, where α is the small-signal loop gain. The g_{active} in Equation 7 and g_{tank} in Equation 6 are the active and the tank conductance respectively.

$$\alpha \times \max(g_{tank}) \le g_{active} \tag{5}$$

$$g_{tank} = g_{ind} + g_{cap} + \frac{g_{ds}^{pmos}}{2} + \frac{g_{ds}^{nmos}}{2} \tag{6}$$

$$g_{active} = \frac{g_{ds}^{pmos}}{2} + \frac{g_{ds}^{nmos}}{2} \tag{7}$$

When the LCO is connected to the comparator, the load from the comparator affects the differential waveform of the oscillator output. To avoid this load from the comparator, either a voltage follower or an inverter can be used at the output of LCO [4]. In this project, a CMOS voltage follower was used as it consumed minimum power compared to a CMOS inverter (27.8<60.0 mW).

The structure of the voltage follower is in Figure 1, wrap with the red text box. A CMOS analog voltage follower is a low-distortion circuit which used also in high-speed ADCs [5]. The transistor MN6 and MN8 are the current sources.

The transient simulation result is shown in Figure 2. The waveform with red and green color represents the differential output of the oscillator and the oscillation frequency and startup time for the oscillation is illustrated by pink and blue color respectively. The oscillation frequency is 1.024 GHz, the startup time is 15.53 ns, and the output magnitude is 1.33 V.

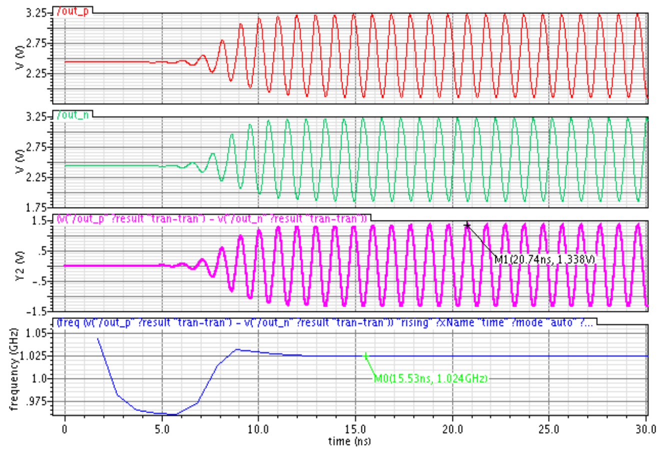

Figure 2 - LCO waveform in Transient analysis.

Figure 3 shows the oscillator frequency which is varying with the temperature. In this project, the oscillator should have an output constant frequency with temperature. Next section will be explained the different techniques used to compensate the temperature frequency drift.

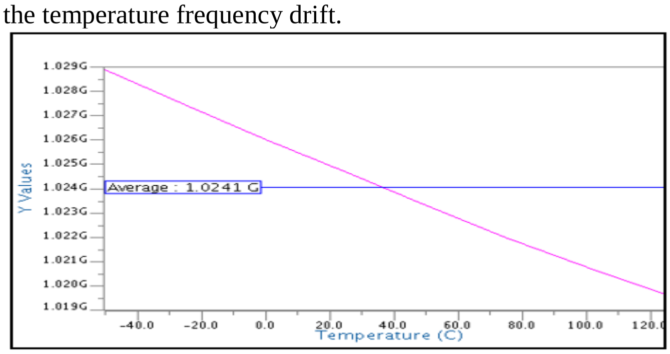

Figure 3 - The output frequency versus temperature.

III. Circuit Design

a. Integrated LCO Topology

The circuit topology is shown in Figure 4 and each block is explained below.

The LCO consists of *LC* tank and cross-couple circuit. The oscillator will be designed to a frequency of 1.024 GHz to increase the Q factor and minimize the frequency divider. To solve the frequency variation with the temperature, a temperature sensor will be used to compensate the drift. Before using the temperature sensor, with varactor and v_{ctrl}, the circuit will evaluate whether the frequency can be compensated or not.

In f_{TC} Compensation, two equally size varactors will be connected in parallel to the *LC* tank where v_{ctrl} will be connected to it. That will control the oscillation frequency as the capacitance of varactor is controlled by an input DC voltage, v_{ctrl}.

The CMOS Switch will compensate the capacitance value to the corners. The idea behind for using this switch is that some corners will have lower and higher frequency than the desired frequency. So, with the switch, the capacitance will be compensated to get desired frequency across process corners.

The temperature sensor will generate the control voltage, v_{ctrl}, which will create a temperature-dependent voltage reference. The detail circuit calibration will be explained in section IV.

The output of the oscillator will be feed to the comparator. The comparator converts the LC oscillator voltages to a digital signal to be used by the digital divider to get the 16 MHz output.

The oscillation frequency of the oscillator is 1.024 GHz. To obtain the 16 MHz output frequency, the frequency divider will divide the frequency. Dynamic latch circuits will be used to minimize the power consumption.

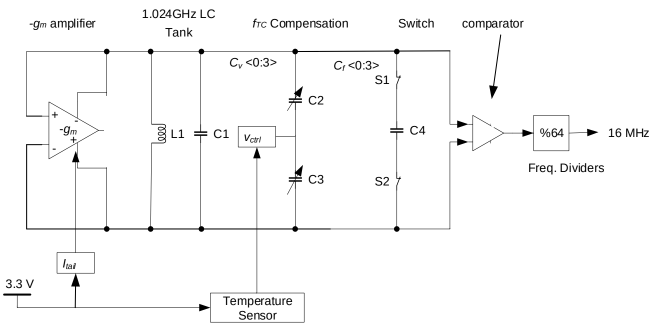

Figure 4 - Schematic of LCO chip architecture including Temp. Sensor.

b. Temperature Sensor

Analog temperature sensors create a temperature-dependent voltage reference. From section II, the f_{TC} is negative slope for the oscillator, thus temperature sensor must be a positive slope. Figure 5 is the Proportional To Absolute Temperature, PTAT voltage which will generate v_{ctrl}.

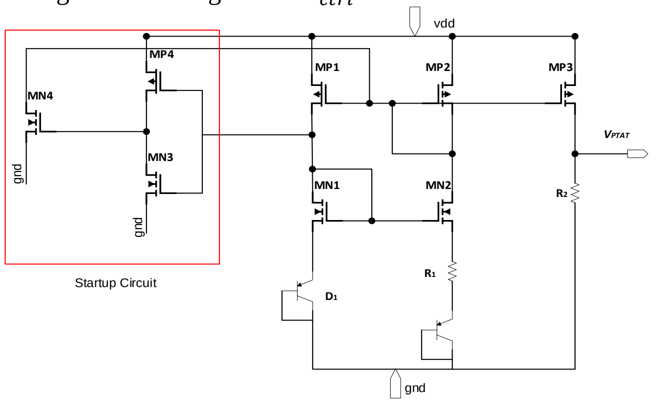

Figure 5 - Schematic of an analog PTAT voltage reference.

A CMOS current mirror is used to generate equal current (I_1= I_2), regardless of the supply voltage [6]. To promote the current flow through the resistor, the voltage drops across D_2 (V_{D2}) must be smaller than the one across D_1. The size of the D_2 should be greater than D_1 to have the same amount of current flowing through both devices and the smaller voltage drop across D_2. This happens because the value of the saturation current is directly proportional to the device junction area [7].

Another possible solution to achieve the same current at different branches is by using equal devices and reduce V_{D2}. If K diode in parallel is used to implement D_2, the current I will flow equally through K device. The voltage drops across the diode D_1 and D_2 is can be expressed by

$$V_{D1} = \frac{k}{q}.T.In\left(\frac{I}{I_{s1}}\right) \tag{8}$$

$$V_{D2} = \frac{k}{q}.T.In\left(\frac{I}{kI_{s1}}\right) \tag{9}$$

So, as the current flowing through each of the K devices in parallel is smaller than the current flowing on the left branch, through D_1, V_{D2} will be smaller than V_{D1}. Assuming two branches of the current mirror are matched, I_{D1}= I_{D2} = I.

hence

$$V_{D1} = V_{D2} + R.I \tag{10}$$

Solving 8 and 9 by considering I_{s1}= I_{s2} = I_s as all transistors have the same size.

$$I = \frac{k.In\,K}{q.R}.T \tag{11}$$

The current will be proportional to the absolute temperature. However, the temperature coefficient of the resistor will distort the linearity of the PTAT current. In order to obtain a PTAT voltage, the current mirror by MP3, on the right branch of the circuit. The resistor on this branch defines the voltage at the output of the circuit. This voltage will be given by

$$V_{PTAT} = I.L.R \tag{12}$$

where L is a scale factor between R1 and R2 used in the circuit.

The change in reference voltage with temperature is given by

$$\frac{\partial(V_{REF})}{\partial T} = \frac{nk.L.InK}{q} \tag{13}$$

Using $k = 1.38 \times 10^{-23}$ and $q = 1.6 \times 10^{-19}$, the change of the reference voltage with temperature will be in mV/C.

The temperature sensor a being self-biasing circuit, it required a startup circuit as shown in schematic in Figure 5. The startup circuit is used to avoid a zero-current state. It should also not interfere with the normal operation of the reference once the desired operating point is reached [8].

PTAT couldn't obtain the required slope and reference voltage. Therefore, the circuit was changed to bandgap reference. However, even with the bandgap reference circuit, the correct slope at correct reference voltage couldn't obtain. The bandgap reference circuit was modified as illustrated in Figure 6. Here the output, $outx$ will be the control voltage. It is given by

$$outx = Itemp * R_3 + Vconstant \tag{14}$$

where $Vconstant$ is given by $Ivbg * R_5$.

Depending on the corner a constant offset voltage is needed and correspondent PTAT slope. Therefore, the bandgap gives the constant offset voltage and the PTAT current, the correspondent slope.

The $Vconstant$ will be independent of the temperature. The source, vbg for the Voltage Control Voltage Source (VCVS) was feed from the output reference voltage of the bandgap. It was designed with zero slopes. The only variable voltage with the temperature is $Itemp * R_3$. Therefore, to get correct slope at correct reference voltage which was the main issue in the previous two solutions was solved with this modified circuit.

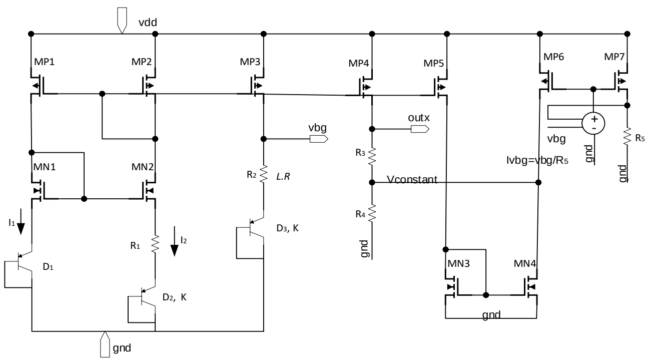

Figure 6 - Modified Bandgap reference circuit.

Now, by adjusting the value of the resistance at R_3, R_4, and R_5, the correct slope at correct reference voltage can be obtained. The resistor string (R_3, R_4, and R_5) is the resistor which is connected in series and they are an identical resistor with the value 2.7 KOhm. By changing the number of the string, the value of resistance was adjusted.

To have a higher gradient of the slope, R_3 is increased and vice versa. The R_4 is constant. The $Ivbg$ is controlled by R_5 to have higher and lower voltage at the output, $outx$. To have higher voltage at $Vconstant$, R_5 is decreased so that $Ivbg$ will be higher and increased R_5 to have low $Vconstant$. With those variable resistors, a required slope at correct reference voltage is obtained.

To implement the circuit into UMC 130 nm technology, the following transistor dimension was chosen in Table 3.

Table 2 - Sizing of the MOS (LCO).

	WF (um)	LF (nm)	NF	M
MP1 & MP2	5	500	2	30
MN1	5	700	2	1
MN2	5	700	2	15
MN3 &MN4	5	500	2	10

Table 3 - Sizing of the MOS (Temp. Sensor).

	WF (um)	LF (nm)	NF	M
MN1 & MN2	5	340	1	1
MP1, MP2, MP3	15	340	1	1

IV. Simulations & Results

First, the simulation of the LCO was done to see the slope (change in output voltage with temperature) of the output frequency. All the corner of the circuit was simulated, and analysis was done. After knowing the change in output voltage with the temperature of the LCO, the next task is to simulate the temperature sensor to obtain the correct slope and a reference voltage.

a. *LCO with all sub-circuit*

Now, the LCO circuit was simulated along with all the sub-circuits after preparing the test bench as shown in Figure 7. With the voltage follower connected at the output of the oscillator, the result at different corner has improved. With just Vctrl from the temperature sensor, the frequency can be compensated, and it doesn't need an extra circuit, CMOS switch to compensate capacitance at the corner. The dimension of the transistor for LCO is shown in Table 2. The output frequency of the comparator and inverter is 1.024 GHz which was feed to the 64-bit frequency divider to give an output of 16 MHz. The digital output from the transient analysis of the comparator, inverter and frequency divider is illustrated in Figure 8 and 9.

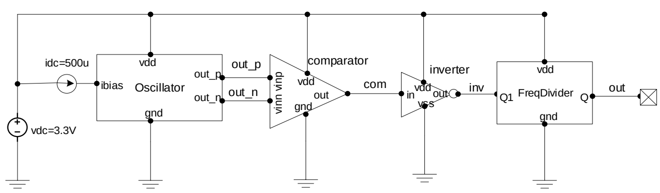

Figure 7 - Test bench of LCO along with sub-circuits.

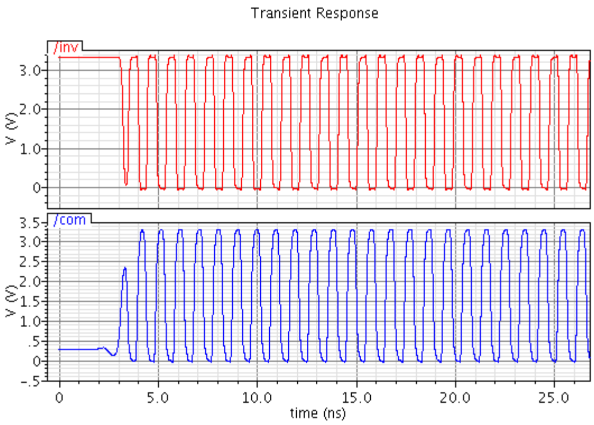

Figure 8 - The digital output of the comparator and inverter.

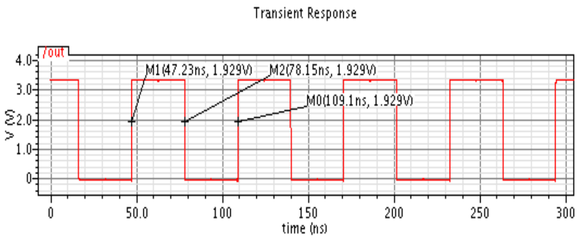

Figure 9 - The digital of the frequency divider.

The peak frequency variation is higher than the specification. Simulating all the corners gives the result as shown in Table 4 and Figure 10. The corners are categories into different type depending on the output frequency.

To compensate the frequency drift of Table 4, the simulation was done by sweeping the Vctrl for the different types. The Vctrl that required to compensate frequency at the different type of corners and typical is shown in Table 5. At low Vctrl, the capacitance of the varactor is high, and the frequency will be low. Similarly, for higher Vctrl, the capacitance of varactor will be low, which result in high frequency. With this idea, the frequencies at the different corners are compensated.

The peak frequency variation (df), was also found for all the corner cases. The df is wider for all the cases.

Table 4 - Output frequency at different corners.

Corner	Freq (MHz)	Type
9,10,11,12,25,26,27,28 41,42,43,44,57,58,59,60	15.1-15.4	Lower
1,2,3,4,17,18,19,20, 33,34,35,36,49,50,51,52	15.6-15.9	Low
13,14,15,16,29,30,32,32 45,46,47,48,61,62,63,64	15.9-16.5	Ok
5,6,7,8,21,22,23,24 37,38,39,40,53,54,55,56	16.8-17.2	High

Table 5 - Vctrl for different corners.

Type	Lower	Low	Ok	High	Typ
Vctrl	2.05	1.75	1.5	1.05	1.65
df(kHz)	238	254	678	302	237

In order to find the slope for the oscillator, the simulation was done by sweeping Vctrl for maximum and minimum temperature. The slope is given by

$$Slope = \frac{V_2 - V_1}{Temp_{max} - Temp_{min}} \quad (15)$$

Based on the slope of the oscillator, the temperature sensor will be designed to have a reference voltage with the correct slope.

For the typical condition, the slope was found by the Figure 11. The calculated slope is 0.728 mV/C. Which mean the temperature sensor need to have a slope of 0.728 mV/C at the reference voltage of 1.65V.

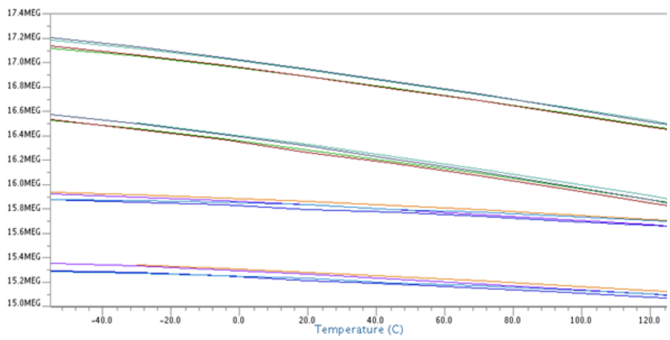

Figure 10 - Frequency Versus Temperature for the corners.

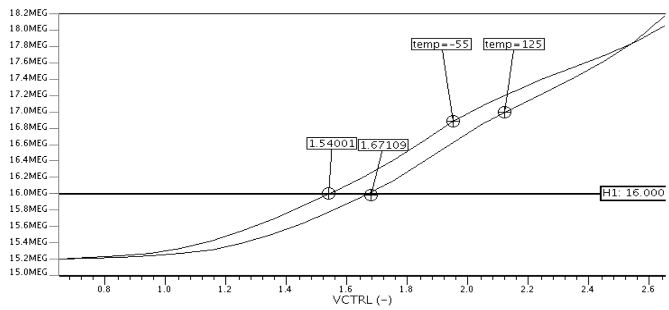

Figure 11 - Vctrl for the Max (1.67109V) and Min (1.54001V) Temperature at 16 MHz.

Similarly, the required slope for the different corners is calculated from the simulation result which is shown in table 6.

Table 6 - Slope (mV/C) for corners.

Type	Vctrl@max Temp (V)	Vctrl@min Temp (V)	Slope (mV/C)
Typ	1.67108	1.54001	0.728
Lower	2.05619	1.94979	0.591
Low	1.75554	1.62547	0.723
Ok	1.71884	1.30381	2.305
High	1.08885	0.77953	1.718

b. Temperature Sensor

The temperature sensor is designed for a 3.3 supply voltage and current consumption of 20uA. From Equation 12, the solution for R is:

$$R = \frac{0.026 * In(8)}{20uA} = 2.7Kohm \quad (16)$$

$$l = \frac{R2}{R1} \quad (17)$$

From Equation 17 and 12, l and V_{PTAT} are calculated for the requirements for the different corner. The theoretical value for the change in reference voltage with temperature, $\frac{\partial(V_{REF})}{\partial T}$ for different corners and the typical condition is in Table 7. Using Equation 12, $\frac{\partial(V_{REF})}{\partial T}$ is calculated. However, a modified slope for Table 7 can be found in Table 9.

Table 7 - V_{PTAT} and $\frac{\partial(V_{REF})}{\partial T}$ for different corners.

	L	V_{PTAT} (V)	$\frac{\partial(V_{REF})}{\partial T}$ (mV/C)
Typ	28	1.65	5.02
Lower	35	2.05	6.27
Low	30	1.76	5.38
Ok	25	1.47	4.48
High	18	1.06	3.23

The corner simulation for the bandgap reference voltage is shown in Figure 13. For all the corner, the reference voltage is approximately equal.

In Figure 12, the slope required for the oscillator for typical condition and different type of corners is illustrated. In Table 9, the reference voltage and slope obtained from the simulation result (Temperature Sensor) are compared with the slope and reference voltage needed for the oscillator. Next task is to simulate the oscillator with the temperature sensor.

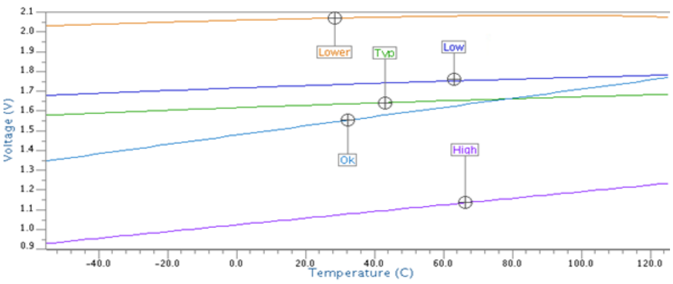

Figure 12 - Slope for the temperature sensor.

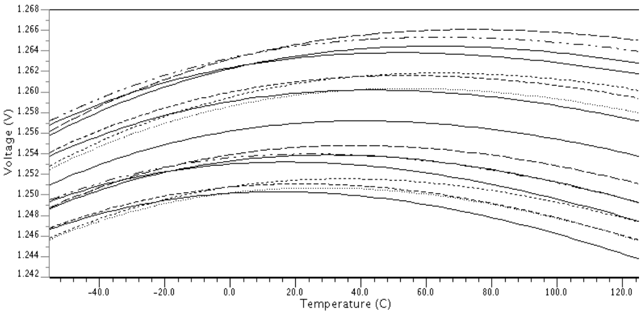

Figure 13 - Corner simulation for the bandgap reference.

c. LCO with Temperature Sensor

After the design of temperature sensor (bandgap reference), the final task is to connect with the LCO as shown in Figure 16. The reference voltage generates by the bandgap reference is connected to the Vctrl of the oscillator. The simulation was done to check whether the output frequency of the LCO is having minimum df at the typical condition. Similarly, all the corners are simulated. The df for the typical condition is illustrated in Figure 14.

The final result for the compensated output frequency is in Table 8.

Table 8 - Peak frequency Variation at output frequency (16 MHz).

	Typ	Lower	Low	Ok	High
Comp. (kHz)	4.09	25	22	20	25
Not Comp. (kHz)	238	254	678	302	237

In typical condition, the output frequency is compensated approximately 58 times lower than not compensated output frequency.

The comparison between compensated and not compensated output frequency at the corner of the integrated LCO is illustrated in Figure 15. A temperature sensor has compensated the output frequency approximately 10, 30, 15 and 10 times lower than not compensated frequency for “Lower”, “Low”, “Ok” and “High” respectively.

Table 9 - Reference voltage and slope from Temperature Sensor

Type	R_3 (string)	R_4 (string)	R_5 (string)	$Vconstant$ (V)	$outx$ (V)	Required V_{REF} (V)	Slope (mV/C)	Required Slope (mV/C)
Typ	5	23	40	1.408	1.66	1.65	0.829	0.728
Lower	4	23	30	1.877	2.07	2.05	0.592	0.591
Low	5	23	38	1.482	1.74	1.75	0.830	0.723
Ok	14	23	71	0.801	1.54	1.50	2.346	2.305
High	10	23	105	0.543	1.07	1.05	1.686	1.718

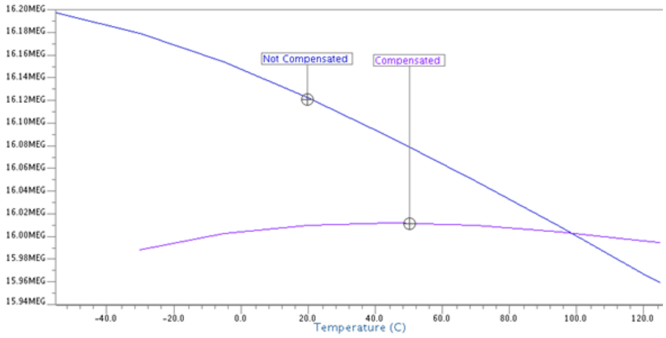

Figure 14 - Compensated compared with not compensated output freq. in Typical condition.

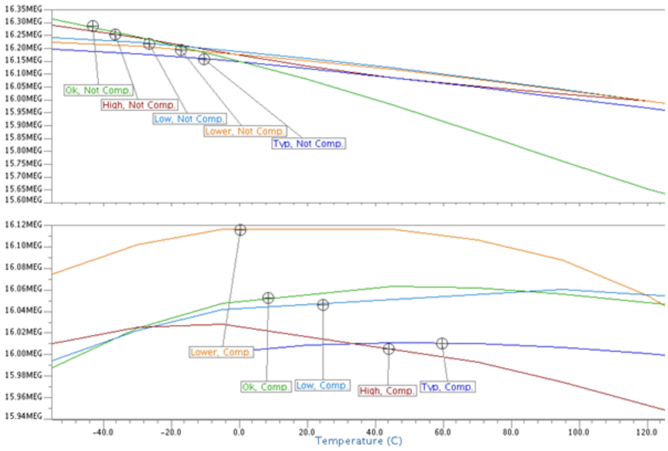

Figure 15 - Comparison between not compensated and compensated output frequency.

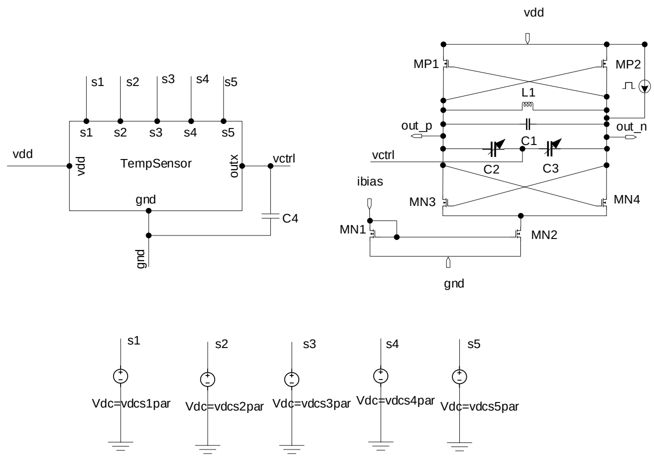

Figure 16 - LCO with Temp. Sensor.

V. Conclusions And Future Work

This work demonstrates an implementation of LCO into CMOS technology with no external components and to compensate the output frequency of the integrated LCO. The total frequency error obtained is ±256ppm which is lower than the specification, ±500ppm. Table 10 shows the achieved results.

The result can be improved by considering the recalculation for the temperature sensor circuit to obtain the correct slope and reference voltage required to compensate the LCO output frequency.

Table 10 - The Final Results.

	Output Freq. (MHz)	Duty Cycle	Total Freq. error	df (kHz)	Power dissip.
Spec.	16	50%	±500ppm	8	≤ 30mW
This work	16	50%	±256ppm	4.09	27.8mW
[2]	25	50%	±152ppm	19	59.4mW

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