Model of a Battery Energy Storage System for Power System Stability Studies

Daniel J. R. Santos
Instituto Superior Técnico
University of Lisbon
Lisbon, Portugal
danieljrs1993@gmail.com

***Abstract*—this paper aims the detailed study of a Power Conversion System (PCS) of a Battery Energy Storage System (BESS). An effective energy storage device, such as a BESS, is able to offer to the network many advantages, both in power quality applications and in energy management. A Power Conversion System (PCS) is responsible for the interface between the DC side and the AC side of a BESS, i.e. between the battery subsystem and the Point of Common Coupling (PCC). When performing power system stability studies using a BESS its relevance among the system components leads to the necessity of a PCS model. Thus a current-mode control in dq-frame of a VSC system made possible the control of the real and reactive power in a BESS. Finally, the PCS model was used to simulate the connection of a battery model, developed in another dissertation work, with an AC load.**

Keywords- BESS, Power Conversion System, Power Control, Power Quality, Power System Stability Studies.

I. INTRODUCTION

The world's energy consumption has increased over the years and the expectation is for this behavior to continue. In the past decades, there has been an increased awareness of the harmful effects caused by CO_2 emissions on the sustainability of the environment. Therefore, a new challenge has arisen: to maintain economic growth whist providing energy security and environmental protection. Accordingly, on-site small-scale electricity generation, also called distributed generation (DG), emerged as a solution for the energy challenge, eliminating the cost, complexity, interdependencies and inefficiencies with transmission and distribution. An important form of DG is the grid connection of Renewable Energy Sources (RES). RES, as photovoltaic and wind, have probabilistic nature, so its output is intermittent and fluctuates. The increasing penetration of these DGs into microgrids can affect the stability of the electrical grid [1-3].

Energy storage devices, such as battery energy storage systems (BESS) are capable of providing the microgrid with active and reactive power simultaneously, providing the required energy security level. The introduction of this device in a microgrid is important for purposes of Power System Stability Studies.

The Power Conversion System (PCS) plays an important role in a BESS. This component interfaces the AC side of the system with the batteries subsystem. It controls the real and reactive power exchanged with an interfaced load at the point of common coupling (PCC). Thus, in order to interface a BESS with a microgrid, a model of the PCS becomes useful.

In this dissertation a PCS model for BESS applications was developed. It was considered a current-mode control in dq-frame of a two-level VSC to control the active and reactive power at the PCC. In order for this control mode to be used it was necessary to design a Phase- Locked Loop (PLL) compensator to track the imaginary component of the AC-voltage at zero.

The PCS model was then used to interface a Battery Model to an AC load, simulating the behavior of a BESS.

The PCS model of this dissertation is a good foundation for future BESS related studies, as it can effectively perform a bidirectional control of the active and reactive power of the system

II. BATTERY ENERGY STORAGE SYSTEM

Firstly, it is important to look at the constitution of a BESS: A BESS, represented in Figure 1, is composed of a DC battery subsystem, a Power Conversion System, and a Coupling Transformer.

A. Battery

The battery subsystem is composed of battery containers and of Battery Management Systems (BMS). Each container contains modules of battery cells that are responsible for the energy storage. The BMS performs the necessary measurements (voltage, current, temperature) to manage the batteries, in order to increase the safety of the system.

B. Coupling Transformer

When the voltage in the battery array is low, a coupling transformer connects the battery system to the grid.

C. PCS

The Power Conversion System is composed of an electronic bi-directional converter and of a control system. It acts as a rectifier when the batteries are charging, converting

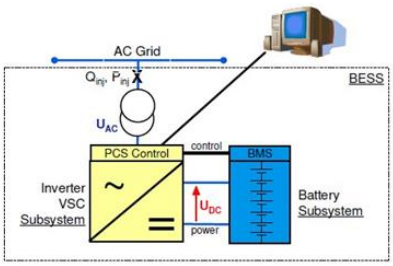

Figure 1-Battery Energy Storage System Components [4]

AC to DC current, and acts as an inverter during the supplying of energy to the grid, converting DC to AC current. The work of this dissertation is focused mainly on a model of a PCS, so the VSC and the control system will be the focus of this chapter.

1) VSC

The VCS considered was a three-phase two-level-VSC, represented in Figure 2. The switches are IGBT. The DC/AC half-bridge converter may be used as a building block for the three-phase, DC/AC VSC, so the principles of operation of the DC/AC half-bridge converter can be studied and then extrapolated to those of the three-phase VSC.

2) Control of DC/AC Half-Bridge Converter

The DC/AC half-bridge converter, illustrated in Figure 2, is composed of an upper and of a lower switch cell, numbered 1 and 4 respectively. Each switch cell comprises of a fully controllable unidirectional switch (Q1 and Q4) connected in antiparallel with a diode. Nodes p and n represent the DC-side terminals of the converter, while the node t represents the AC side. The half-bridge converter is interfaced with a voltage source, V_s. The AC-side voltage V_t is a switched waveform containing voltage ripple. Thus, between V_t and V_s there is an interface reactor that acts as a filter, providing low-ripple AC-side current.

The half-bridge converter operates based on the varied switching of Q1 and Q4. The commands of Q1 and Q4 are expressed through a pulse-width modulation (PWM) strategy.

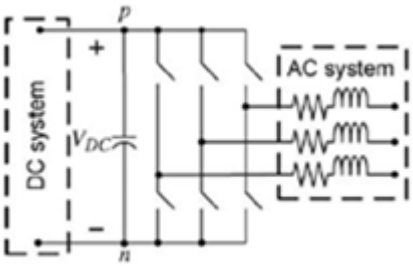

Figure 2- Schematic diagram of the three-phase and two-level VSC[5]

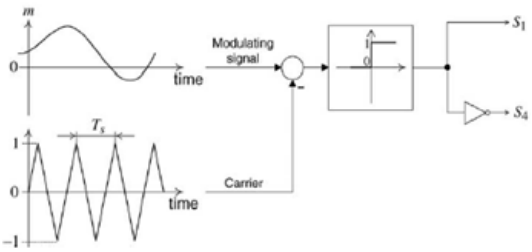

Figure 3- PWM strategy scheme

The PWM compares a high-frequency periodic triangular waveform, the carrier signal, with a modulating signal, as seen in Figure 3. The carrier signal has a periodic waveform with period Ts, and its amplitude oscillates between -1 and 1. The switching instants of Q1 and Q4 are determined by the intersections of the modulating and the carrier signals. The mechanism that generates PWM gating pulses is represented in Figure 3. The resultant function for each switch is established as:

$$s(t) = \begin{cases} 1, if\ the\ switch\ is\ commanded\ to\ conduct \\ 0, if\ the\ switch\ is\ commanded\ to\ turn\ off \end{cases} \quad \textbf{(1)}$$

The dynamics of the AC-side current of the equivalent circuit of Figure 4 is expressed by:

$$\mathrm{L}\frac{di}{dt} + (R + r_{on})i = V_t - V_s \quad \textbf{(2)}$$

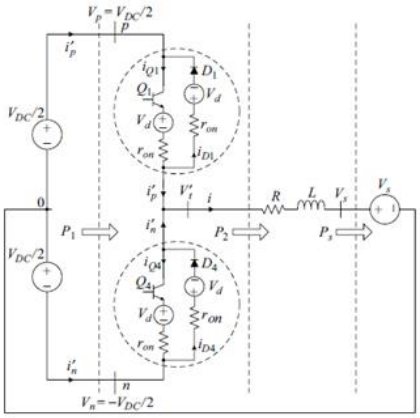

Figure 4- Simplified power circuit diagram of a half-bridge converter with non-ideal switches

Where

$$V_t = \frac{V_{DC}}{2} m \quad (3)$$

In the equation (2) i represents the state variable, V_t is the control input and V_s is the disturbance input of the system. The system output can be the power exchanged with the AC-side, given by:

$$P_s = V_s i \quad (4)$$

Thus, the control input can be controlled by the modulating signal m, to which is proportional. The respective control block diagram, is represented in Figure 5

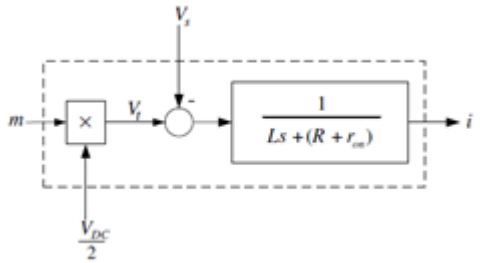

Figure 5- Control model of the half-bridge converter

The control diagram of Figure 5 has the objective of regulating the output i at a predefined reference value.

3) Space Phasors and two-dimensional frames

In three-phase VSC systems it is often required the tracking of a sinusoidal command, swiftly and with small steady-state errors, and to impose rapid changes in amplitude or phase of the commands. A compensator designed to track a sinusoidal command with a high degree of fidelity is more elaborate than a compensator for DC command tracking. Therefore, the control design of a three-phase VSC system is distinctly simplified if the problem of sinusoidal command tracking is transformed into a problem of DC command tracking.

The two-dimensional frames, composed mainly by the αβ -frame and by the dq-frame, represented in Figure 3.13 along with the abc-frame, simplify the analysis and control of a VSC system. Both the αβ-frame and the dq-frame transform the problem of controlling a system of three half-bridge converters, as is the case with the three-phase VSC, to a problem of two similar subsystems. Additionally, the dq-frame transforms a sinusoidal command tracking problem to an equivalent DC command tracking problem. For that reason, proportional-integral (PI) compensators can be used for the control. Commonly, components of power systems are expressed and studied in dq-frame. Thus, the representation of VSC systems in the dq-frame facilitates design and analysis tasks based on methods usually applied for power systems.

The Park transform is a space vector transformation of three-phase time-domain signals from a stationary coordinate system, abc, to a rotating coordinate system.dq0. The transform applied to time-domain voltages in the abc frame is as it follows:

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (5)$$

The representation of a space phasor in dq-frame is defined by:

$$\vec{f} = (f_d + j f_q) e^{j\varepsilon(t)} \quad (6)$$

Where f_d and f_q are the components of vector $\vec{f}$ in a coordinate system rotated by ε(t) with respect to the αβ-frame. The rotational speed of the dq-frame is the same as that of $\vec{f}$. ε(t) is given by:

$$\varepsilon(t) = \varepsilon_0 + \int \omega(\tau)\, d\tau \quad (7)$$

Finally, at steady-state, balanced, sinusoidal condition, the apparent power is given by:

$$S(t) = P(t) + jQ(t) = \frac{3}{2} \vec{v}(t) \vec{i}^{*}(t) \quad (8)$$

Then in tomes that the real power is given by (9) and the reactive power is given by (10):

$$P(t) = \frac{3}{2} \left[v_d(t) i_d(t) + v_q(t) i_q(t) \right] \quad (9)$$

$$Q(t) = \frac{3}{2} \left[-v_d(t) i_q(t) + v_q(t) i_d(t) \right] \quad (10)$$

III. PCS MODEL

The Figure 6 illustrates the structure of the grid-imposed frequency VSC system. The averaged ideal three-phase VSC can be either a two-level VSC or a three-level Neutral Point Clamped (NPC) Converter. The VSC is modeled by a power processor that includes a DC-bus capacitor, C, a current source, i_{loss}, representing the converter switching power loss, and on-state resistances at the AC side, r_{on}, representing the converter conduction power loss. The DC-side is connected in parallel to the battery storage system. The AC system is

modeled by V_{sabc}, an ideal three-phase voltage source, balanced and sinusoidal. Each branch of the VSC is connected to the AC system through a series RL branch.

The VSC system of Figure 6 exchanges real and reactive power, Ps(t) and Qs(t) respectively, with the AC system at the PCC. Thus, with adequate control strategy, the VSC system of 6 can be used as a real and reactive power controller.

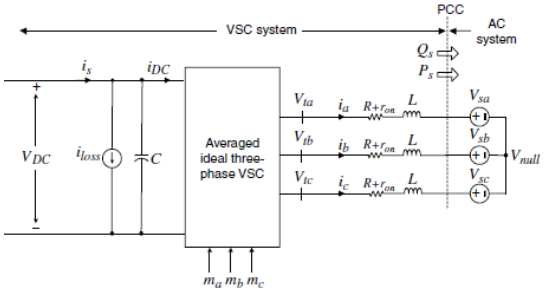

Figure 6- Schematic of a grid-imposed frequency VSC[5]

There are two major methods for controlling Ps and Qs in the VSC system of Figure 6: current-mode control and voltage-mode control. Despite voltage-mode control being a simple method with a low number of control loops, there is no control loop closed on the VSC line current. Therefore, the VSC is unprotected against overcurrents. Contrarily in the current-mode control the VSC line current is regulated by a dedicated current-control scheme, through the VCS AC-side terminal voltage. There are other advantages of the current-mode control, such as superior dynamic performance and higher control precision. Thus, the control strategy used in this model is the current-mode control.

A. Current-mode Control

As discussed in section II, instantaneous decoupled control of the reactive and active power exchanged with the AC system is possible in dq-frame control. Contrarily to the αβ-frame control, whose control variables are sinusoidal functions of time, the dq-frame control of a grid-imposed frequency VSC system features DC quantities in the steady state as control variables. This attribute facilitates the compensator design therefore reducing the complexity of the dq-frame control system. Additionally, since the control variables are DC quantities, zero steady-state error is achieved by including integral terms in the compensators. The power system dynamics, represented in (2), are commonly modelled and analyzed in dq-frame. Due to all the enumerated advantages of the dq-frame control of a grid-imposed frequency VSC, that will be the adopted control strategy in the model of the PCS.

By expressing $\vec{i}$ and $\overrightarrow{V_t}$ in the dq-frame using (6), and then substituting them in the d and q components of the dynamic equations, (2), it is possible to obtain the equations that describe the system of Figure 7:

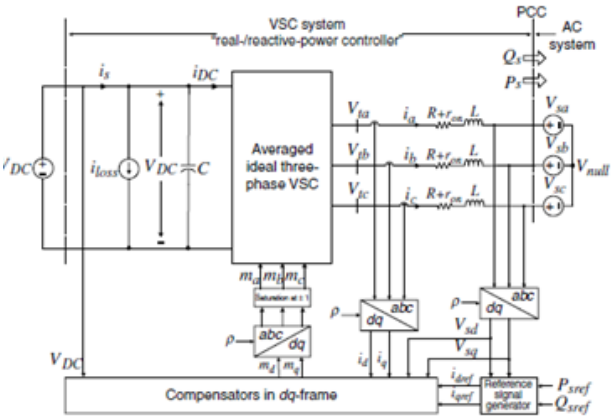

Figure 7- Schematic of a current-controlled real and reactive power controller in dq-frame[5]

$$L\frac{di_d}{dt} = L\omega(t)i_q - (R + r_{on})i_d + V_{td} - \overrightarrow{V_s}\cos(\omega_0 t + \theta_0 - \rho) \quad \textbf{(13)}$$

$$L\frac{di_q}{dt} = -L\omega(t)i_d - (R + r_{on})i_d + V_{td} - \overrightarrow{V_s}\sin(\omega_0 t + \theta_0 - \rho) \quad \textbf{(14)}$$

$$\frac{d\rho}{dt} = \omega(t) \quad \textbf{(15)}$$

The AC system voltage of the VSC system of Figure 7 may be described by the space-phasor:

$$\overrightarrow{V_s}(t) = \widehat{V_s}e^{j(\omega_0 t+\theta_0)} \quad (16)$$

Using (6) to represent (16), it can be obtained:

$$V_{sd} = \widehat{V_s}\,cos(\omega_0 t + \theta_0 - \rho) \quad \textbf{(17)}$$

$$V_{sq} = \widehat{V_s}\,sin(\omega_0 t + \theta_0 - \rho) \quad \textbf{(18)}$$

If $\rho(t) = \omega_0 t + \Theta_0$, then, based on (18), $V_{sq}=0$. Therefore, based on (9) and (10), the real and reactive power, P_s and Q_s, are proportional to i_d and i_q, respectively. Thus, if ρ(t) is regulated at $\omega_0 t + \Theta_0$ then the problem of power control in the VSC system model can be converted to a problem of control of the AC line current of the VSC system of Figure 2.

Consequently, it was designed a mechanism that regulates ρ(t) at ω0t+θ0, the Phase-Locked Loop (PLL).

1) PLL

A mechanism to regulate V_{sq} at zero was conceived, based on the following feedback law:

$$\boldsymbol{\omega(t) = H(p)V_{sq}(t)} \quad \textbf{(19)}$$

Where H(p) is a linear transfer function, known as compensator, and p=d(.)/dt is a differentiation operator. By substituting V_{sq} for (18) in (19) it is obtained a nonlinear dynamic system, known as the PLL:

$$\boldsymbol{\omega(t) = H(p)\widehat{V_s}\sin(\omega_0 t + \theta_0 - \rho)} \quad \textbf{(20)}$$

Under certain conditions, the nonlinear characteristic of the PLL may lead to unsatisfactory behavior. For example, if the initial conditions of the PLL corresponded to ρ(0)=0 and ω(0)=0, the term $H(p)\widehat{V_s}\sin(\omega_0 t + \theta_0 - \rho)$ in (20) would be a sinusoidal function with frequency ω_0.Consequently, the PLL would fall in a limit cycle and ρ would not track $\omega_0 t + \theta_0$. In order to prevent this to happen, the control law was modified to:

$$\begin{gathered}\boldsymbol{\omega(t) = H(p)V_{sq}(t)} \\ \boldsymbol{\omega(0) = \omega_0} \\ \boldsymbol{\omega_{min} < \omega < \omega_{max}}\end{gathered} \quad \textbf{(21)}$$

Where ω(t) has an initial value of ω_0 and is limited to the lower and upper limits of, ω_{min} and ω_{max}., respectively. The values selected had to be close to ω_0 to restrict the range of variations for $\omega(t)$, and at the same time had to be wide enough to allow for excursions of $\omega(t)$ during transients.

As the function of the PLL is made to track $\omega_0 t+\Theta_0$, the term $\omega_0 t+\Theta_0 -\rho$ in (20) is approximately zero. Thus, (20) can be simplified as:

$$\boldsymbol{\omega(t) = H(p)\widehat{V_s}(\omega_0 t + \theta_0 - \rho)} \quad \textbf{(22)}$$

The control loop of Figure 8 represents equation (22) of the PLL

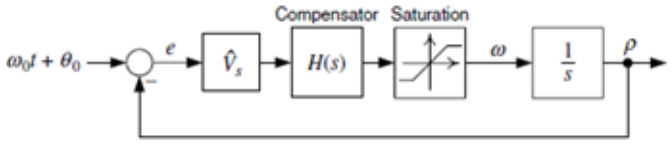

Figure 8- Control block diagram of the PLL[5]

The schematic diagram of the PLL model as part of the current-mode control diagram of Figure 6 is represented in Figure 8. The PLL transforms V_{sabc} to V_{sdq} based on (5), and by adjusting the rotational speed of the dq-frame, ω, it forces V_{sq} to zero and V_{sd} to V_s in the steady-state. In order for the PLL to follow the control law of (21), a saturation block is introduced in the control block diagram of the PLL. The compensator, H(s), has a major influence in the performance of the PLL, therefore it will be designed in the next subchapter.

2) PLL compensator design

The reference signal of the control block of Figure 8, $\omega_0 t+ \theta_0$, is composed of a constant component, θ_0, and a ramp function, $\omega_0 t$. The loop gain includes an integral term, so ρ tracks the constant component of the reference signal with zero steady-state error. To ensure a zero steady-state error for the ramp component, the loop component must include at least two integrators. Thus, the transfer function *H(s)* must include one integral term, that is, one pole at s=0.

Simultaneously, the compensator must take into account the unbalanced and harmonic components of the three-phase voltages:

$$V_{sa}(t) = \widehat{V_s}\cos(\omega_0 t + \theta_0) + k_1\widehat{V_s}\cos(\omega_0 t + \theta_0) \quad \textbf{(23)}$$

$$V_{sb}(t) = \widehat{V_s}\cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) + k_1\widehat{V_s}\cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) \quad \textbf{(24)}$$

$$V_{sc}(t) = \widehat{V_s}\cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) + k_1\widehat{V_s}\cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) \quad \textbf{(25)}$$

Where k1 represents the amplitude of the negative sequence harmonic component compared to the amplitude of the positive sequence component.

$$V_{sd} = \widehat{V_s} + k_1\widehat{V_s}\cos(2\omega_0 t + 2\theta_0) \quad (26)$$

$$V_{sq} = -k_1\widehat{V_s}\sin(2\omega_0 t + 2\theta_0) \quad (27)$$

If the sinusoidal components of V_{sq} are not mitigated by H(s), then ω and ρ also display fluctuations. Those are modulated by the control signals and after transformations between the abc-frame and the dq-frame result in the formation of troublesome voltage and current distortions in the VSC system. Amongst the AC components of V_{sq} the ones with larger magnitude are the more important, as is the case with the double-frequency component, represented in (24) and (25), often generated during faults.

Therefore *H(s)* includes one pair of complex-conjugated poles, at $s=\pm j2\ \omega_0$, with the purpose of attenuating the double-frequency component of V_{sq}. Furthermore, to ensure that the loop gain magnitude drops with the slope of -40dB/dec for $\omega>2\ \omega_0$, the compensator must include a double real at $s=-2\ \omega_0$. Finally, the compensator for the PLL takes the form of:

$$H(s) = \left(\frac{h}{V_{sn}}\right)\frac{s^2 + (2\omega_0)^2}{s^2(s + 2\omega_0)^2}F(s) \quad \textbf{(28)}$$

Where V_{sn} is the nominal value of $\hat{V}_s$,, h is a constant equal to $6x10^3$, and the F(s) represents the proper transfer function with no zero at s=0.

B. Current-mode Control with PLL

It was considered the PLL model (28), where $\omega_0=2\pi x50$ rad/s and $\hat{V}_s = 400V$. Then, assuming that both a gain crossover frequency of ω_c=200 rad/s and a phase margin of 60° are needed, it is calculated that F(s) must add 85° advance to the phase loop. Accordingly, F(s) is composed of two cascaded lead compensators, each to provide 42.5° at 200 rad/s. Thus,

$$F(s) = \left(\frac{s + \frac{p}{\alpha}}{s + p}\right)\left(\frac{s + \frac{p}{\alpha}}{s + p}\right) \quad \textbf{(29)}$$

Where

$$p = \omega_c\sqrt{\alpha} \quad \textbf{(30)}$$

$$\alpha = \frac{1 + sin\delta_m}{1 - sin\delta_m} \quad \textbf{(31)}$$

and δ_m=42.5° is the phase of each lead compensator at ω_c.

The reference signal generator of Figure 7 generates i_{dref} and i_{qref} through the equations (32) and (33):

$$i_{dref} = \frac{2P_{sref}}{3V_{sd}} \quad \textbf{(32)}$$

$$i_{q_{ref}} = -\frac{2Q_{s_{ref}}}{3V_{sd}} \quad \textbf{(33)}$$

The reference signals generated are DC variables if P_{sref} and Q_{sref} are constant signals. If the control system can provide fast reference tracking, then $P_s(t)$ and $Q_s(t)$ can be controlled independently by i_d and i_q. Based on the dynamic equations that describe the VSC the control loops of Figure 9 were deduced.

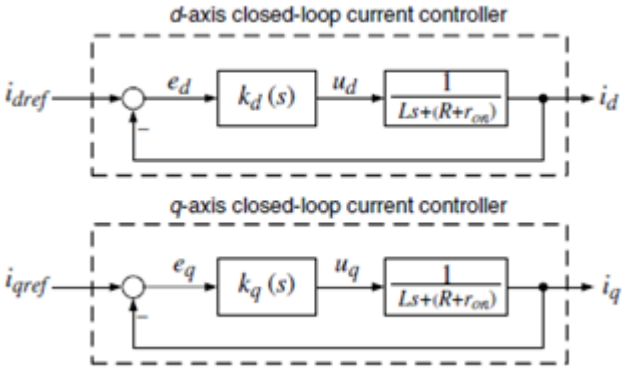

Figure 9- Simplified block diagram of the current-controlled VSC system

As the control loops of Figure 9 are similar, the compensators k_d and k_q are identical as well.

$$\boldsymbol{k_d(s) = k_q(s) = \frac{k_p s + k_i}{s}} \quad \textbf{(34)}$$

In order to test the performance of the current-mode real/reactive-power control model of Figure 7, the control schemes of Figure 8 and Figure 9 were tested in MATLAB. An integration technique was necessary for the implementation of the differential equations in MATLAB. Thus, it was chosen the trapezoidal rule:

$$\int_{t-\Delta t}^{t} \boldsymbol{y(t)\,dt} = \frac{\boldsymbol{y(t) + y(t - \Delta t)}}{\boldsymbol{2}}\boldsymbol{\Delta t} \quad \textbf{(35)}$$

The transfer function of the PLL, (28) was integrated by (35) and the result was three different equations:

$$w_{a1}(s) = V_{sq}(s)\left(\frac{s^2 + 2s\frac{p}{\alpha} + \left(\frac{p}{\alpha}\right)^2}{s^2 + 2sp + p^2}\right) \quad \textbf{(36)}$$

$$w_{a2}(s) = w_{a1}(s)\left(\frac{s^2 + 4w_0^2}{s^2 + 4sw_0 + 4w_0^2}\right) \quad \textbf{(37)}$$

$$w_a(s) = w_{a2}(s)\frac{h_r}{V}\frac{1}{s} \quad \textbf{(38)}$$

By writing (34) as (36):

$$\frac{d}{dt}\left(u_d(t) - k_p e_d(t)\right) = k_i e_d(t) \quad \textbf{(36)}$$

It was possible to apply the trapezoidal rule. By integrating the equations of Figure 9, the current control scheme was simulated in MATLAB

IV – RESULTS

1) PLL

In order to analyze the behavior of the PLL compensator, it was simulated its response to a voltage unbalance. The input of the PLL was considered to be the three-phase V_{sabc}.(23), (24), (25) Initially, $\omega_0=2\pi x50$ rad/s, $k_1=0$, $\Theta_0=\pi/3$ rad and Vs=400V. As the constant k_1 is zero, V_{sabc} represents a balanced voltage and the PLL is in steady state. At about t=0.3s the AC system voltage becomes unbalanced, as V_s and k_1 undergo step changes, from 400V to 260V, and from 0 to 0.1, respectively. At approximately t=0.125s the system returns to its initial balanced condition.

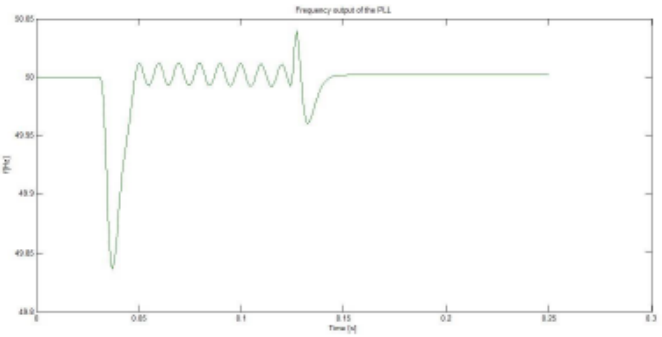

Figure 10- PLL response of the frequency

Figure 11 illustrates the output of the PLL, V_{sd} and V_{sq}. As can be seen, initially the system is balanced and consequently $V_{sq}=0$ and $V_{sd}=V_s=400V$. When the system suffers a sudden voltage imbalance at about t=0.03s, V_{sd} changes to 260V. The compensator H(s) acts upon the dq-frame frequency unbalance, so as expected V_{sq} transiently changes to zero. At t=0.125s the system becomes balanced again with Vs=400V. The PLL again maintains the system at steady-state operating conditions, with $V_{sq}=0$ and $V_{sd}=V_s=400V$.

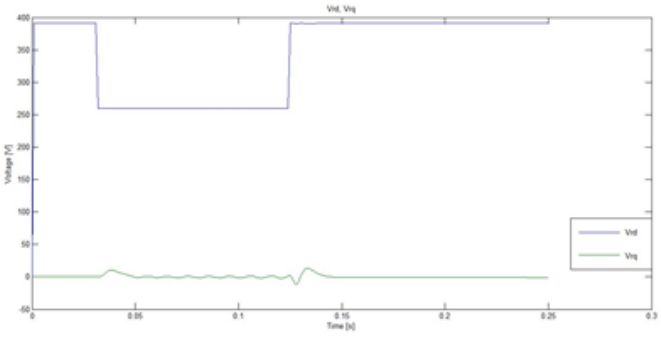

Figure 11- PLL- Voltage output (Vsd and Vsq)

2) Power Control

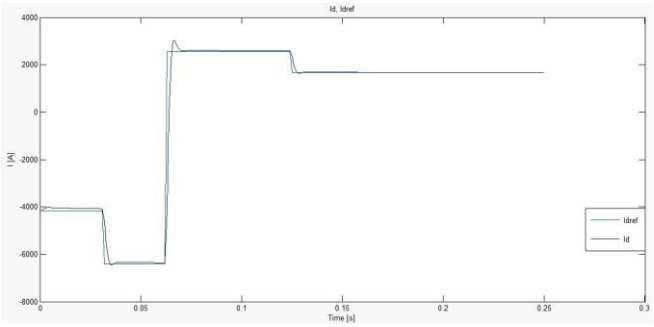

Figure 12- Id and Idref response

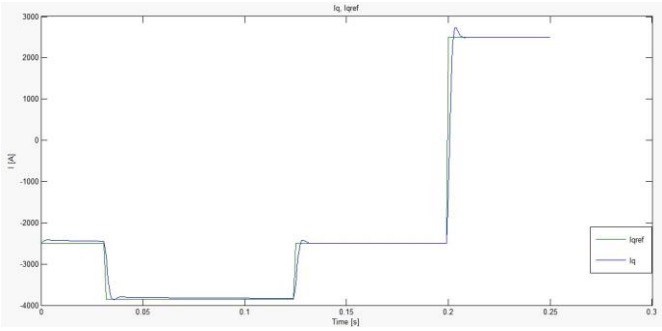

Figure 13- Iq and Iqref response

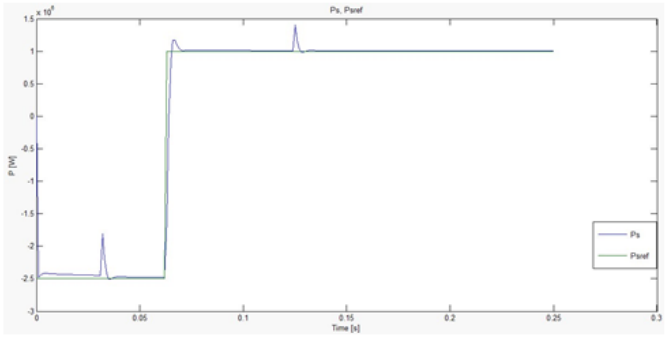

Figure 14- Ps response

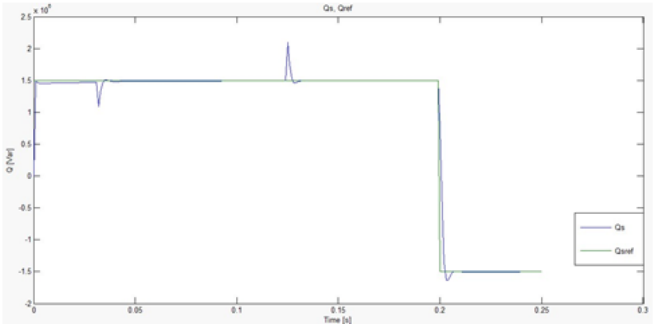

Figure 15- Qs response

Initially the PLL was in its steady state, with V=400V, the P_{sref}=-2.5MW and Q_{sref}=1.5 MW. Then the system was subjected to the following sequence of events: at t=0.0.625s P_{sref} is subjected to a step change from -2.5 to 1MW. At t=0.2s, Q_{sref} is subjected to a step change from 1.5 to -1.5 MVar. Additionally, as seen in Figure 11, at t=0.03s V_{sd} changes to 260V and at t=0.125s it returns to its original value, 400V.

From Figure 12 and Figure 13 it is possible to observe that the current control of id and iq is successfully achieved: the current controller transiently changes the current values accordingly, when either the voltage or power steps occur at the PCC. As a result, Figure 14 and Figure 15 show that the PCS effectively tracks the both real and reactive power. Also, as can be seen, this control is done independently.

V- BESS MODEL SIMULATION

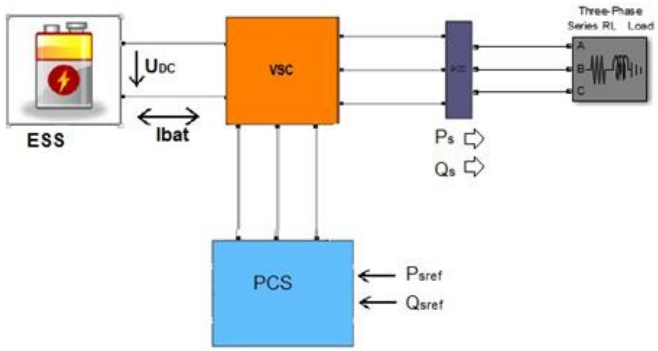

Figure 16- BESS Model with PCS modelled and Battery Model

The model of the BESS represented in Figure 16 is composed by a storage system, a VSC system and a PCS. The model is connected at the PCC with a RL load.

The model of the battery used is the one modeled in the previous thesis work, represented in Figure 17.

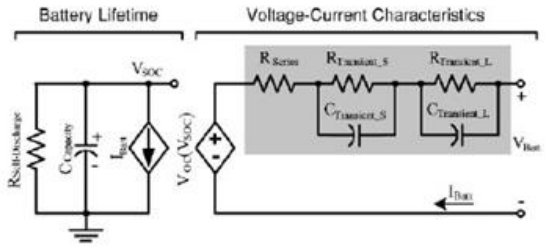

Figure 17- Battery Electric Model [6]

It was considered a battery with a capacity of 2A.h, that is, a battery whose total charge can continuously feed a load with a current of 2A during an hour. In order to increase the capacity of the battery storage system, it was considered a string of 100 batteries connected in series. Thus, the total capacity of the Energy Storage System was 200A.h. The SOC of the ESS is proportional to the DC current that flows between the VSC and the ESS, I_{bat}. If I_{bat}>0, the batteries is discharging, the SOC of the ESS decreases.

If I_{bat}<0, the current flows to the batteries, so the SOC of the ESS increases. It was considered a battery that can be fully charged, and whose charge can't be lower than 20%, that is, the maximum SOC value of the ESS is 1 and the minimum SOC value is 0.2. The DC voltage at the output of each battery is 12V. Thus, the DC voltage at the output of the ESS, U_{DC} is 1200V.

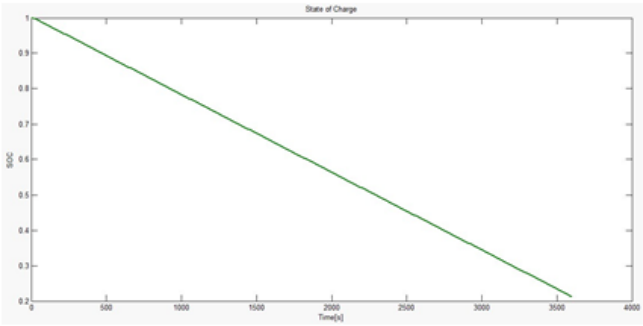

Figure 18. Battery discharging

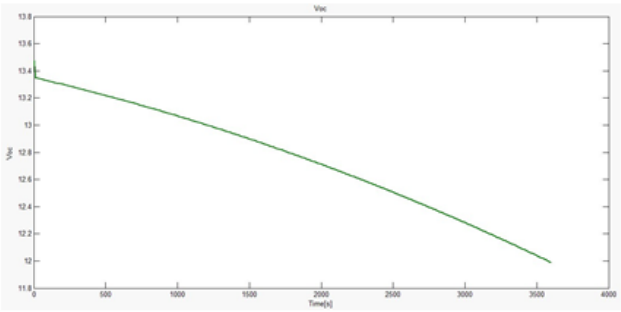

Figure 19- Evolution of the Open Circuit Voltage

VII- CONCLUSIONS

In this dissertation it was developed a model of a Power Conversion System (PCS) for Energy Stability Studies. Additionally, the model was tested to interface a battery modelled in a previous thesis work with an AC load.

The PCS can seriously impact the performance and lifetime of a BESS. Thus, this thesis focused on modeling a Power Conversion System for BESS applications.

The proposed model was based on the control of a two-level three-phase half-bridge converter, using the current-control mode in dq-frame of the real and reactive power.

It was designed successfully a PLL compensator to eliminate the effect that unbalanced voltages may have had in the performance of the PCS, creating the necessary conditions for the implementation of the current-mode control in dq-frame.

With the integration in MATLAB of the equations of current-mode control in dq-frame it was possible to validate the PCS model equations deduced. It was concluded that the model permits the separate control of active and reactive power.

Then, the PCS model was used to interface a battery modelled in a previous thesis work with an AC load. From simulations with two different RL loads it was possible to conclude that the PCS modelled can effectively interface a DC storage system with an AC load, by discharging the battery system (Figure 17 and Figure 18).

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