Analog to Digital CMOS Converter for Wireles BLE Sensors.

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***Abstract*—This work details the design and implementation of an Incremental Delta-Sigma ADC for the purpose of converting the output signal of a temperature sensor with a precision of 0.25^{o}C. The conversion range specified for the ADC is from -40^{o}C to 80^{o}C. The chosen architecture is that of a second-order Incremental ADC with a third order Sinc filter (Sinc^3) that computes the Modulator output into a 11-bit word. The Integration process is accomplished with switch capacitor circuits and two different Current Mirror Operational Transconductance Amplifiers (CM-OTA). The Converter takes advantage of the sensor output signals to attain a Vref signal. This feature makes the ADC specially designed for this purpose. The final simulations unveil that the ADC precision slightly increases when the temperature read by the sensor rises, starting at 0.3^{o}C and ending at 0.15^{o}C. The ADC has an ENOB of 10.97 bits, a power consumption of 3.17 μW and an implementation area of 0.049 mm^2 (Modulator) and 0.01 mm^2 (Decimation Filter).**

***Index Terms*—ADC, Sigma-Delta, Incremental, low-power, high-resolution.**

I. Introduction

THE Internet of Things (IoT) is a network that has taken over everyday life, and as such, the technology that supports it is in high demand. This work describes the complete design of an Analog-to-Digital converter (ADC), to be implemented in a Bluetooth Low-energy (BLE) Chip, meant to convert an analog voltage produced by a temperature sensor to a digital word.

A. Motivation

Nowadays, with the automation of everyday tasks, sensors and wireless transmitters/receivers have a major role in society and everyday life. The bluetooth transmitters/receivers have an important role to play in the IoT. With so much information being sent and received, there is an important need of ADCs with specific characteristics for selected purposes. In a world where power consumption is ever more important, projecting and designing an ADC with ultra-low power consumption and high resolution is an opportunity to be involved in high-end technology development.

Although the already implemented ADC has a good power consumption, its accuracy has to be improved, and as expected, the power consumption will rise due to a higher resolution. The existing ADC in the SoC was designed with a Successive Approximation Register (SAR) structure. The major objective of this work is to increase the resolution of the ADC designed in [1], with a focus on power consumption. The SAR ADC was designed to have a 10-bit resolution, but only an 8-bit ENOB was reached.

B. Specifications

The ADC resolution needs to be higher than that of the already existing ADC in the Chip, [1], this will lead to an increase in the reading precision of the temperature. The ADC temperature conversion range is from -40 ^{o}C to 80 ^{o}C.

The ADC will be incorporated in a SoC that already exists. This SoC will bring some restrictions to this work. It has a supply voltage of 1.2V with a tolerance of $\pm$5%. The available clock frequency is 16MHz, which will restrict the sampling frequency, through a succession of simple frequency. As an initial specification for this ADC area, the same area used in [1] is considered, which is approximately $200\mu m$x$200\mu m$.

The targeted ADC precision is 0.25^{o}C and, by using (2), the ADC has to deliver an accuracy of 11.2 bits (conversion range of 600^{o}C). A better explanation of the ENOB calculation is made in Section III-A. The conversion speed is going to be kept under 10ms. The targeted maximum for power consumption is 10 μW.

C. Work Structure

In Section II a simple study of the typical ADC structures is given, in order to justify the choice of an Incremental $\Delta\Sigma$ ADC (IADC). This structure is explained in some detail, as well as some traditional techniques used to improve it. In Section III a systemic study is made for the ADC, in order to establish goals and specifications for the ADC structure. In Section IV the ADC design at CMOS level is described. In Section V the Decimation filter implementation is described and the final step for the project, Layout implementation, is presented. Finally, in Section VI, the final results are presented and commented upon and a proposition of Future work is given.

II. State of the Art

This Section presents a small study on the background of ADCs, deciding on which architecture to use in this work, and developing a more profound study on the chosen architecture.

A. ADC Architecture

There are several existing architectures for ADCs, they can be roughly divided into two big groups, fast and high-resolution, achieving both characteristics, comes with a cost of higher power consumption and implementation area.

The Flash ADC is not only used as a stand alone ADC, but also commonly used inside some architectures. The simple FLASH ADC obtains the output digital word with a specific number of comparators. The number of reference voltages (or comparators) is determined by the Flash ADC resolution. In order to achieve N bits resolution, $2^N - 1$ comparison blocks are required (in a simple FLASH ADC).

When talking about low-power consumption, the architecture most commonly used is a successive-approximation-register (SAR) ADC (the structure used for the existing ADC in the

Chip). Although a SAR converter can be very power efficient in comparison to other structures, its resolution is limited by component mismatch. One of the SAR advantages is the high conversion rate that it can achieve, one specification that is not important for this application. One of the SAR setbacks is the fact that it uses a significant number of capacitors and the capacitor array matching requirement limits the ADC area, [2].

In comparison to the SARs, dual-slope and $\Delta\Sigma$ converters are often used in Instrumentation and Measurement (I&M) applications, due to their potential in achieving high resolution (this type of ADCs can be categorized as slow and high-resolution). The main difference between these two structures is the trade-off ratio between resolution and conversion time. In the case of a dual-slope converter, since its resolution is linearly proportional to the conversion time, high resolution is achieved by greatly sacrificing conversion rate. However the $\Delta\Sigma$ converters, using oversampling and higher-order structures, achieve that higher resolution without greatly sacrificing speed and in consequence, attain better energy efficiency than the dual-slope converters.

In instrumentation applications it's common to use a subclass of the $\Delta\Sigma$ converters, the Incremental ADC (IADC). The IADCs achieve higher resolution and its main difference between the normal $\Delta\Sigma$ converters is the block control. The IADC is not operated continuously, all its blocks have a reset signal that's activated at the end of each conversion. This characteristic permits new functionalities, such as using multi-channel input (Conversion from different sources, alternating the input signal between conversions).

Based on the comparison made between the most common ADC structures, the ADC designed in this work is an Incremental $\Delta\Sigma$ ADC, a subclass of the $\Delta\Sigma$ ADC.

B. Incremental ADC

Compared to the $\Delta\Sigma$ ADC, the IADC has a higher sample-by-sample conversion accuracy. This is accomplished by using reset signals at the end of every conversion. Between two resets the result of the conversion will be obtained at the output of a decimation filter. After a reset it's easy to change the input channel of the ADC, making this ADC capable of operating in a multi-channel mode [3].

The IADC uses $\Delta\Sigma$ modulation, which means that it uses oversampling and noise-shaping [4]. An oversampled ADC has a sampling frequency (f_s) higher than the Nyquist frequency (f_N, the sampling frequency of Nyquist-rate ADCs). This results in an oversampling ratio (OSR) of $\frac{f_s}{f_N}$. One of the advantages of using oversampling, is the requirements relaxation of the $\Delta\Sigma$ Modulator ($\Delta\Sigma$M) in comparison to Nyquist-rate ADCs.

Understanding a first order IADC (IADC1) is the first step for grasping the functionality behind higher order IADCs, or other hybrids architectures with IADCs. The basic structures of a first order IADC are the $\Delta\Sigma$ Modulator and the Decimation filter, the last block, in the simplest of cases can be a simple counter [5], as it can be viewed in Figure 1. The quantizer only compares the integration output at the end of every oversampling cycle.

The conversion is made using $\Delta\Sigma$ modulation and applying it a reset when the sample conversion is completed. The conversion time is controlled by, the number of oversampling cycles (OSR) and the sampling frequency (f_s).

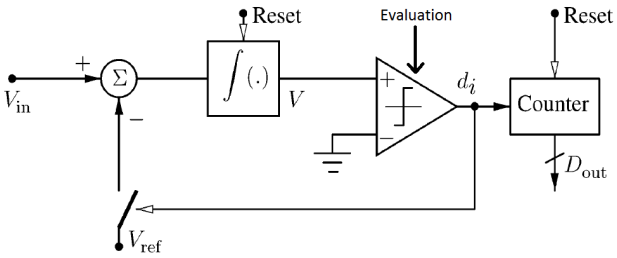


Fig. 1: Structure of a first order Incremental ADC. [5]

1) Improving the IADC: Whilst one of the bigger advantages of the first order incremental ADC is its simplicity and easy implementation, the big drawback is its conversion-rate/resolution trade-off. For a *n*-bit resolution, the conversion needs 2^n clock periods to achieve it. To surpass this drawback several measures can be taken, the most obvious one is to increase the IADC order. When the incremental ADC order is increased, it is necessary to increase also, the order of the decimation filter and the number of integrators.

There are however other techniques used to increase the resolution, that don't necessarily need an order increase. Other methods were pursued because when increasing the order, the structure has more amplifiers and scale factors, leading to a higher instability risk, [5].

To decrease the stability problem when the order of the IADC is increased, it is normal to apply the technique of multistage noise-shaping (MASH) to an IADC [6]. MASH is a technique that consists in dividing the ADC into different stages, using the quantization error of the previous stage as the input of the next stage, dividing the conversion into two or more steps.

C. Conclusion

The bigger factor that affects the design process is the ADC application. Some of te more advanced techniques used to improve the IADC aren't designed to convert a differential signal with the same specifications as this temperature sensor output signal. Every application is different, and this ADC specifications are the main constraints on its design. Another factor to take into account is the absence of a reference voltage. The external generation of a reliable reference voltage causes a consumption problem. The approach taken in this ADC structure design is to develop a second order IADC that has the capability to create a reference voltage while taking advantage of the input signals. This also means that there is no present reference voltage source.

III. Systemic Study

In this Section the overall temperature sensor and its implications on the ADC design are further explained. The ADC topology and its blocks are designed at a black-box level, justifying their specifications.

A. Temperature Sensor

A simplified version of the sensor used for reading the temperature is shown in Figure 2.

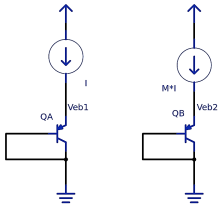


Fig. 2: Simplified structure of the temperature sensor used.

Both PNP transistors have the same dimensions, the *ratiometric* measurement is accomplished by a difference in the current passing through them and not in their size, mainly because dynamic element matching (DEM) is more easily applied in the current. The first current source has a value five times smaller than the second, creating a difference between both V_{EB} signals ($\Delta V_{EB} = V_{EB2} - V_{EB1}$). The signal ΔV_{EB} reacts linearly to the absolute change in temperature, as it can be seen in Figure 3.

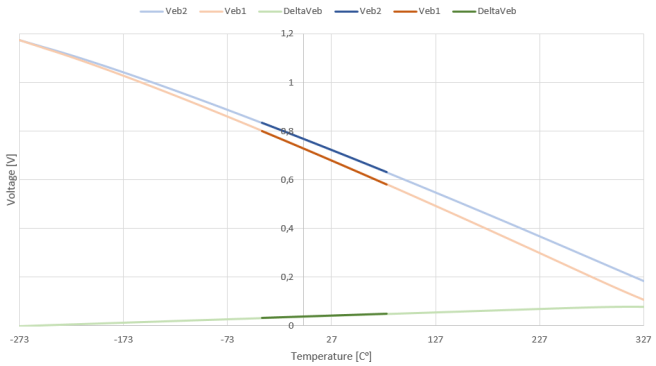


Fig. 3: Temperature sensor behaviour through, the whole temperature scope (light colours), and the desired scope (darker colours).

The signal ΔV_{EB} is differential and is the actual input sent to the converter, which must have mechanisms to prepare the signal for conversion. One way to obtain a reference voltage is to use both $\alpha * \Delta V_{BE}$ and V_{EB2}. The α value is what determines the stability of the reference voltage (1).

$$Vref = \alpha * \Delta V_{EB} + V_{EB2} = V_{PTAT} + V_{EB2} \quad (1)$$

The Sensor is not capable of adjusting its reading range, which means that, despite the desired conversion range, the signal V_{PTAT} is linear roughly in a 600 degree range. The signal sent to the ADC is prepared to be converted from -273^{o}C to 327^{o}C (0K to 600K), this means that the ADC accuracy is determined by the desired precision of the temperature reading. Equation (2) is used to calculate the target ENOB for an ADC at the output of the described sensor.

$$ENOB = \log_2 \frac{600}{Precision} \quad (2)$$

B. V_{PTAT} and $Vref$

The signal V_{PTAT} is achieved by subtracting V_{EB1} to V_{EB2} and multiplying the result by the factor α. Through simulations the best value for α is 12, because its $Vref$ variance is the smallest one. The α value could be further improved, but by using decimals to define α it would not be possible to implement Dynamic Element Matching (DEM), leaving α more vulnerable to mismatch.

The sensor has the ability to send several different combinations of the V_{EB} signals, the ones used by the ADC are ΔV_{EB} and $-V_{EB2}$. The V_{PTAT} signal (**??**), is achieved by multiplying the ΔV_{EB} signal by α. The $Vref$ signal is achieved by integrating $-V_{EB2}$ instead of $V_{PTAT} - Vref$. The system that multiplies the input signal uses the switched-capacitor circuitry and ratio between the input capacitors (C_i) to achieve it. Figure 4 illustrates, for single-ended integrators, the mechanism used t achieve V_{PTAT} and $Vref$.

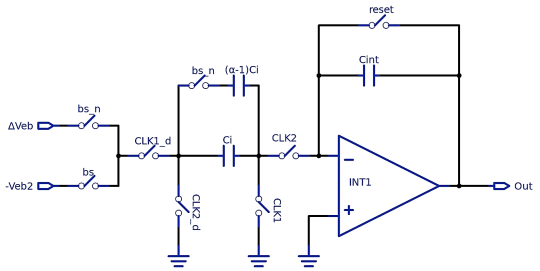


Fig. 4: Structure of the mechanism that creates V_{PTAT} and $Vref$.

When $bs =' 1'$ the integration has a gain of $\frac{Ci}{Cint_1}$, but when $bs =' 0'$ the integration has a gain of $\frac{\alpha * Ci}{Cint_1}$, α times bigger than the first case. The bs signal is the IADC comparator output bit that activates the subtraction of $Vref$ input signal. The modulation done by this IADC is the same as the one done in a normal IADC, except that in this IADC no $Vref$ signal is present.

This $Vref$ implementation has one negative implication, certain structure variations normally used in the IADC have a more challenging implementation, since the Vref signal isn't constantly available. The ADC input signals can be consulted in (3).

$$\Delta V_{in} = \begin{cases} V_{EB2} - V_{EB1} & , bs = 0 \\ 0 - V_{EB2} & , bs = 1 \end{cases} \quad (3)$$

C. IADC Topology

The ADC is a second order incremental Delta-Sigma (IADC2). The first order wasn't implemented due to its poor trade-off between speed and precision, while the third order was ignored due to its higher vulnerability to become unstable. The ADC can either be built in a Feed-Back(FB), a Feed-Forward(FF) topology or built using characteristics from both. Only the Cascade of Integrators with Feed-Forward (CIFF) and Cascade of Integrators with distributed Feed-Back (CIFB) topologies were considered, since the other options (Cascade of Resonators with Feed-Forward, CRFF, and the Cascade of Resonators with distributed Feed-Back, CRFB) were eliminated due to implementation difficulties.

Both topologies have a feed-forward path from the input signal to the quantizer, which has implementation difficulties. The necessity of that feed-forward path was studied in [7], and with systemic simulations no improvement in the temperature conversion accuracy was found. Simulations with [8] showed

no improvement in the ADC Noise Transfer Function (NTF). The decimation filter implemented also helps to balance the non-existence of this feed-forward path, since the only benefit of such a path is a faithful conversion on the early cycles.

Both structures (CIFB and CIFF) are compared in [7], through simulations, in order to understand what other features differentiate them. It was concluded that in the case of temperature conversion, the major difference between the structures resides in the implementation practicality. The Feed-Back path difficulties on the CIFB are avoidable by choosing the CIFF topology. The ADC topology used is presented in Figure 5.

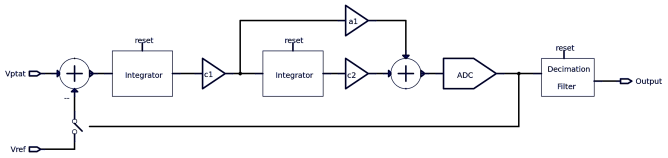


Fig. 5: Delta-Sigma Topology used for the ADC.

The loop coefficients have to be chosen so that the amplifiers output swing voltages are not violated. In a systemic simulation the amplifiers output voltages are not limited but in a normal amplifier, the output voltage is delimited by the output swing which depend on the number of MOS in the amplifiers last stage. The values that contain the amplifiers output inside their respective output swing are $c_1 = 1/3$ and $c_2 = 1$.

Using the same simplification methods used in [5] for a third order modulator, the equation that defines the ADC OSR is presented in (4).

$$OSR = 2^{\frac{n_{bit}+1-log_2(c_1 c_2)}{2}} \tag{4}$$

As it is specified in Section III-H, the Filter used is a third order Sinc filter (Sinc^3), which means that, due to implementation details, the OSR has to be dividable by three. The resulting OSR value of the equation is 118.8, so the value used for OSR is 120.

D. Implementation details

The ADC is not implemented with single-ended amplifiers since, the Chip does not have symmetrical voltage supply. The ADC is implemented in a fully-differential mode of operations. Since the ADC is implemented with FD circuits, the output swing is doubled and the common mode noise rejection is higher [9].

The common-mode voltage (VCM) is a voltage value generated in the ADC. It's value represents the reference voltage in a differential structure. Since this ADC does not have symmetrical voltage supply (only 1.2V and ground) the common-mode voltage (VCM) has to be generated (in case of symmetrical voltage supply the VCM is the ground, 0V).

In order to have a more simple circuit and less area usage, the ADC will be implemented with a 1-Level quantizer, which can be built by a simple single-ended comparator. The comparator function is to check the output of both integrators and accordingly check if the condition (5)

$$2 * V_{int1} + V_{int2} > V_{reference} \quad \equiv \quad \Delta V_{int1} + \frac{\Delta V_{int2}}{2} > 0 \tag{5}$$

E. Sensor design Adaptation

Although the objective of this thesis is the ADC design, the sensor front-end generates the ADC input signal whose behaviour will influence the ADC specifications. A simple schematic for the sensor presented in Figure 6, where the necessary modifications were made for working synchronized with the ADC.

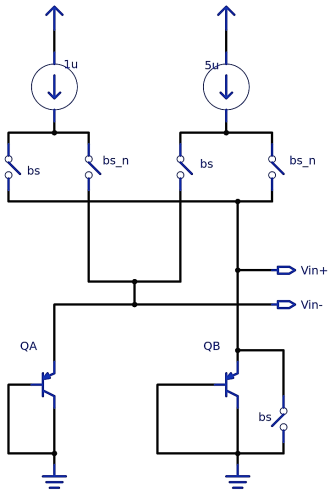


Fig. 6: Schematic of the temperature sensor front-end used for the ADC simulation.

The mechanism displayed in Figure 6 creates the ADC input voltage by manipulating the current that passes through both bipolar transistors, or by shorting one of the transistors.

F. Clock Generation

The ADC has an available clock of 16 MHz. With that signal the clock generation block creates all the control signals for the ADC. The ADC has an OSR of 120, but the conversion time is not only influenced by the OSR and sampling frequency. The OSR value and the sampling frequency only represent the time that the ADC analog blocks are working. After the 120 sampling cycles pass, the analog blocks are reset and only the digital filter is working. Only after the digital filter finishes, is the digital output ready. Since the conversion time is limited to 10 ms, the sampling frequency is calculated with a time limit of 5ms (to take into account the extra time the decimation uses). Assuming that the analog blocks can't operate for more than 5ms, the sampling frequency has the condition expressed in (6).

$$T_{conv} < \frac{OSR}{f_s} \quad \rightarrow \quad f_s > \frac{OSR}{T_{conv}} = 24kHz \tag{6}$$

The sampling frequency has to be grater than 24 kHz. By using 9 frequency dividers a signal of 31.25kHz with a duty cycle of 0.5 is created. From this signal, two main control signals are created, CLK1 and CLK2. The clock signals that control the ADC are presented in Figure 7.

One of the most important features of the clock signals is their non-overlapping characteristic, like displayed in Figure 7. Another aspect to take into account when dimensioning the non-overlapping interval is the existence of delayed signals. These signals cannot overlap their "counter-phase" not delayed signals, e.g. CLK1_d cannot overlap CLK2.

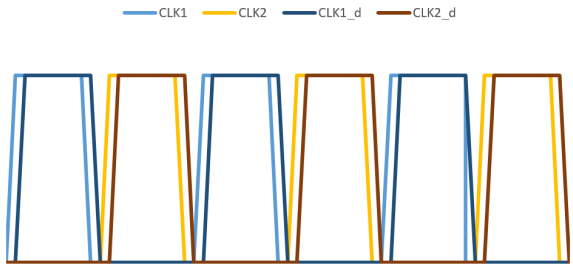


Fig. 7: Non-overlapping clock signals and their delayed counterparts.

The ADC has implemented other control signals, for example two power-down signals, a digital and an analog (the ADC operates in a one-shot operation mode where it turns it self down after a conversion), two reset signals, one for the start and another for the conclusion of the conversion and an evaluation signal, used in the comparator. The ADC also receives an Wake-up signal that asks for a conversion.

G. Integrators

The amplifiers used in the integration process are the most power hungry blocks in an IADC. The DC gain specification for both amplifiers to use in this work are obtained through systemic simulations, studying the DC gain limits so that the ADC precision would not drop bellow 0.25^{o}C. The specifications for both amplifiers are displayed on Table I.

Amplifier	DC gain	BW	PM	V_{offset}
First	>72dB	>62.5kHz	>70^o	<2mV
Second	>60dB			-

TABLE I: Specifications of both amplifiers in the ADC.

The second amplifier has a much lower DC gain specification than the first because the most important integration is the one done by the first amplifier. This happens because an error done in the first conversion will lead to errors in two evaluations operated by the comparator, the current one (output of INT1) and the next evaluation (output of INT2). An error occurred in the second integration only influences the current evaluation.

The amplifiers input offset voltage (V_{off}) is affected by several factors in the ADC, but the main factor are the amplifiers themselves. The V_{off} is the differential input voltage that produces an output voltage of zero. The technique used to mitigate the amplifiers offset voltage is Chopping (possible to apply due to the use of FD amplifiers). This technique chops the amplifiers outputs and inputs for half of the conversion time (it can be triggered "on" and "off" as frequently as possible, but to be effective it has to be "on" during half of the conversion). Chopping is only applied to the first amplifier. Since Chopping is applied every oversampling cycle, the frequency chosen for its control signal mechanism is 15625Hz.

H. Decimation Filter

The decimation filter is responsible for computing the bit-stream into the digital output word composed of 11 bits. The are several possible topologies that can be used for the decimation filter, but normally only two are usually used in IADCs, the FIR filter and a Sinc^L filter. Both topologies require a decimation block at the output.

The sample weight is very important in the Filter design, by using a symmetric triangular filter the Copping error mitigation is unaffected. The most commonly used filter for the IADC is the Sinc^L decimation filter. It is custom to use a Sinc filter one order higher than the modulator [10]. Frequency response of four Sinc^L decimation filters can be viewed on Figure 8.

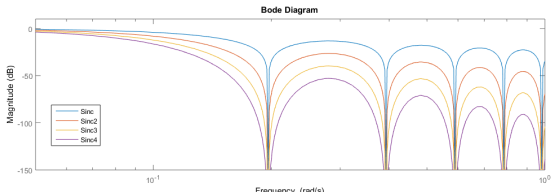


Fig. 8: Frequency response of the Sinc Decimation Filter from the first to the fourth order.

As it can be seen, with order increase the transition band becomes more steep and a higher attenuation is achieved. The filter implemented in this work is a Sinc^3, which has a symmetric characteristic. The structure of the Sinc^3 implemented in the ADC is presented in Figure 9.

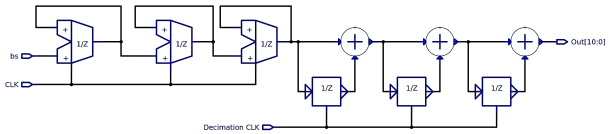


Fig. 9: Sinc^3 Decimation Filter.

The Decimation clock signal presented in Figure 9, is a signal that activates the Z^{-1} blocks every $\frac{OSR}{3}$ sampling cycles. By implementing the filter this way, the digital output is ready $\frac{5.OSR}{3}$ conversion cycles after the conversion starts. The filter implementation details are explained in Section V-A.

IV. Schematic Design

In this Section the ADC blocks design at schematic level is described.

A. Amplifiers

The amplifier choice for the integrator is a crucial step. The amplifiers do not affect only the area and the power consumption, their DC gain highly affects the ADC precision. Another factor to take into consideration for the amplifiers is the voltage output range. The amplifiers have a limited range for the output voltage (output swing), thus the capacitors dimensioning (loop coefficients) is influenced by the output voltage range.

Despite the difference in specifications, the same main topology is used in both integrators, since using the same topology allows an output swing centred in the same value. Due to having a high input and output impedances, and a potentially high transconductance, the operational transconductance amplifier (OTA) is the best type of amplifier to implement in a SC circuit, [11].

There are several structures that could be taken into account, but some environment features narrow the choice. The desired

features for the OTAs are two stages (to implement different reference voltages in its input and output) and no more than 4 CMOS levels at the second stage. The chosen OTA is the Current Mirror OTA (CM-OTA), and two variations are used. The simple CM-OTA can be consulted in Figure 10 and is the topology used for the second amplifier.

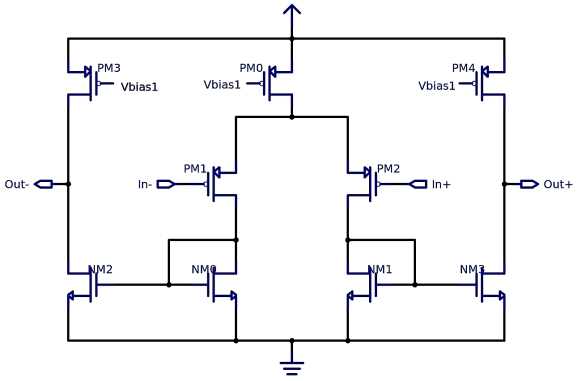


Fig. 10: Simple Current Mirror OTA topology.

Since the simple CM-OTA could not reach the desired DC gain for the first amplifier, a more complex structure is used. The first OTA can be viewed in Figure 11.

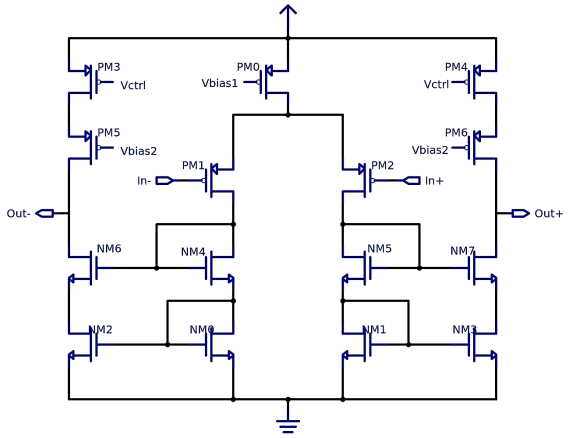
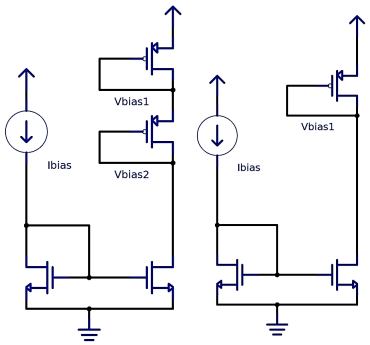


Fig. 11: High DC gain Current Mirror OTA topology.

One of the setbacks of using a more complexed structure is the extra current consumption needed to maintain the Bandwidth and PM values and the smaller output swing. Since the first amplifier has a smaller output swing, the VCM is calculated having it in mind. The chosen value for the VCM is 500mV.

The biasing circuit used for the first and second amplifiers is displayed in Figure 12. The circuit that biases the first amplifier receives a reference current of 100nA, while the second biasing circuit receives a current of 50nA.

The first amplifier, on contrary to the second, is designed with a different input VCM, this means that for the first charge injection mechanism the common mode voltage used is different than the one used at the input of the second amplifier and comparator. This measure is implemented because the bigger capacitors in the ADC are used at its input, and by implementing a VCM with a value closer to the input signals in the first charge injection, the capacitor charge is more relaxed. A VCM



(a) (b)

Fig. 12: Biasing circuit for the amplifiers. a) First amplifier. b) Second amplifier.

of 700mV at the input charge injection, means that less current has to be used to charge up the capacitors. The first and second amplifiers nominal specifications are presented in Table II.

OTA	DC gain	BW[Hz]	PM	I_{total}	I_{bias}	δV_{Outmax}
1st	84dB	70.5k	62^0	1.8μA	100nA	600mV
2nd	59.76dB	102k	69^0	380nA	50nA	800mV

TABLE II: Nominal specifications for the first and second amplifiers.

The Common Mode Feed Back (CMFB) is one of the most crucial parts of a fully differential amplifier. Its purpose is to maintain the bias points of the output voltages at the desired value, even under fabrication dispersion and temperature variations. For the CMFB to work properly, it will need a common mode voltage, which will be generated by a reference voltage generator (Section IV-D). The circuit used for the CMFB is presented in Figure 13.

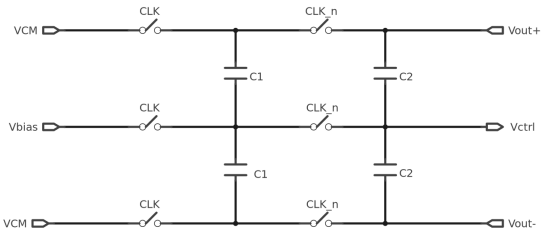


Fig. 13: Common Mode Feedback for switched-capacitor amplifiers.

The CMFB compares the mean value of the amplifier output signals to the reference voltage (VCM), and according to that comparison, the V_{ctrl} value changes around the Vbias value. The amplifiers output average value is obtained through the C2 capacitors. The switched-capacitors, C1, are responsible for the V_{ctrl} generation, by constantly distributing the charge between themselves and the C2 capacitors.

B. Capacitors and DEM

The ADC has many capacitors, while most of them are matched in pairs, the 24 input capacitors (C_i) are matched in

groups of 12. In order to make the ADC more robust in face of these capacitors mismatch, DEM must be applied.

1) Input capacitors DEM: The capacitors are responsible for several ratios, but the most important one is the α factor, which is responsible for the generation of a stable reference value. The relation between the capacitance integrated when $bs = 1$ must be exactly $\frac{1}{12}$ of the capacitance integrated when $bs = 0$.

A way to prevent the α factor to change due to mismatch between the capacitors is to use 12 isolated capacitors (for each input path), and when only one of them is needed ($bs = 1$), the capacitor used for the charge injection alternates. The twelve switches used for each capacitor are commanded by the bit stream signal and by a state machine. When $bs = 0$ all the switches are closed, if $bs = 1$, the state machine controls which switch is closed.

The solution used to create the state machine is a counter capable of counting up to 12, and triggered by the rising edge of the control signal (the output signal of an AND gate that has at the input CLK1 and bs). Each state is represented by a logic gate that has 5 inputs, bs and the counter outputs.

2) Chopping: Chopping is a technique already described before, its main purpose is to mitigate the errors provoked by the amplifiers offset voltage. The chopping block is built with four switches and is displayed in Figure 14.

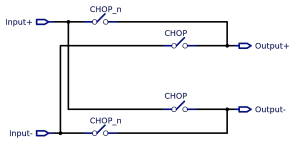


Fig. 14: Chopping mechanism used in the ADC.

The Chopping blocks are only implemented in the first integration, as it is explained and justified in Section III-G. When chopping the inputs and outputs of amplifiers, it's necessary to make sure that the differential information is passed on correctly, since the only voltage that's meant to be inverted is the input offset voltage. The points where chopping is applied in the ADC are indicated in Figure 15.

The delayed signals exist so that the amplifier input chopping switches are opened slightly before than the output switches. This delaying technique reduces the output switches signal-dependant charge injection, [12].

C. Clock Generation

The non-overlapping clocks are generated through two delay blocks and two logic gates. The delay blocks are built with a cascade of buffers (each buffer is composed by two inverters in cascade). The propagation time of each buffer defines its delay time. The number of delay buffers and their components dimensions are the essential features to design in order to obtain the desired non-overlapping interval. Figure 16 displays the circuit used for generating the non-overlapping clock signals.

Two more delay blocks are used to generate CLK1_d and CLK2_d, the delay generated by these blocks is considerably smaller than the one caused by the ones presented in Figure 16.

D. Common Mode Voltages Generator

As it was explained in Section IV-A, two VCM are necessary, one of 700mV and a second of 500mV. The simpler way to generate the two signals is to use voltage dividers. Instead of using one voltage divider circuit to obtain both VCM signals, two dividers are used. The first divider (700mV) is only connected to the capacitors C_i while the second divider is connected to all the other SC circuits in the ADC. The use of two dividers allows for a better VCM generation since the noise from one VCM doesn't affect the other. There are several options for the VCM generation, but the chosen topology is the one presented in Figure 17.

The divider presented in Figure 17 is built with CMOS components, connected in a way that they behave like diodes. This is achieved by shorting the drain with the gate. The voltage division can be controlled by the number of components used and their dimensions. The more components used, less current will be consumed by the divider.

Each voltage division must have a current higher than a certain threshold so that it can preform the division without being largely affected by the SC circuits. Certain fluctuations are allowed, since CMN is mitigated in a FD circuit. The minimum current for the first division (700mV) is 300nA and for the second (500mV) is 25nA. The first division has a much higher current budget, since the input SC charge injection mechanisms works with a load of 30pF, while the second division has a load of only 3.35pF.

By using two different circuit for both voltages, a more precise voltage can be obtained, since if only one circuit was used, the dimensioning would be more challenging and less robust. The voltage divider specifications are specified on Table III.

Spec	VCM [mV]		Current [nA]		# Components	
	1st	2nd	1st	2nd	1st	2nd
Nominal	700.1	500.8	626.1	121.5	5	6
MC Deviation	1.7	2.2	13.3	2.2		

TABLE III: Voltage Divider specifications.

E. Current Mirrors

Assuming that the ADC receives a reference current of 100 nA, this ADC needs to mirror this current into three biasing currents of 100nA, 50nA and 20nA, for the first OTA, second OTA and Comparator respectively.

Two Current Mirrors topologies were considered, the simple CM and the cascoded CM. For transistors with small dimensions the cascoded CM has a better performance, but the simple CM has a significant improvement when its components have bigger dimensions. This happens because the output impedance increases considerably, approximating the simple CM to an ideal current source. The chosen topology is that of a simple CM, and its schematic can be viewed on Figure 18.

The pMOS that's connected to MP0 gate and the supply voltage is responsible for the power down mechanism. The output currents can be consulted in Table IV.

V. Implementation

In this Section, a detailed description will be given about the most important layout techniques and the Filter implementation.

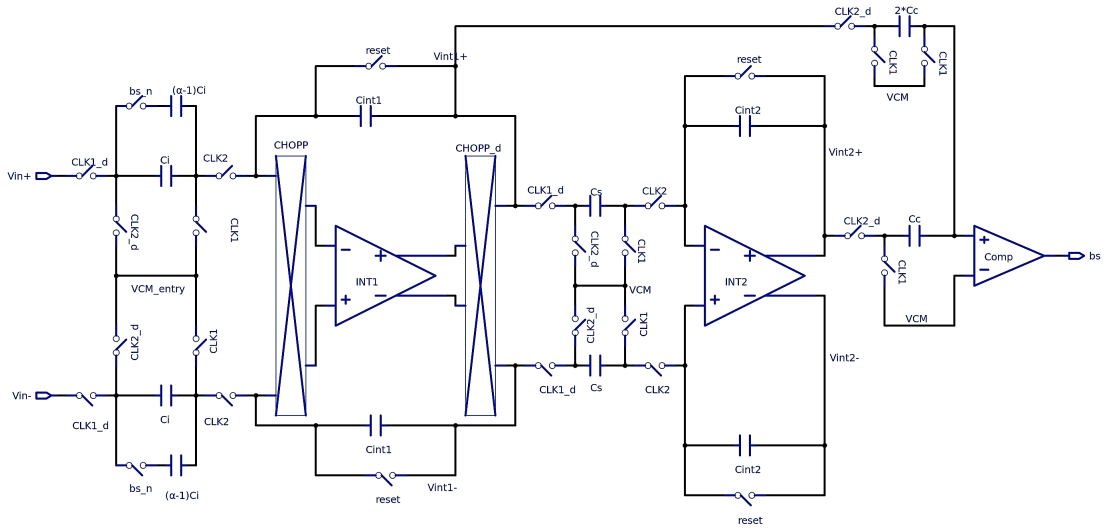


Fig. 15: Locations where the system level chopping is applied.

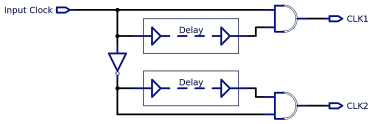


Fig. 16: Schematics for the generation of non-overlapping clocks.

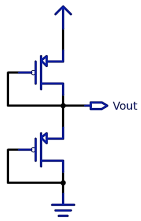


Fig. 17: Diode-connected MOS voltage divider.

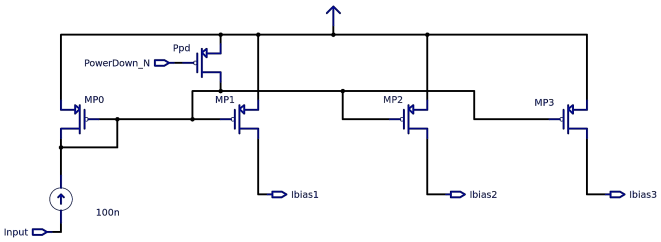


Fig. 18: Current Mirrors with power down system.

Block	1^{st} OTA	2^{nd} OTA	Comparator
Current	102.0 nA	51.1 nA	20.5 nA
MC Deviation	1.3 nA	0.902 nA	0.465 nA
Current (Power-down)	0.486 nA	244 pA	0.099 nA

TABLE IV: The output currents from the Reference current generator.

A. Decimation Filter

The Decimation Filter structure was presented in Figure 9. The implemented Verilog code is slightly based on the one described in [13]. There are several measures that reduce digital circuits power consumption that can be applied to this project [14], such as: reducing the maximum number of bits per register, reducing number of signal transitions ('1'→'0' and '0'→'1') and controlled counters (avoid operating counters when unnecessary).

The filter synthesis with technology standard cells and its layout creation was done with digital design flow tools. This layout implementation is done with "high-speed" family cells, although "low leakge" family cells would be more suitable (could lead to lower power consumption), but because of manufacturing rules the chip can only use "high-speed" cells. The design rule check was done and no violations were found. Since the worst slack time is 1886ps and the clock has a period of 32000000ps, the cells speed clearly presents no performance problem. The filter layout area is defined with approximately the same height as the ADC so that they can be implemented next to each other with no area wasted. The filter area is also defined with a predicted occupancy rate of 70%. The filter has a final implementation area of approximately 0.1 μm^2.

The filter layout is presented in the final Layout for the whole ADC in Figure 19.

B. Implementation details

Layout techniques are used to reduce the circuit vulnerability to mismatch errors. The main technique used in this work is the "Common-centroid", which is either applied in "Fingers" or in a Matrix form. These techniques can be implemented on transistors that have widths with common dividers, so that each finger has the same width (in the case of a Matrix common-centroid, the transistors must have also the same length).

1) Capacitors: The capacitors can be designed with two different structures, Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM). The chosen structure is the MOM since it's less sensitive to parasitic capacitance and occupy less area, Table V presents the ADC capacitors implementation details.

2) Current Mirrors: The reference current generator is implemented with simple techniques. Four main pMOS are used, and these components need a high robustness against

Blocks	Integration				Capacitor		CMFB			
	First		Second				First		Second	
Capacitor	Ci	C_{int1}	Cs	C_{int2}	C_{c1}	C_{c2}	C1	C2	C1	C2
# Capacitors	24	2	2	2	1	1	2	2	2	2
Area [μm^2]	913	2392	508	508	154	250	154	508	154	508
Capacitance [F]	1p	3p	500f	500f	100f	200f	100f	500f	100f	500f
After extraction [F]	1.012p	3.027p	509.6f	509.6f	104.2f	206.2f	104.2f	509.6f	104.2f	509.6f

TABLE V: Capacitor layout specifications.

mismatch. In order to achieve such vulnerability, these 4 pMOS are implemented with the "Fingers" technique.

3) Integrators: For the integrators to work properly, apart from the OTA DC gain and settling time, there are two major factors that play a major role in the integrators performance. These are the output common mode voltage, and the input offset voltage. As it was explained before (Section III-G) the first amplifier offset voltage is mitigated with Chopper stabilization, but other measures to decrease the offset voltage are implemented. Mismatch between certain components generate offset voltage. In the case of the first amplifier the input offset voltage is generated from mismatch between the following components: PM1-PM2, PM3-PM4, PM5-PM6, NM0-NM1, NM2-NM3, NM4-NM5 and NM6-NM7. In the case of the second amplifier, offset voltage is caused by mismatch between the following components: PM1-PM2, PM3-PM4, NM0-NM1 and NM2-NM3. To minimize the offset voltage, the matrix common-centroid technique is applied to all the transistor pairs described previously, and in order to ensure a higher mismatch insensitivity, the components are divided by 4.

4) Comparator: The Comparator performance is dependant on the ratio between two pairs of transistors, NM0-NM1 and PM0-PM1. Due to this fact, the implementation of both transistor pairs is done with the matrix common-centroid technique (transistors divided in 2).

C. Final Layout

The layout for the whole ADC is presented in Figure 19 (Filter included).

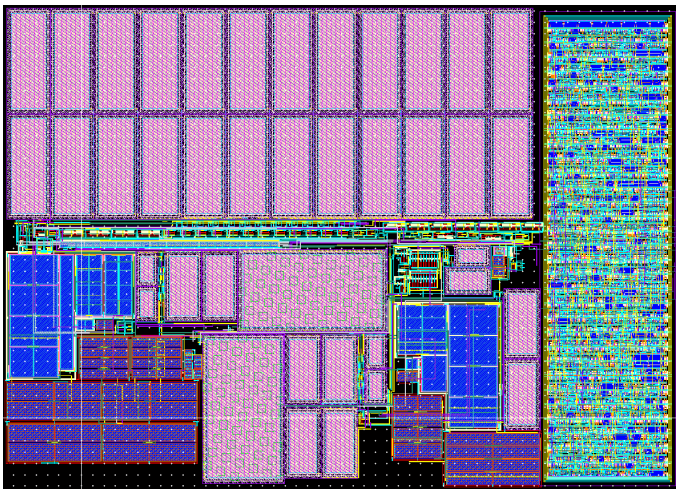


Fig. 19: Layout for the whole ADC.

The ADC blocks are highlighted in Figure 19. The Analog blocks, or modulator, have a total area of 0.49mm^2 and the Filter has an implementation area of $\approx$0.1mm^2.

VI. Conclusion

In this Chapter, the final results are presented, while a comparison is made with previous works. Future work is also proposed.

A. Results

One of the most important objectives of this work is the ADC power consumption. The Modulator and the Filter are the two main blocks that compose the ADC. Due to the difficulties in measuring the Filter power consumption accurately, the Modulator power consumption is referred to as the ADC power consumption. The conversion is divided in two stages, one where the Modulator is operating, and another where only the decimation process is in operation. In the first stage (120 Oversampling cycles) the ADC has an average power consumption of 3.17 μW, while on the second stage (80 Oversampling cycles) it consumes 0.37 μW (this is the Modulator consumption in power down mode).

The power consumption slightly increases with an extracted view simulation (from 2.9 μW to 3.17 μW), but to simplify the analysis, the power distribution study is done with a schematic simulation. The power down system creates a great power reduction in the integrators (power decrease of 99.6% for the first and 99.8% for the second), which in turn, makes the voltage division circuits the block that spends more power in the power down mode.

The conversion speed is easily calculated. The first stage is composed by 120 oversampling cycles, and the second by 80, which means that the conversion period id of 6.4ms.

One of the most important features regarding a precise temperature conversion is the ability to maintain a stable Vref signal throughout the conversion range. To verify it, the number of bits that represent a 10^{o}C increment were tested at -40^{o}C, 20^{o}C and 70^{o}C. The 10^{o}C gaps are represented at the output by a 104, 103 and 106 bit increment, respectively, which is a strong indicator of the Vref signal stability.

The ADC precision is measured with static simulations. Which means that in order to obtain the precision, several simulations were run with a small step of temperature between them. This measurement leads to an approximation of the ADC ENOB with the relation between it and the achieved precision (2), already discussed in Section III-A.

By simulating the ADC with small temperature steps (compared to the desired precision), an approximation to the ADC precision can be achieved. This procedure is done around

three temperatures, -20^{o}C, 20^{o}C and 70^{o}C. The ADC precision slightly decreases with the decrease in temperature, from 0.3^{o}C to 0.15^{o}C. For comparison purposes, the considered value for the achieved ADC precision is 0.3^{o}C. By using (2), the predicted value for the ENOB is 10.97.

B. Performance

In this section, the ADC results are compared to some recent works using specified Figures of Merit (FoM). Two FoM formulas are commonly used when comparing IADCs with low power consumption, [12], [15]–[18]. The first is the Walden FoM (FoM$_W$), and the second is the Schreier FoM (FoM$_S$). Unfortunately, since it wasn't possible to run dynamic simulations with this ADC, the Dynamic range value was not obtained, which means that only the FoM$_W$ is used, (7).

$$FoM_W = \frac{power}{2^{ENOB}.2BW} \qquad (J/conv.) \qquad (7)$$

For comparison purposes, only the modulator is considered. The works presented used external filters (for example with an FPGA), which means that regarding power consumption and implementation area, the values used for comparison are only referring to the modulator. In Table VI, the specifications for each of the ADCs can be seen and compared.

Several conclusions can be taken from Table VI. The ADC implementation area is higher than that of the other ADCs presented. A measure that reduces the ADC area is presented in Section VI-D. This ADC presents a considerably lower power consumption, this happens since the architecture is a simple IADC2 instead of a more complex pipelined or mixed architecture. The Walden FoM for this work has a higher value than the other presented ADCs, which happens due to the ADC speed. This FoM could be highly improved by implementing a faster clock (higher sampling frequency), but the ADC BW was not one of the prioritized specifications.

One of this projects advantages is that it accounts with almost all of the power consumption sources in the final implementation (in terms of the analog blocks). The other ADCs presented in this work did not specify if the generation of a stable Vref signal is accounted for, which can serve as an advantage for this work, since it does not require an external voltage source for the Vref signal.

C. Initial vs. Achieved specifications

This work was done with certain specifications in mind, which are stated in Section I-B. Table VII states the initial specifications for this work, and the achieved values by the designed ADC.

The ENOB value presented is the one achieved in the lower part of the conversion range. The ENOB value of input signals that correspond to higher temperatures, can reach up to 11.97 bits.

In terms of speed and power consumption, the ADC achieves specifications that respect this project requirements. The ENOB value is slightly lower than the initial specification, but only for lower temperatures (at 20^{o}C the ENOB is 11.55).

The only specification that is clearly broken is the implementation area. As it is explained in Section I-B, this specification is the area used by the SAR ADC implemented in the Chip. The area was limited in this way so that the ADC doesn't occupy more area than the already existing one. The presented implementation area may not present a problem for this ADC integration inside the Chip. If the ADC area poses a problem, a measure to reduce the Modulator implementation area is proposed in Section VI-D.

In conclusion, the primary objective of replacing the existing ADC with one that has a higher conversion precision is achieved. This ADC is also specially designed to work with the proposed temperature sensor, and was also tested with an ideal model of it, which can lead to a chip integration with fewer problems.

D. Future Work

The integration capacitors that belong to the first integration are the components that occupy the largest area in the ADC, and mismatch between them causes an unbalanced integration. They implemented in a way that allows for a more compact Layout. In order to improve the ADC performance, the two capacitors could be implemented with a common-centroid technique. This would reduce the ADC vulnerability to these capacitors spacial dispersion, but it would definitely increase the ADC implementation area and require its layout re-design.

As it was mentioned in the previous Section, the ADC area can be reduced by applying a technique described in [10]. When $bs = 1$ only 2 capacitors are used at the input, and when $bs = 0$ all 24 capacitors are used. In order to use half of the 24 capacitors, the integration when $bs = 0$ would be done in two steps. Instead of integrating all the 24 capacitors at the same time, two cycles would be used, integrating 12 capacitors at a time.

The system that controls the clock signals would have to be changed, and not to redesign the amplifiers, the conversion time would rise to double its present value. All the clock signals that control the ADC SC circuits had to be able to produce two different frequencies, one for $bs = 0$ and another for $bs = 1$. The area could be reduced as much as $10957\mu m^2$ (ignoring the additional control circuits). The final layout could have an implementation area of $\approx$0.48mm^2 (filter included).

If the Chip needs a higher precision reading, the easiest plan to implement is to increase the OSR (modify the final reset signal generation and the filter accordingly) and, if necessary, increase the number of bits per register (output included) in the Decimation filter.

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Work	CT-IADC [15]	IADC1 hybrid [16]	Two-step IADC2 [12]	Zoom ADC [17]	Self-Timed IΔΣADC [18]	This work
Year	2015	2014	2015	2013	2012	2017
Architecture	Pipelined IADC	EC-ADC	IADC2 + IADC1	SAR + IADC	ZCB-IADC	IADC2
Technology	0.18 μm	0.18 μm	65 nm	0.16 μm	0.16 μm	0.13 μm
Area	$0.337mm^2$	$0.038mm^2$	$0.4mm^2$	$0.375mm^2$	$0.45mm^2$	$0.49mm^2$
V_{DD}	1.2/1.8 V	1.8 V	1.2 V	1.8 V	1 V	1.2 V
f_s	8 kHz	-	96 kHz	50 kHz	-	31.25 kHz
OSR	40	32 (1^{st} stage)	192	400	500	120
BW	4 kHz	-	250 Hz	12.5 Hz	-	130 Hz
Reslution	14-bit	12-bit	16-bit	20-bit	14-bit	11-bit
Power	34.8μW	13μW	10.7 μW	6.3 μW	19.8 μW	3.17 μW
FoM$_W$ [pJ/conv.]	0.85	0.221	0.76	0.32	1.48	6.07

TABLE VI: Performance comparison.

Specs	ENOB	Speed	Area	Power
Initial	11.2 bits	<10 ms	<0.04 mm^2	<10 μW
Achieved	>10.97 bits	6.4 ms	0.049+0.01 mm^2	3.17 μW

TABLE VII: Initial and achieved ADC specifications.

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