High speed serial busses
USB Bus

- Asymmetric Bus (Host and peripheral devices), 5 V power, (max 500 mA)

- USB supports three data rates:
  
  - The Full Speed rate of 12 Mbit/s (1.5 MB/s) is the basic USB data rate defined by USB 1.0. All USB hubs support Full Speed.
  
  - A Low Speed rate of 1.5 Mbit/s (187.5 kB/s) is also defined by USB 1.0. Intended primarily to save cost in low-bandwidth Human Interface Devices (HID) such as keyboards, mice, and joysticks.
  
  - A High-Speed (USB 2.0) rate of 480 Mbit/s (60 MB/s) was introduced in 2001. All high-speed devices are capable of falling back to full-speed operation if necessary.
  
  - “Super-Speed” (USB 3.0) rate of 4.8 Gbit/s (600 MB/s), from Nov 2008.
USB Physical Bus

- **Pinout**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Color</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V+</td>
<td>Red</td>
<td>+5V</td>
</tr>
<tr>
<td>2</td>
<td>D-</td>
<td>White</td>
<td>Data +</td>
</tr>
<tr>
<td>3</td>
<td>D+</td>
<td>Green</td>
<td>Data -</td>
</tr>
<tr>
<td>3b</td>
<td>Id</td>
<td></td>
<td>Host/Slave</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Black</td>
<td>Ground</td>
</tr>
</tbody>
</table>

- **Bit Coding**

NRZI + BIT STUFFING

(Every Six “1” bits, a “0” is added)

Begins with an 8-bit synchronisation sequence '00000001'.

EOP state SE0 (D+ and D− both below max)
USB Protocol

• Based on pipes (logical channels). A pipe is a connection from the host controller to a logical entity, named Endpoint. Stream and Message pipes

• Handshake packets (packet identifier PID)
  ACK, NAK, STALL

• Token packets (sent by the host)
  IN, OUT, SETUP, PING

• Data packets (0–1023 bytes of data payload)

• PRE "packet" (marks the beginning of a low-speed packet)
Very High Speed Serial Links

- Low-voltage differential signalling (LVDS)
  - Used in HDMI, Serial ATA, PCI Express, ATCA, etc
  - 655 Mbit/s (rates up to 1-3 Gbit/s possible)
  - Uses 8b/10b coding
Extreme Speed Serial Links

- The JESD204/B data converter serial interface standard was created through the JEDEC (Solid State Technology Association) to standardize and reduce the number of data inputs/outputs between high-speed data converters and other devices, such as FPGAs (field-programmable gate arrays).

JESD204 Original Standard

JESD204B Second revision
Parallel Buses and Protocols for Instrumentation

SHARED MEDIUM (Parallel Bus)
GP-IB BUS (IEEE 488)

- Developed by Hewlett-Packard (HP), in the late 60’ (HP-IB)
- Standardised in 1975:
  - IEEE-488.1 - mechanical, electrical, and basic protocol parameters
  - IEEE-488.2 (1987) - Codes, Formats, Protocols, and Common Commands

- TTL logic Levels
- Data Handshake: “We're ready - Here's the data - We've got it”
- The slowest device determine the speed of the transaction (~1MB/s)
GP-IB Topologies

- Max 15 devices
- Each device has a 5 bit (0-30) unique address

Diagram:

1. **Computador**
   - **Gerador de Funções**
   - **Fonte de Tensão**
   - **Multimetro**

2. **Computador**
   - **Gerador de Funções**
   - **Medidor de LCR**
   - **Osciloscópio**
   - **Voltímetro**
**GP-IB Connector**

<table>
<thead>
<tr>
<th>DATA LINES</th>
<th>PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIO1</td>
<td>1</td>
</tr>
<tr>
<td>DIO2</td>
<td>2</td>
</tr>
<tr>
<td>DIO3</td>
<td>3</td>
</tr>
<tr>
<td>DIO4</td>
<td>4</td>
</tr>
<tr>
<td>DIO5</td>
<td>13</td>
</tr>
<tr>
<td>DIO6</td>
<td>14</td>
</tr>
<tr>
<td>DIO7</td>
<td>15</td>
</tr>
<tr>
<td>DIO8</td>
<td>16</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MANAGEMENT LINES</th>
<th>PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFC</td>
<td>9</td>
</tr>
<tr>
<td>REN</td>
<td>17</td>
</tr>
<tr>
<td>ATN</td>
<td>11</td>
</tr>
<tr>
<td>SRQ</td>
<td>10</td>
</tr>
<tr>
<td>EOI</td>
<td>5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HANDSHAKE LINES</th>
<th>PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAV</td>
<td>6</td>
</tr>
<tr>
<td>NRFD</td>
<td>7</td>
</tr>
<tr>
<td>NDAC</td>
<td>8</td>
</tr>
</tbody>
</table>

Sistemas de Aquisição de Dados MEFT 2016/17
GP-IB BUS LINES

- **Data Lines** - Eight lines (DIO1 through DIO8) used to transfer information (data and commands) between devices on the bus, one byte at a time.
- **Handshake Lines** - Three lines used to handshake the transfer of information across the data lines:
  - **DAV**: Data Valid
  - **NDAC**: Not Data Accepted
  - **NRFD**: Not Ready for Data
- **Bus Management Lines** - Five lines used for general control and coordination of bus activities:
  - **ATN**: Attention
  - **IFC**: Interface Clear
  - **REN**: Remote Enable
  - **SRQ**: Service Request
  - **EOI**: End or Identify
- **Ground Lines** - Eight lines used for shielding and signal returns:
GP-IB Data Handshake

Open Collector Lines: NRFD, NDAC (active low)
FAST DATA Handshake (HS488)

The Talker uses this HS488 "wink" signal (the momentary, low-going pulse on -NRFD) to tell the Listener that the Talker is capable of sending data using HS488.

Lack of -NRFD transition indicates that all Listeners are HS488 capable.

Second byte transferred (using HS488).
GP-IB Arbitrating

5 bit Address- 30 combinations

PC Card
- Active Controller
- MTA 7
- MLA 10

MULTIMETER
- STATION # 7 (idle)
- Talker

PRINTER
- STATION # 10 (idle)
- Listener
“Back-plane” parallel Busses

- CAMAC (1970->)
- VME (1980->)
- PCI/PCle (1990->)
- ATCA (2002->)
BUS CAMAC

Still used in many high energy/nuclear Lab throughout the world

COMMAND TYPE:
- STATION NUMBER (N)
- SUBADDRESS (A8, A4, A2, A1)
- FUNCTION (F16, F8, F4, F2, F1)
VMEBus IEEE-1014
(VERSAmodule Eurocard)

• Based on the Motorola 68000 line of CPUs (late 1970’)
• Eurocard sizes, mechanicals and connector

Evolution of VME:

<table>
<thead>
<tr>
<th>Topology</th>
<th>Year</th>
<th>Bus Cycle</th>
<th>Maximum Speed (Mbyte / Sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMEbus32</td>
<td>1981</td>
<td>BLT</td>
<td>40</td>
</tr>
<tr>
<td>VMEbus</td>
<td>1987</td>
<td>BLT</td>
<td>40</td>
</tr>
<tr>
<td>VME64</td>
<td>199</td>
<td>MBLT</td>
<td>80</td>
</tr>
<tr>
<td>VME64x</td>
<td>1997</td>
<td>2eVME</td>
<td>160</td>
</tr>
<tr>
<td>VME320</td>
<td>1997</td>
<td>2eSST</td>
<td>320</td>
</tr>
</tbody>
</table>
VME Backplane electrical termination
(to minimize reflections on the bus lines for high speed signals)

The thevenin equivalent equal to 194 ohms / 2.94 Volt +/- 10%
VME bus features

- Asynchronous bus – there is no central synchronization clock (uses handshaking protocol)

  ![Diagram](image)

  - Data
  - Address
  - Control signals
  - DTACK
VME Asynchronous Data Cycle Handshake

Data transfer Modes = D00 -> D07, D15, D23, D31, or D43 bits
Address Modes = A01 -> A15, A23, A41, A40
VME Interrupt management
7 IRQ# lines + Daisy Chaining
VME Eurocard Board Sizes

9U
Size D

6U
Size C

6U
Size B

3U
Size A
Peripheral Component Interconnect (PCI Local Bus)

- PCI was developed by PCI-SIG, an industry consortium, to replace ISA and VESA Local Bus to connect peripherals to a motherboard.
- Developed in early 90’s and widely adopted by all major PC manufactures. In 1996 adopted also by Apple.
- The PCI specification covers the physical size of the bus, electrical characteristics, bus timing, and protocols.
PCI Bus Topology
PCI Specifications

• 33.33 MHz clock with synchronous transfers

• 32-bit or 64-bit parallel bus width
  • peak transfer rate of 133 MB/s for 32-bit, (266 MB/s for 64-bit) bus width

• 32-bit or 64-bit bus width

• 32-bit address space (4 gigabytes)/32-bit I/O port space

• 256-byte configuration space

• 5-volt/3.3 signalling

• Reflected-wave switching (no bus termination)
PCI Reflected-wave switching

- Reflected signal adds up to the forward signal
- Level enough for signal detection at the receiver.
- Helps to have low power consumption, low cost
PCI Board
Auto-Configuration

- Standardised registers
- Firmware (BIOS) (or operating system) queries all PCI buses at startup time
- Plug & Play
PCI Interrupt Mechanism

• 4 Interrupt physical Lines (INTA#. .. INTD#)
Each board uses only one Line, that can be shared.

• Level Triggered
PCI Connector keying
PCI Extensions and Evolutions

- PC/104-Plus (Industrial PC)
- Mini-PCI (for Laptops)
  PCI-X (eXtended), max 4266 MB/s @ 533Mhz (for servers)
- CompactPCI (3U or 6U Eurocard)
- PCI eXtensions for Instrumentation (PXI)
PCI Express

- Point-to-point serial links (lanes), rather than a parallel shared bus (avoid of timing skew)
- Lane is composed of two differential signaling pairs, (full-duplex byte stream)
- 1 to 32 lanes (each lane 250 MB/s.) 8b/10b encoding
Advanced Telecommunications Computer Architecture (ATCA)

- The ATCA PICMG 3.0 standard defines
  - Shelves, Backplane, Boards, Mezzanines, Management, Data transport
  - Boards: SBC, IO, Hub/switching, Carrier (AMC, PMC)
- Scalable system with **availability** up to **99.999%** ("five nines")
  - Dual redundant communication processors, cards, power supplies and links
  - Intelligent shelf diagnostics and management (temperatures, fans, settings, remote update …)
- **hot-swap**-capable modules and sub-modules.
ATCA Backplane

- **Timing Clocks**
- **Update Ports**

**Fabric Interface**
- [Full Mesh]
  - (8 diff. pairs each)

**Base Interface**
- [Ethernet Dual Star]
  - (4 diff. pairs each)

**IPMB Star**
- 8 Ring/Test Lines
- 48VDC Power

**Single Blade**

**Central Fabric Switch Blades**
ATCA platform highlights

- Each slot is interconnected through up to four 2.5 Gb/s links with an actual throughput capacity of ~800 MByte/s per link
- Multi-protocol support for interfaces up to 20 Gb/s
- Scalable aggregated shelf capacity to 2.5Tb/s
- The ability to host multiple controllers and storage on a shelf (blade servers and DSP farms)
- High availability due to inherent redundancy and regulatory conformance
- Robust power infrastructure (distributed 48V power system) and large cooling capacity (200W per board)
- Reliable mechanics (serviceability, shock and vibration)
- Ease of integration of multiple functions and new features
- Supports 14 slots in 19” cabinet
Bibliografia

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