ADC for IoT Systems

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Abstract

Nowadays, the designers of analog circuits face problems due to the ever-decreasing device sizes, which require the system voltage to decrease. Among other limitations, this leads to a reduced input voltage swings and linearity problems. On the other side of the coin, technology scaling allows the digital cells, such as logic gates and oscillators, to show faster propagation times. Therefore, in the analog design arises a new approach, in which a Time-Domain Quantization replaces the classical Voltage Domain Quantization. There are two different ways to implement Time-Domain Quantization: one way uses a Voltage Controlled Oscillator to convert the input signal from the voltage domain to the frequency and then quantify that frequency; the other uses a Voltage-to-Time Converter to produce two digital signals. The time difference between the digital signals is proportional to the input signal amplitude. Then, a Time to Digital Converter quantifies that time interval. In this dissertation, an Analog-to-Digital Converter was designed, with time interval based Time Domain Quantization, through a time-domain folding approach. It has a 7 bit resolution, operates at 2.5GS/s, and features 6.32 ENOB in typical conditions. This ADC consumes 33.6 mW, leading to a Walden Figure of Merit of $FOM_W = 168.fJ/conv - step$.
Keywords: Analog to Digital Converter, Time Domain Quantization, Voltage Controlled Oscillator, Voltage to Time Converter, Time to Digital Converter

1. Introduction

Nowadays, the improvement of technology leads to a new concern among analog design, related to the ever-decreasing size of the devices. The reduction in transistor gate-oxide thickness forces the system voltage to decrease, making analog design hard to do. It results from weak bias point operation, gate leakage, reduced input voltage swings, and linearity problems. Therefore, this dissertation offsets some of the design challenges imposed by digitally-driven deep-submicrometer CMOS processes by analyzing time-based or time-mode signal processing, [1]. It is a novel approach to manipulate and process analog sample information using digital blocks. In this methodology, conventional voltage and current variables are replaced by time-domain variables such as the time differences between two rising edges, or by the frequency of an oscillator, and logic circuits substitute the large-sized and power-hungry analog blocks. Moreover, adopting digital elements as the base of analog circuits enables digital synthesis and test methods to be used. It is an important step forward in bridging the design gap between analog and digital design.

The analog signals are more frequently in the voltage domain. Therefore, there must have a conversion of the analog input information from the voltage domain to the time-domain. The time-domain variables can either be a change in the frequency of a periodic signal or a time difference between the rise of two different digital signals. In figure 1 are shown these two examples.

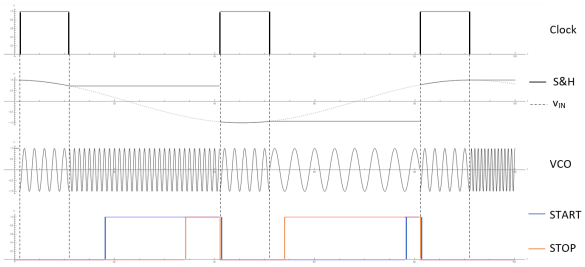


Figure 1: Conversion between Voltage Domain and Time Variables.

In figure 1, the clock signal, the differential input signal, and the sample and hold signal are common to the two approaches. The Sample and Hold signal follows the input when the clock signal is HIGH, and when the clock signal is LOW, it holds, allowing that the following blocks of the converter be able to quantify the amplitude. The conversion type, in

which the time domain variable is frequency, uses a Voltage Controlled Oscillator (VCO). When the clock signal is HIGH, the VCO is at the free-running frequency, and when the clock signal is LOW, the VCO frequency is controlled by the amplitude of the Sample and Hold signal.

In the time interval based conversion type, the time interval between the rising edge time instant of the START and STOP signals is proportional to the differential input's amplitude. If the differential input amplitude is positive, the START signal's rising edge occurs sooner than the STOP signal's rising edge. Otherwise, the STOP signal is the first to rise. When the clock signal is HIGH, these digital signals are LOW.

This work presents the two types of Time Domain Quantization ADCs and then is implemented and simulated a Time Interval Based ADC, with 7-bit resolution, the sampling rate of $2.5GS/s$, that implements a time-domain folding approach.

This paper is organized as follows: Section 2 shows the overall architectures of time domain quantization ADCs, based on frequency and based on time interval, section 3 shows the implemented ADC, section 4 shows the pre layout simulation results and section 5 concludes this paper.

2. General Time Based Quantization ADC Architectures

As said before, there are two main types of Time Base Quantization ADCs: frequency-based quantization and time interval based quantization.

2.1. Frequency Based Quantization

The basic circuit of frequency based quantization ADC is in figure 2.

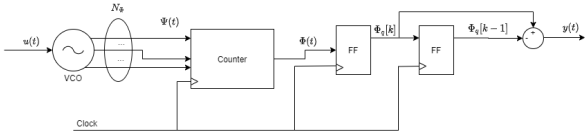


Figure 2: Frequency based ADC Circuit.

In figure 2(a), the analog input, $u(t)$, is presented to an oscillator and will define its frequency. This oscillator converts the analog input into frequency. If the VCO is ideal, the transfer function between the VCO's input signal and its frequency $\Psi(t)$ is

$$\Psi(t) = 2\pi(K_o u(t) + f_o), \tag{1}$$

where K_o is the VCO gain ([Hz/V]) and f_o is the free-running frequency of the oscillator, [2, 3].

The phase signal, $\Phi[k]$, at every sampling period, [4], is described by

$$\Phi[k] = \int_{kT_s}^{(k+1)T_s} \Psi(\tau)d\tau + p_i[k], \tag{2}$$

where $\Phi[k]$ is the VCO's phase signal, $\Psi(t)$ is the VCO's frequency signal, and $p_i[k]$ is the initial phase at $t = kT_s$. As seen in figure **??**, the initial phase is equivalent to the previous quantization error, $p_i(kT_s) = e((k-1)T_s)$. The phase is then the previous phase quantization error plus the phase variation, $\Phi_x(t) = \int_{kT_s}^{(k+1)T_s} \Psi(\tau)d\tau$, during the sampling period.

At the output of the counter, there is a flip flop (FF), to quantify phase signal at every instant $t = kT_s$,

$$\Phi_q[k] = \frac{N_\Phi}{2\Pi}(\Phi[k] - e[k]), \tag{3}$$

where $\Phi_q[k]$ is the phase quantified, $\Phi[k]$ is the phase, and $e[k]$ is the phase quantization error. The phase quantified, $\Phi_q[k]$, is an integer given by the counting of the Counter, and so there is the factor $\frac{N_\Phi}{2\pi}$ in (3) to translate the phase value to an integer.

The last block of this ADC type, figure 2(b), is a differentiator between the actual output phase quantified and the previous one. By differentiating phase with respect to time yields frequency. Since VCO's frequency is proportional to the input signal, the output of this differentiator is proportional to the input signal, described by

$$y[k] = \frac{N_\Phi}{2\pi}\left(\Phi_q[k] - \Phi_q[k-1]\right) \tag{4}$$

$$= \frac{N_\Phi}{2\pi}\left[\Phi[k] - \Phi[k-1] - (\Phi_\epsilon[k] - \Phi_\epsilon[k-1])\right]$$

where N_Φ is the number of VCO's output phases.

Taking the z transform of (4) yields

$$Y(z) = \frac{N_\Phi}{2\pi}(1 - z^{-1})(\Phi(z) - \Phi_\epsilon(z)). \tag{5}$$

From (5), it is possible to take the noise transfer function, $NTF = \left(\frac{Y(z)}{\Phi_\epsilon(z)}\right)|_{\Phi(z)=0}$, and the signal transfer function, [2], $STF = \left(\frac{Y(z)}{\Psi(z)}\right)|_{\Phi_e=0}$, described by

$$\begin{cases} NTF(z) \approx \frac{N_\Phi}{2\pi}(1 - z^{-1}) \\ STF(z) \approx \frac{N_\Phi}{2\pi}\frac{(1+z^{-1})}{2}. \end{cases} \tag{6}$$

The STF shows that the output signal is just an average between consecutive samples. This leads to some problems. Analysing a sinusoidal input signal with period T_{in} and correspondent frequency f_{in}, it has symmetric values at time instants $t = T_{in}(\frac{1}{2} + k)$. Since samples are taken at every T_s, if $T_s = T_{in}(\frac{1}{2} + k)$, the samples will always be symmetric. It means that if $f_{in} = f_s(\frac{1}{2} + k)$, the ADC's output signal will have no information about the input signal because the consecutive samples cancel each other due to the averaging. The cancellation

is not a particularly bad thing once this frequency is the well known Nyquist frequency, $f_{nyq} = f_s/2$, which is the maximum bandwidth of an ADC.

If the input frequency is low, two consecutive samples have similar values, the average between them near results in a value close to the samples' value leading a small error. As the input frequency increases to near $\frac{f_s}{2}$, the average of the consecutive samples converge to zero since they become near symmetric, and the error increases. For this reason, this type of ADC requires an oversampled input signal, which means that the maximum frequency of the input signal is much smaller than the sampling frequency. As the error increases with the increase of the input frequency, the ADC has a high pass characteristic.

To prevent the high pass characteristic and increase the input bandwidth there is possibility of time interleaving N identical ADCs. The sampling period of each ADC becomes $T_s' = N \times T_s$. The cancellation of samples, due to the averaging, now happens when $T_s' = NT_s = T_{in}(k + \frac{1}{2})$. It shows that with N time-interleaved ADC blocks if the input frequency is $f_{in} = \frac{f_s}{N}(k + \frac{1}{2})$ the output does not have information of the input signal, and the error is maximum. However, due to periodicity the input signal, is the smae at $t = kT_{in}$. Then, if $T_s' = NT_s = T_{in}k$, the samples will be equal, for each ADC. So if $f_{in} = \frac{f_s}{N}k$, the output signal does not have an error due to the averaging, which means that the signal transfer function is maximum and the error is null. Therefore, the high pass characteristic becomes a bandpass characteristic.

From (6) is possible calculate the frequencies that correspond to the maximum and zeros of the NTF and STF:

$$|NTF(\omega)| = 0 \leftrightarrow \omega = \frac{i}{N}\omega_s,$$

,

$$|NTF(\omega)|_{max} \rightarrow \omega = \frac{\omega_s}{N}\left(\frac{1}{2} + i\right),$$

$$|STF(\omega)| = 0 \leftrightarrow \omega = \frac{\omega_s}{N}\left(\frac{1}{2} + i\right) \text{ and}$$

$$|STF(\omega)|_{max} \rightarrow \omega = \frac{i}{N}\omega_s$$

which is consistent to what was discussed before.

The fact that the STF has zeros for frequencies in the range of $[0, \frac{f_s}{2}]$ makes this type of ADC unable to produce an output that has information of the analog input signal for those frequencies.

2.2. Time Interval Based

The other time-domain quantization uses a VTC. It converts the input analog signal from the voltage domain to the time domain, where the time variable is the time difference between the rising edge of two digital signals. Time-domain quantization ADCs can use either multiple VTCs or a single VTC.

2.2.1 Multiple VTC

Usually, when Time-domain quantization ADCs use multiple VTCs, the most common architecture is a Flash ADC in the Time Domain, as represented in figure 3, [5, 6, 7, 8, 9].

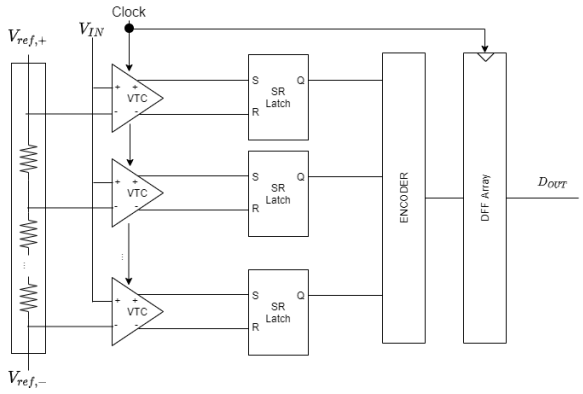


Figure 3: Flash ADC using VTCs.

The architecture of figure 3 is quite similar to most common Flash architectures in the voltage domain, but in this case, VTCs replace the comparators and latches make the decisions, acting as time comparators. As seen in figure 3, this flash ADC architecture needs 2^N VTCs and 2^N Latches for an N bit resolution ADC. It leads to a big area ADC with high consumption. On the one hand, a Time Domain Interpolation technique, as seen in figure 4, can reduce the number of needed VTCs and Latches. On the other hand, a Time Domain Folding can improve the area's efficiency and power consumption by reducing the number of Latches.

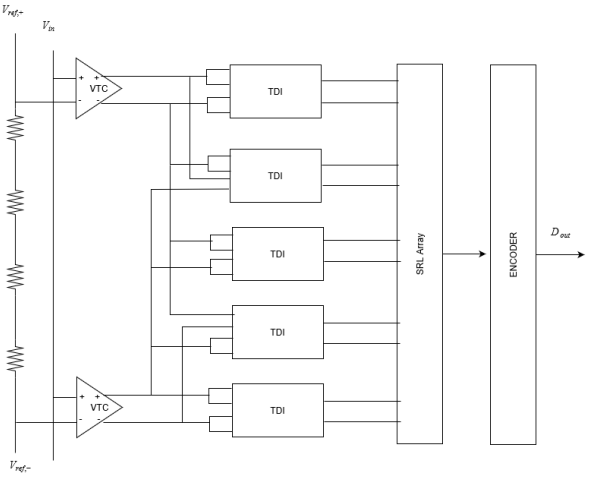


Figure 4: Basic block diagram of time domain interpolation Flash ADC.

As seen in figure 4, when implementing an interpolation approach, the number of VTCs reduces to $2^{bits}/IF$. In this example $IF = 4$. Interpolating the output of the existing VTCs generates the information of the eliminated VTCs. In the time domain, Time Domain Interpolators (TDI) perform the interpolation. The TDI circuit is in figure 5.

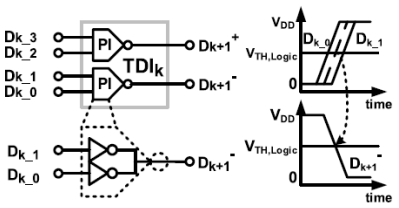


Figure 5: TDI Circuit, adapted from [5].

The TDI cell, shown in figure 5, is composed of two-phase interpolators. The interpolators are composed of two inverters with the outputs connected. If the input D_{K_0} rises from Low to High at time instant t_1 and D_{K_1} does it at t_2, the output of the phase interpolator falls from High to Low at $t = \frac{t1+t2}{2}$.

2.2.2 Single VTC

Time domain quantization ADCs that have a single VTC lead to all quantization of the analog signal be done in the time domain. To perform the quantization, there is a Time to Digital Converter (TDC), as represented in figure 6.

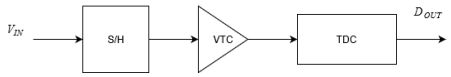


Figure 6: Time interval Based ADC, with a single VTC and a TDC.

One approach of time domain quantization is to implement a time domain folding, as illustrated in figure 7.

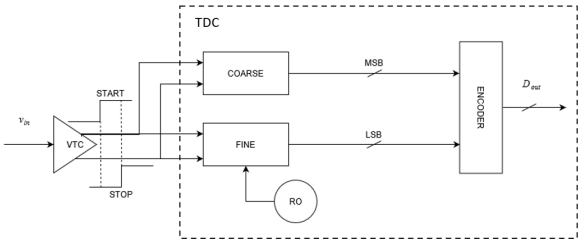


Figure 7: Basic time domain folding block diagram.

As seen in figure 8, the folding circuit folds the input range into 2^n folds, each with 2^{N-n} levels,

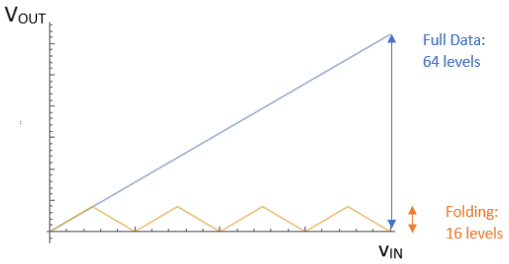
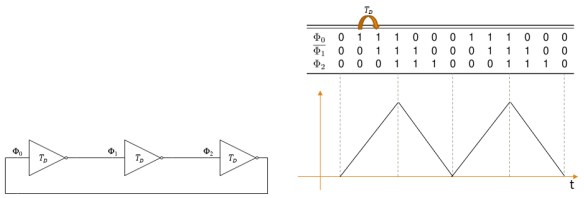


Figure 8: Transfer curve of folding circuit in comparison with transfer curve of a full ADC's output.

where N is the full ADC's resolution, and n is the coarse quantizer resolution. In the example of figure 8, $N = 6$ and $n = 2$. The Folding codes correspond to the least significant bits (LSBs) of the ADC's output code. The n-bit coarse quantizer is required to identify to which fold the input voltage corresponds, generating the n most significant bits (MSBs). The coarse quantizer and the fine quantizer generate the n MSBs and the $N - n$ LSBs synchronously. The concept of time-domain folding is illustrated in figure 9, [10].



(a) 3 stage RO. (b) Fine Quantifier Codes.

Figure 9: Concept of time-domain folding.

Let us take a three-stage RO as an example. The RO is free running, and periodic oscillatory waveforms appear on the three internal nodes, ϕ_0, ϕ_1, and ϕ_2. If we record ϕ_0, $\overline{\phi_1}$ (the inversion of ϕ_1) and ϕ_2 collectively for some time, we can observe a thermometer-like digital code (represented together by ϕ_0, $\overline{\phi_1}$ and ϕ_2) circulating among six codes per RO period. The repeating nature of the oscillation gives rise to the folding operation in the time domain. The time-lapse between two consecutive thermometer codes corresponds to exactly one inverter delay. Therefore, it represents the LSB size of the quantizer. Thus, RO provides a compact realization of signal folding and quantization in the time domain. Compared to voltage-domain folding operations, time-domain folding provides two distinctive advantages. First, voltage-domain folding is quite non-linear, while time-domain folding using RO results in an inherently linear operation. Secondly, time-domain folding, given enough conversion time, yields an infinite folding factor, whereas

it is limited by the number of folding amplifiers in the voltage domain. Thus, time-domain folding is also very efficient.

3. Implementation

The implementation chosen for this master dissertation is a 7 bit Time Interval Based ADC, with a TDC that implements a folding approach. The Time-Based ADC uses a VTC, an Asynchronous Counter, a Ring Oscillator, and a Decoder as seen in figure 10.

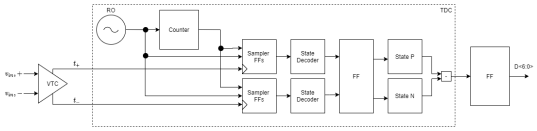


Figure 10: General Circuit of the ADC.

3.1. VTC

The input analog signals are more frequently in the voltage domain. Then, there must be an auxiliary circuit that converts the voltage domain's amplitude into a time variable, which is the time difference between the rising edge of two digital signals. The VTC used is represented in figure 11, [11, 12]. In figure 11, $\phi_2 = \overline{\phi_1}$.

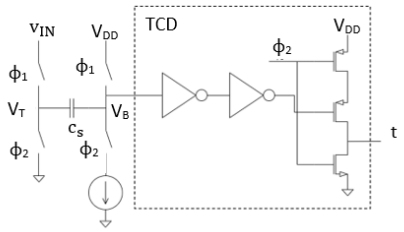


Figure 11: VTC Schematic Circuit.

To understand how this VTC works, figure 12 shows the main signals.

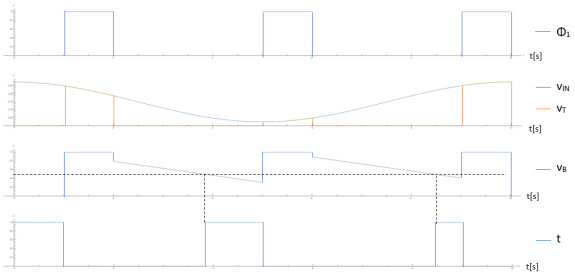


Figure 12: VTC Main Signals.

The VTC implemented, shown in figure 11, is composed of four switches, a capacitor, a reference current source, and a Threshold Cross Detector (TCD). The TCD is composed of two simple inverters and a true phase inverter. As seen in figure 12, the process begin with the left terminal of the capacitor C_s follows the input signal, $V_T = v_{IN}$, while ϕ_1 is HIGH and the right terminal of the capacitor is charged to the supply voltage, $V_B = V_{DD}$. Then, as the left terminal of the capacitor discharges to the ground, the right terminal must discharge the same amount, once the differential potential between the two terminals of the capacitor can not change instantaneously, and so $V_B = V_{DD} - v_{IN}$. Then, the node V_B discharges by a constant current. When V_B crosses the threshold voltage of the first inverter, the output digital signal becomes HIGH.

As seen in figure 12, the time that takes the output signal, t, to rises is longer for a small amplitude signal of the input sample. Assuming an ideal capacitor, which current-voltage relation is $i_C = C\frac{dV}{dT}$, results:

$$\Delta t = \int \frac{C}{i_C} dV. \tag{7}$$

In (7) C is positive and constant and i_c is negative and constant. From (7) results:

$$\Delta t(t_k) = -\frac{C}{|i_C|}(v_f - v_i), \tag{8}$$

where v_f is the threshold voltage of the cross detector, v_{TH} and $v_i = V_B(t_k) = V_{DD} - v_{IN}(t_k)$. Then:

$$\Delta t(t_k) = \frac{C}{|i_C|}(V_{DD} - v_{TH}) - \frac{C}{|i_C|}v_{IN}(t_k), \tag{9}$$

which translates a linear relationship between the input signal and the rising time instant and shows that higher input amplitude, $v_{IN}(t_k)$, results in a higher time interval. However, the VTC generates two output digital signals that translate the differential input amplitude through the time difference between their rising edges. So, if the positive input is defined by $v_{in,+} = V_C + \frac{v_d}{2}cos(2\pi f_{in}t)$, where V_C is the common-mode voltage, v_d is the differential input amplitude and f_{in} is the input frequency, the negative input is defined by $v_{in,-} = V_C - \frac{v_d}{2}cos(2\pi f_{in}t)$, the time interval between the outputs of the VTC is defined by

$$\Delta t_{VTC}(t_k) = t_- - t+ - = \frac{C}{|i_c|}v_d cos(2\pi f_{in}t_k). \tag{10}$$

The time interval between the outputs of the VTC is linear in respect to the input signal, and the gain of the VTC is $\frac{C}{|i_C|}[s/V]$, which translates the relation between the input voltage amplitude and the time interval between the rising edges of the two digital signals at the output of the VTC.

3.2. TDC

As seen in figure 10, the TDC is composed of a RO, an asynchronous Counter, and FFs. The TDC quantifies the time interval between the two digital signals at the output of the VTC by a folding approach.

As the information from the VTC is given by a time difference, the quantization is also given by a difference. Each digital signal at the output of the VTC defines a state, defined by two bits from the counter and four bits from the RO. This folding approach differentiates between four folds, and each fold is differentiated between sixteen codes. The final code is given by the difference between the states defined by the two digital signals, t_+ and t_-. The t_+ signal corresponds to the positive input signal, $v_{in,+}$, and the t_- signal corresponds to the negative input signal, $v_{in,-}$. If the rising edge of the t_+ signal occurs first than the rising edge of the t_- signal it means that the differential input signal is positive, i.e, $v_{in,+} > v_{in,-}$.

$$\begin{cases} EP = T_D \times (16 \times Coarse_P + Fine_P) + e_P \\ EN = T_D \times (16 \times Coarse_N + Fine_N) + e_N. \end{cases} \tag{11}$$

The state difference is then given by $EN - EP = T_D \times [(Fine_N - Fine_P) + 16 \times (Coarse_N - Coarse_P)] + e_N - e_P$, where $|e_N - e_P| < 1$LSB. If the t_+ rises sooner than t_- when the input differential amplitude is positive, the state difference must be positive, and if t_- rises sooner, the state difference must be negative. Due to the double quantization error, the ADC's linearity is limited, once there is a 3 dB degradation of the SNR, and so the maximum linearity of the ADC is 6.5 ENOB.

This ADC implementation does not reset the RO nor the Counter at any time. Then, the state defined by each digital signal is always random. On the one hand, this allows having an inherent DEM operation, in which the LSB is not given by the propagation time of one single delay cell in the RO, but by the average between all of the propagation cells in the delay cells. The differences between those propagation times do not generate nonlinearity but white noise. On the other hand, the codes generated from the folding approach are crescent and periodic. It means that the following code of the higher state value is the lower state value, as seen in figure 13.

For some time intervals, the states sampled by each digital signal of the VTC can belong to different folding code periods. So, to correct the results of the computation of the state difference, it is added a bit to the counter, redundancy bit, that identifies if the states are from the same folding period or not.

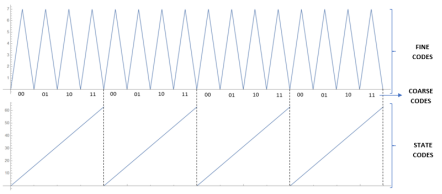


Figure 13: Fine, Coarse and State Codification.

3.2.1 Ring Oscillator

As seen before, the RO is responsible for a 4bit periodic code. To do so, it needs eight delay differential stages, using the negative and the output of the delay stage, consecutively, as seen in figure 14.

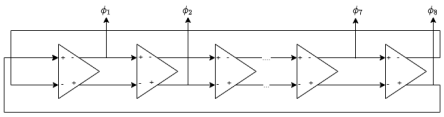


Figure 14: Differential RO.

The RO implemented has a main oscillator and a sub-oscillator, as seen in figure 15, [13].

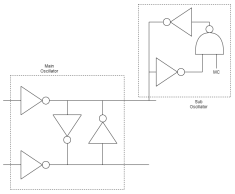


Figure 15: Main and Sub Oscillator.

The main oscillator is a conventional differential inverter, while the sub-oscillator has two inverters and a NAND gate. The MC signal controls if the sub-oscillator is active, $MC = 1$, or not, $MC = 0$. This control signal has the starting value of LOW then rises to HIGH to help the oscillator to begin to oscillate.

To reduce the charge effect of the rest of the ADC in the propagation time of the delay stages, the output phases of the RO go through buffers, figure 16.

As the RO's output signal Φ_8 goes to the input of the counter and the input of a FF, while all the others only go to the FFs, the buffers are composed of four inverters, generating two different paths. Each path is composed of three inverters. One leads to the sampling FFs and the other leads to the input of the counter. The implementation assures the same charge in all stages sampled by the FFs, allowing that the propagation time of each become similar as possible.

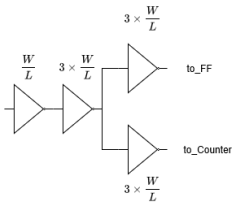
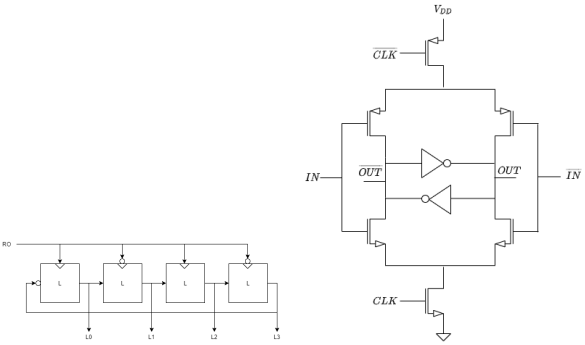


Figure 16: RO Output Buffers.

3.2.2 Counter

The Counter identifies in which fold the time difference between the digital outputs of the VTC resides. To do so, it counts the number of periods of the RO, with a divide-by-four structure, [14]. Figure 17(a) shows the divide-by-four structure and the latch schematic circuit is in figure 17(b). To understand how the circuit works, figure 18 shows the signals.



(a) Divide-by-Four Structure. (b) Latch Circuit.

Figure 17: Asynchronous Counter Circuit.

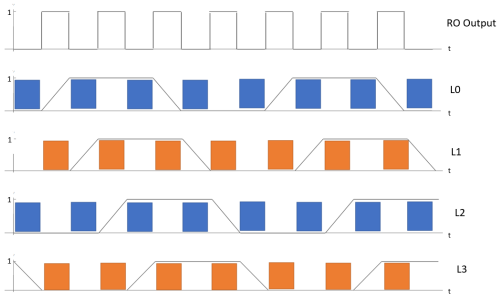
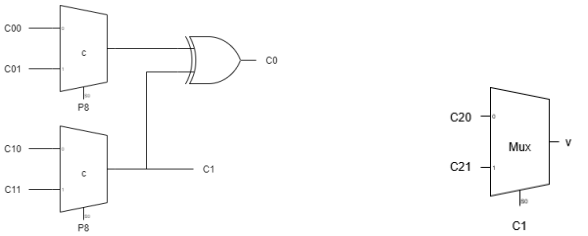


Figure 18: Counter Signals.

As seen in figure 18, the divide-by-four structure outputs four signals, L0-L3. Each has the same frequency, which is 1/4 of the RO signal frequency, and they are a half period of the RO signal shifted between each other. At each half period of the RO signal, there is a variation in one of the counter output signals. Those variations are consecutive and periodic: first changes L0, then L1, then L2, then L3, then L0, and so on. Assuming that each variation takes a whole half RO period, each signal is stable for three half periods. If the even signals (L0 and L2) are sensitive to the half periods where the RO signal is HIGH, and the odd signals (L1 and L3) are to the half periods where the RO signal is LOW, the even are stable when the RO signal is HIGH, and the even ones are stable when the RO signal is LOW. The signals L0-L3 and Φ_8 RO's signal are sampled and decoded to compute the 2-bit word of the coarse code. In figure 19 is shown the counter's signals decoder.



(a) Two Least Significant Bits. (b) Most Significant Bit.

Figure 19: Counter Decoder.

In figure 19(a), C00-C11 are the sampled signals of L0-L3, and P8 is the sampled RO's signal Φ_8. As L1 and L3 are stable when $\Phi_8 = 0$ and L0 and L2 are stable when $\Phi_8 = 1$, to compute the coarse code, P8 is the selection bit of two multiplexers, L0 and L2 are the LOW inputs, and L1 and L3 are the HIGH inputs. L1 and L3 are guaranteed to be stable when P8=1, and so the multiplexers choose stabilized signals. L0 and L2 are guaranteed to be stable when P8=0 and the multiplexers also choose stabilized signals. Both multiplexers' inputs are guaranteed to be stable when P8 is metastable, and so the multiplexers can choose either one.

The redundancy bit's generation uses the same approach to, figure 19(b). There is a divide-by-two block in which the signal that controls the velocity is the L3 signal of the previous block, and then the selection bit is the selected signal between L2 and L3, which is the output signal C1 of the divide-by-four block.

3.3. ADC Linearity

The SNR evaluates the ADC's linearity. By definition, the signal to noise ratio in the time domain is given by

$$SNR = 20Log\left(\frac{t_{max}}{\sqrt{2}\sigma_{ADC}}\right) \tag{12}$$

where t_{max} is the maximum time interval between the digital signals at the output of the VTC that the TDC can quantify, defined by

$$t_{max} = \frac{2^N \times t_{LSB}}{2} \tag{13}$$

where N is the ADC resolution and t_{LSB} is the size of the Least Significant bit in the time domain and σ^2_{ADC} is the total jitter of the ADC.

To SNR be the relation between the RMS value of the maximum time interval and the RMS time noise, t_{max} is divided by $\sqrt{(2)}$ once it is considered a sinusoidal input.

The total jitter of the ADC, given by

$$\sigma^2_{ADC} = \sigma^2_{VTC} + \sigma^2_{TDC}, \tag{14}$$

where σ^2_{VTC} is the output jitter of the VTC and σ^2_{TDC} is the input-referred TDC jitter. The total jitter is the addition of those two terms, once the two terms are assumed to be independents.

The VTC voltage noise is given by, [10]:

$$V^2_{n,VTC} = \frac{kT}{C_s}\left(1 + 2\gamma\frac{g_m}{I_C}\right) \tag{15}$$

where k is the Boltzmann constant, T is the absolute temperature, C_S is the VTC capacitor, γ is the thermal coefficient of the transistor that operates as current source, g_m is its transconductance and I_C is the discharging current. The VTC output jitter is defined by the noise voltage divided by the slew rate, SR_{VTC}, at the threshold-crossing point,

$$\sigma^2_{VTC} = \frac{2V^2_{n,VTC}}{SR^2_{VTC}} = \frac{\frac{2kT}{C_S}\left(1 + 2\gamma\frac{g_m}{I_D}\right)}{\left(\frac{I_C}{C_S}\right)^2}. \tag{16}$$

The input-referred TDC jitter is given by

$$\sigma^2_{TDC} = 2 \times (\sigma^2_q + \sigma^2_{FF}) + \sigma^2_{RO} + \sigma^2_{Counter} + \sigma^2_{DEM}, \tag{17}$$

where σ_q is the RMS value of the quantization noise, σ_{FF} is the input-referred jitter of the DFF, σ^2_{RO} is the RO jitter, $\sigma^2_{Counter}$ is the counter jitter, and σ^2_{DEM} is the white noise converted from the mismatch, of the RO delay stages, due to the inherent DEM operation. Due to the quantization of the two states, the contribution of the quantization error, σ_q, and the input-referred RMS noise of the FF, σ_{FF}, are doubled, [15]. It leads to a limitation on the ADC linearity. If all blocks are ideal and do not presently jitter, the signal to noise ratio becomes

$$SNR = 20Log\left(\frac{t_{max}}{\sqrt{2}\sigma_q}\right) \tag{18}$$

where the quantization error, σ_q, is defined by

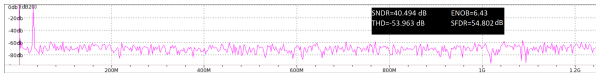
$$\sigma_q = \frac{t_{LSB}}{\sqrt{12}}. \tag{19}$$

The SNR becomes $SNR \approx 6.02(N-1) + 4.77dB$, showing that there is a 3dB degradation due to the double sampling, corresponding to a 0.5-bit degradation in the ENOB. Then, the maximum linearity of this ADC is 6.5 ENOB.

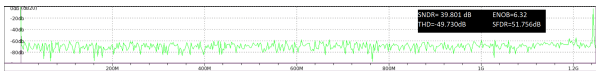
4. Results

4.1. Linearity

In order to evaluate the ADC's linearity in typical conditions, it is evaluated the output for a sinusoidal input, with two different frequencies, $f_{in} = 31.738MHz$ figure 20(a) and $f_{in} = 1242.676MHz$ figure 20(b). The frequency 1242.676MHz is the higher frequency close to the Nyquist frequency that assures a coherent sampling for a 1024 point simulation.



(a) $f_{in} = 31.738MHz$.



(b) $f_{in} = 1242.676MHz$.

Figure 20: Linearity Simulation.

As seen in the results of figure 20, the harmonic distortion is very low, translated by the THD results, confirming that the VTC linearity is high enough to assure a high-resolution ADC.

In figure 20, the FFTs show that the degradation of the ADC linearity is mainly from the noise floor and not from the harmonic distortion. On the one hand, there is harmonic distortion if the mathematical relations between the input and the output of ADC's blocks show components of a high order, which does not exist. On the other hand, the noise floor is justified by the quantization error, which has the same amplitude among the full frequency bandwidth as white noise. These FFTs also show that the SNDR and the ENOB results are almost constant for all input frequency signals, once there are almost none harmonic components that degrade the ADC linearity. The inherent DEM operation leads to good linearity results once the SFDR is very high for all the frequency bandwidth.

To evaluate the robustness of the linearity, it is performed the same simulation for PVT variations.The proccess variation simulation results are in the figure 21, the supply voltage variation ($^+_-10\%$) simulation results are in the figure 22(a) and the temperature variation ($-40°C/125°C$) simulation results are in the figure 22(b)

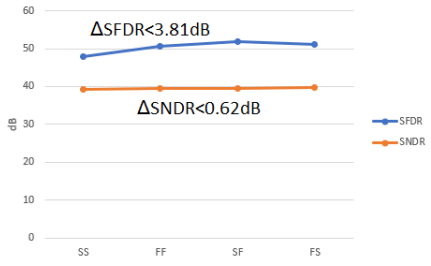
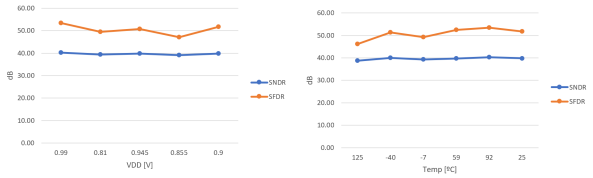


Figure 21: Process Variations.



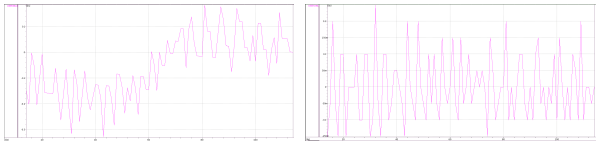
(a) Supply Voltage Variation. (b) Temperature Variation.

Figure 22: VT Variation Simulation Results.

The results of figure 21, show that, in terms of process, the SNDR varies about 0.62dB, and consequently that the ADC is robust in those terms. The results of figure 22 show that variations on the supply voltage lead to a variation of 1.03 dB on the SNDR, and the temperature's leads to 1.47 dB, which allows concluding that the ADC is robust in terms of those variations.

4.2. INL DNL

To evaluate the INL and DNL, the input of the ADC has generated a ramp signal. As the sampling frequency is $f_s = 2.5GHz$, the ADC outputs a new value every 0.4ns. As it is a 7 bit ADC, there are 128 output codes. Performing a 2048 point simulation allows that at each code there are 16 samples. The ramp signal takes $0.4 \times 128 \times 16 = 819.2$ ns to rise to evaluate the INL and DNL, figure 23.



(a) INL. (b) DNL.

Figure 23: INL and DNL Simulation.

As seen in figure 23, DNL= $-0.151/0.249$ LSB and INL= $-0.182/0.329$ LSB, for the 2048 point simulation. The results show that the inherent DEM operation of the folding architecture translates to highly linear ADC.

4.3. Consumption

Running at Nyquist Frequency, the overall power consumption is 33.6mW. Figure 24 represents the power consumption breakdown.

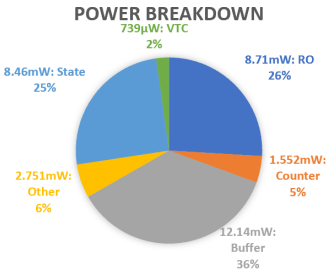


Figure 24: Power Breakdown.

The power consumption shown in figure 24 shows that output buffers of the RO and the RO are the blocks with higher consumption. The power consumption of an oscillator is given by

$$P = f_{osc} \times C_L \times V_{DD}^2 \tag{20}$$

where f_{osc} is the oscillation frequency, C_L is the oscillation capacitance, and V_{DD} is the supply voltage. The capacitance is a function, among other things, of the transistor sizes. So, for a high-frequency oscillator, power consumption is inevitably high. The power consumption described by (20) show why the buffer output has higher power consumption than the RO once the oscillation frequency is the same, the power supply of each circuit is also the same, but the transistors of the buffer are larger than the transistors of the RO.

The results in figure 24 also show that the VTC has low consumption, and so the main voltage domain-dependent block of this ADC is the one with lower power consumption.

4.4. Bandwidth

To evaluate the Bandwidth of the ADC and its PVT variation, the SNR is evaluated for six different frequencies, figure 25.

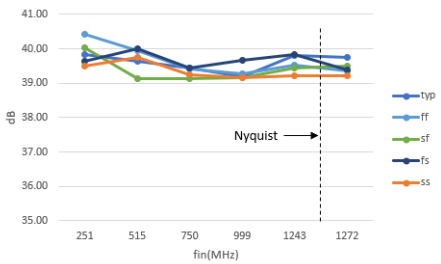


Figure 25: Bandwidth Evaluation.

As seen in figure 25, the ADC's bandwidth does not change in with PVT variation, and the 3dB bandwidth is higher than the Nyquist frequency.

5. Conclusions

This work presents a 2.5 GS/s 7 bit time-domain folding ADC. It achieves highly competitive area efficiency among all recent ADC works of similar sample rate and resolution. The VTC presents high linearity and has low consumption, allowing an ADC design of high linearity for a 7-bit resolution. The RO-based folding TDC achieves high area efficiency and high speed simultaneously. The inherent DEM of the RO-based TDC is also highly linear, manifested by DNL of -0.151/–0.249 LSBs, INL of -0.182/+0.329 LSBs. Due to the double sampling limitation linearity of 6.5 ENOB for a 7-bit resolution ADC, the ADC achieves high linearity of 6.32 ENOB at Nyquist input frequency, ($f_{in} = f_s/2$), with a 33.6mW power consumption, leading to a Walden Figure of Merit $FOM_W = 168.1fJ/step$, which is an improvement when comparing with the architectures that implement time domain folding, [10, 16].

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