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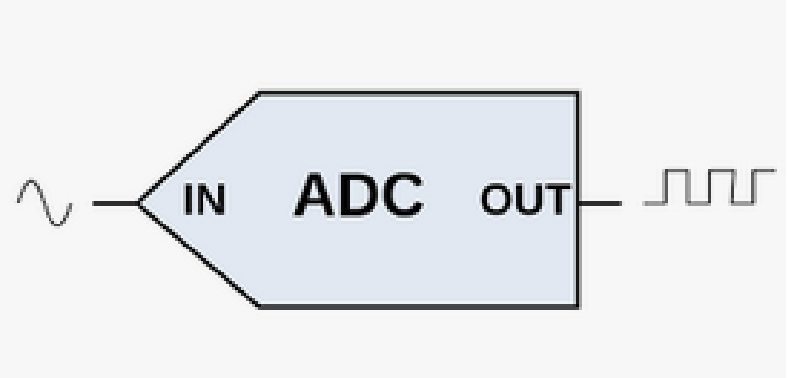

ADC for IoT Systems

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Electrical and Computer Engineering

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I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

Dedicated to my parents

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Resumo

Hoje em dia, os dimensionadores de circuitos analógicos enfrentam problemas devido à continua diminuição dos tamanhos dos dispositivos, que resulta numa redução contínua da tensão de alimentação do sistema. Esta redução provoca, entre outros problemas, uma redução no alcance de tensão de entrada e em limitações de linearidade. Por outro lado, esta redução do tamanho dos dispositivos leva a que células digitais, tais como portas lógicas ou osciladores, apresentem tempos de propagação cada vez mais rápidos. Então, surge uma nova abordagem no dimensionamento de circuitos analógicos, na qual a quantificação clássica do sinal analógico de entrada no domínio da tensão é substituída por quantificação no domínio temporal. Esta substituição pode ser feita de duas formas: utilizar um Oscilador Controlado por Tensão para converter a amplitude analógica de entrada, no domínio da tensão, em frequência e posteriormente quantificar esta frequência; utilizar um Conversor Tensão Tempo para produzir dois sinais digitais cujo intervalo de tempo entre estes é proporcional à amplitude do sinal de entrada e um Convertor Tempo Digital para quantificar esse intervalo de tempo. Nesta dissertação, descreve-se um Conversor Analógico Digital, com quantificação no Domínio Temporal baseada em intervalo de tempo, através de uma abordagem de dobragem no domínio temporal. Este conversor tem uma resolução de 7 bits, funciona a 2.5 GS/s e apresenta 6.32 ENOB, em condições típicas. Este ADC consome 33.6 mW atingindo assim uma Figura de Mérito de Walden de $FOM_W = 168.1fJ/conv-step$.

Palavras-chave: Conversor Analógico Digital, Quantificação no Domínio Temporal, Oscilador Controlado por Tensao, Conversor Tensao Tempo, Conversor Tempo Digital

Abstract

Nowadays, the designers of analog circuits face problems due to the ever-decreasing device sizes, which require the system voltage to decrease. Among other limitations, this leads to a reduced input voltage swings and linearity problems. On the other side of the coin, technology scaling allows the digital cells, such as logic gates and oscillators, to show faster propagation times. Therefore, in the analog design arises a new approach, in which a Time-Domain Quantization replaces the classical Voltage Domain Quantization. There are two different ways to implement Time-Domain Quantization: one way uses a Voltage Controlled Oscillator to convert the input signal from the voltage domain to the frequency and then quantify that frequency; the other uses a Voltage-to-Time Converter to produce two digital signals. The time difference between the digital signals is proportional to the input signal amplitude. Then, a Time to Digital Converter quantifies that time interval. In this dissertation, an Analog-to-Digital Converter was designed, with time interval based Time Domain Quantization, through a time-domain folding approach. It has a 7 bit resolution, operates at 2.5GS/s, and features 6.32 ENOB in typical conditions. This ADC consumes 33.6 mW, leading to a Walden Figure of Merit of $FOM_W = 168.fJ/conv - step$.

Keywords: Analog to Digital Converter, Time Domain Quantization, Voltage Controlled Oscillator, Voltage to Time Converter, Time to Digital Converter

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Nomenclature

Greek symbols

$\Phi(t)$	VCO's Continuous Phase Signal
$\Phi_\epsilon[k]$	VCO's Quantization Error, at $t = kT_s$
$\Phi_q[k]$	VCO's Quantized Phase Signal, at $t = kT_s$
$\Psi(u)$	VCO's Transfer Function
N_Φ	Number of VCO's Output Phases

Roman symbols

f_o	VCO's Free Running Frequency
f_s	Sampling Frequency
f_{tune}	VCO's Frequency Tunning Range
K_o	VCO's gain
N_d	Number of VCO's Delay Cells
P_N	Output Noise Power
T_D	Time Delay of a Delay Cell
T_s	Sampling Period
$T_{d,min}$	Minimum Delay of a VCO's Delay Cell
$t_{out,+}$	Positive VTC's Output Digital Signal
$t_{out,-}$	Negative VTC's Output Digital Signal
V_{DD}	Voltage Supply
V_{FS}	Input Voltage Full Scale
$v_{in,+}$	Positive Analog Input Voltage
$v_{in,-}$	Negative Analog Input Voltage

v_{in} ADC's Analog Input Voltage

V_{TH} Threshold Voltage

Subscripts

ADC Analog to Digital Converter

DAC Digital to Analog Converter

FF Flip Flop

FFT Fast Fourier Transform

IoT Internet of Things

LSB Least Significant Bits

MSB Most Significant Bits

MUX Multiplexer

NTF Noise Transfer Function

P Input Power

RO Ring Oscillator

SFDR Spurious-Free Dynamic Range

SNR Signal to Noise Ratio

SRL Set Reset Latch

STF Signal Transfer Function

TDC Time to Digital Converter

TDI Time Domain Interpolators

TMSP Time Mode Signal Processing

VCO Voltage Controlled Oscillator

VTC Voltage to Time Converter

Chapter 1

Introduction

We live in an analog world, as there is an infinite amount of colors, tones, smells we can smell. These are examples of analog signals. The common theme among them is their infinity of different values that can assume. On the other hand, the digital signals and objects are discrete or finite, meaning there is a limited set of values they can have. Electronic systems have to interact with the real analog world, but most microprocessors, computers, and logic units are purely digital components.

An Analog-to-Digital Converter (ADC) converts an analog input signal, such as the sound picked up by a microphone or light entering a digital camera, into a digital signal. Typically, the digital output is a number proportional to the input. The resolution of the ADC defines the quantization levels that can differentiate the analog input. In this dissertation, it is going to describe a converter for the Internet of Things (IoT) systems.

The IoT is a system of interrelated computing devices, mechanical and digital machines, objects, animals, or people with unique identifiers and the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction.

1.1 Motivation

There are many types of ADCs, such as SAR, FLASH, Pipeline. Each has its advantages and disadvantages. The designer of an ADC always tries to make it faster, smaller and more reliable than the State of the Art. However, the improvement of technology leads to a new concern among analog design, related to the ever-decreasing size of the devices. The reduction in transistor gate-oxide thickness forces the system voltage to decrease, making analog design hard to do. It results from weak bias point operation, gate leakage, reduced input voltage swings, and linearity problems. Therefore, this dissertation offsets some of the design challenges imposed by digitally-driven deep-submicrometer CMOS processes by analyzing time-based or time-mode signal processing (TMSP), [1]. It is a novel approach to manipulate and process analog sample information using digital blocks. In this methodology, conventional voltage and current variables are replaced by time-domain variables such as the time differences between two rising edges, or by the frequency of an oscillator, and logic circuits substitute the large-sized and

power-hungry analog blocks. Moreover, adopting digital elements as the base of analog circuits enables digital synthesis and test methods to be used. It is an important step forward in bridging the design gap between analog and digital design.

1.2 Topic Overview

The analog signals are more frequently in the voltage domain. Therefore, there must have a conversion of the analog input information from the voltage domain to the time-domain. The time-domain variables can either be a change in the frequency of a periodic signal or a time difference between the rise of two different digital signals. In figure 1.1 are shown these two examples.

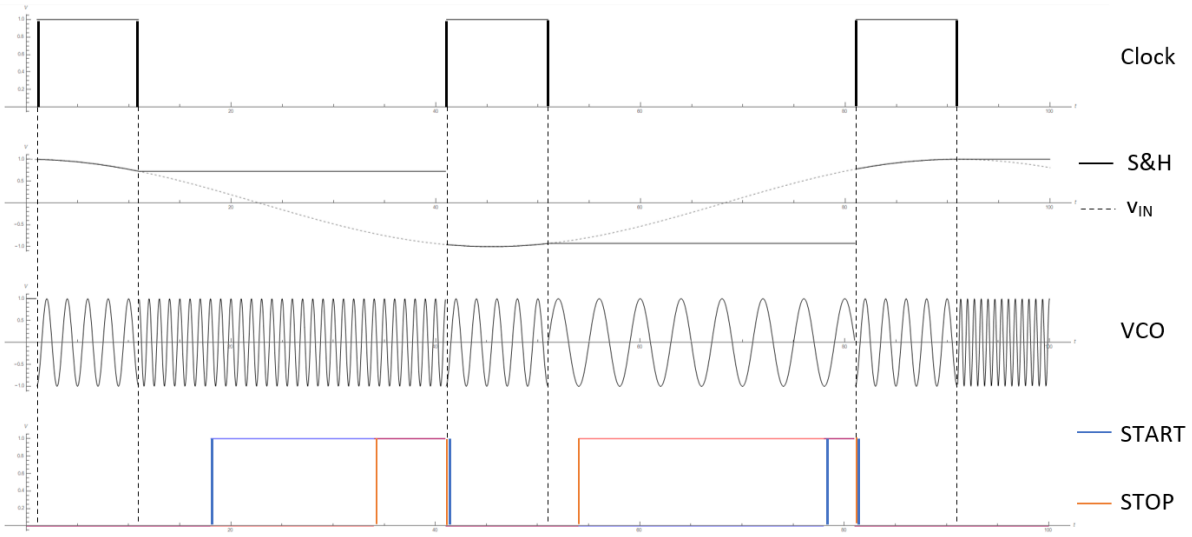


Figure 1.1: Time based Quantization Signals.

Figure 1.1 shows the two types of conversion of the input analog signal, from the voltage domain to time-domain variables. The clock signal, the differential input signal, and the sample and hold signal are common to the two approaches. The Sample and Hold signal follows the input when the clock signal is HIGH, and when the clock signal is LOW, it holds, allowing that the following blocks of the converter be able to quantify the amplitude. The conversion type, in which the time domain variable is frequency, uses a Voltage Controlled Oscillator (VCO). When the clock signal is HIGH, the VCO is at the free-running frequency, and when the clock signal is LOW, the VCO frequency is controlled by the amplitude of the Sample and Hold signal.

In the time interval based conversion type, the time interval between the rising edge time instant of the START and STOP signals is proportional to the differential input's amplitude. If the differential input amplitude is positive, the START signal's rising edge occurs sooner than the STOP signal's rising edge. Otherwise, the STOP signal is the first to rise. When the clock signal is HIGH, these digital signals are LOW.

After converting the input analog signal to time-domain variables, there is a Time-to-Digital Converter (TDC) that quantifies the time-domain information.

1.3 Objectives

One of the objectives of this dissertation is to demonstrate that ADCs using quantization of the input information in the time domain are a viable solution to the problems faced in advanced CMOS technologies, featuring low voltage supply, by taking advantage of the increased speed of digital cells.

A Time Interval Based ADC is designed and simulated, with a TDC based in a Time Domain Folding approach, in Synopsys software. The specifications of the ADC are in the table 1.1.

Resolution	7 bit
Sampling Frequency	2.5GS/s
Input Full Scale	0.5 $V_{PP,diff}$
INL	$\pm$ 0.5 LSB
DNL	$\pm$ 0.5 LSB
ENOB	6
Output Amplitude Variation	$\pm$20 $\%$

Table 1.1: ADC Specification.

1.4 Thesis Outline

This dissertation is organized as follows. Section 2 describes Time Domain Quantization based ADC types and architectures. Section 3 describes the Time Interval Based ADC, with Folding TDC implementation chosen to design the proposed ADC described in this thesis. Section 4 shows the implementation of each block with pre-layout simulations and results. Section 5 show the ADC pre-layout simulation results. Section 6 concludes this dissertation, evaluating the main achievements and describing future work.

Chapter 2

General Time Based Quantization ADC Architectures

The different types of Time Domain Quantization ADCs are categorized in figure 2.1.

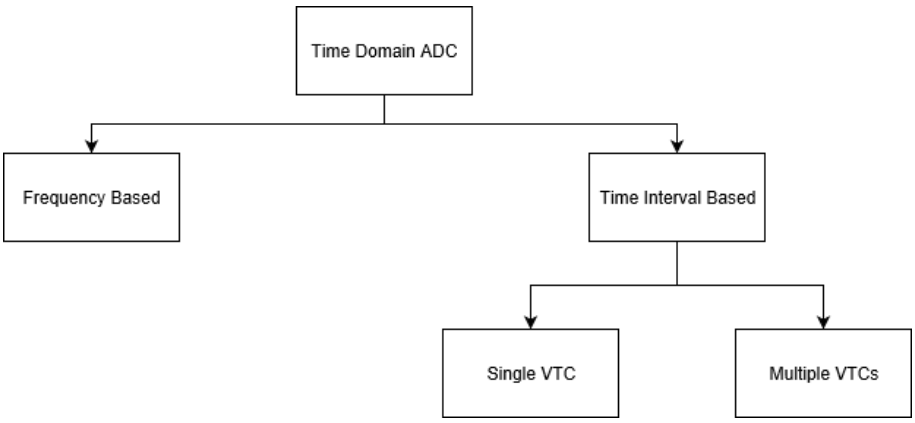


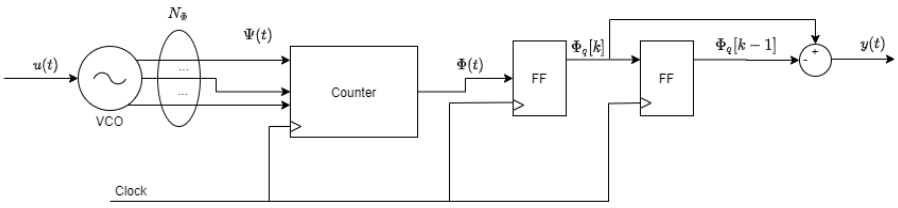
Figure 2.1: Time based ADC Architectures.

Time Domain ADCs convert the analog input in two different ways: by using the amplitude of the analog input to define the frequency of an oscillator (Frequency Based) or by producing two digital signals, where the time interval between the rising edge of both is proportional to the amplitude of the analog input (Time Interval Based). As shown in figure 2.1, Time Interval Based ADCs have two subtypes of Time Interval Based ADCs, based on the number of Voltage to Time Converters (VTCs) used.

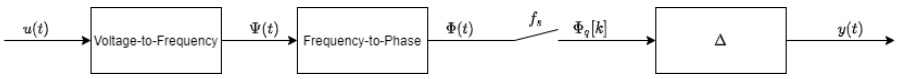
The following subsections will describe different implementations of these ADC types.

2.1 Frequency Based Quantization

The Frequency Based Quantization type of ADC is represented in figure 2.2, [2].



(a) Circuit.



(b) Block diagram.

Figure 2.2: Frequency based ADC.

Figure 2.2(a) shows the architecture of a conventional Frequency Based Quantization ADC, where it consists of a VCO, a Counter, and a differentiator. The VCO converts the analog input signal from the voltage domain to the phase domain. It generates an output signal whose frequency is proportional to the amplitude of the analog input signal. The input voltage signal is converted to a time-based signal. The Counter counts the number of rising (or falling) edges in the VCO's output during the sampling period, thereby quantizing the VCO's phase, $\Phi(t)$, by 2π. In the general case, $\Phi(t)$ is quantized to multiple values of $2\pi/N_\Phi$ with N_Φ the number of output phases of the VCO. By sampling the quantized output $\Phi_q(t)$ at sampling rate $f_s = 1/T_s$ to $\Phi_q[k]$ and taking the first-order difference, the digital output $y[k]$ is obtained. The quantized phase $\Phi_q(t)$ at the end of the sampling period, is the number of the total rising (or falling) edges that the Counter counted. The output signal is proportional to the VCO's frequency, which is proportional to the input's amplitude. Figure 2.3 shows the phase's quantization.

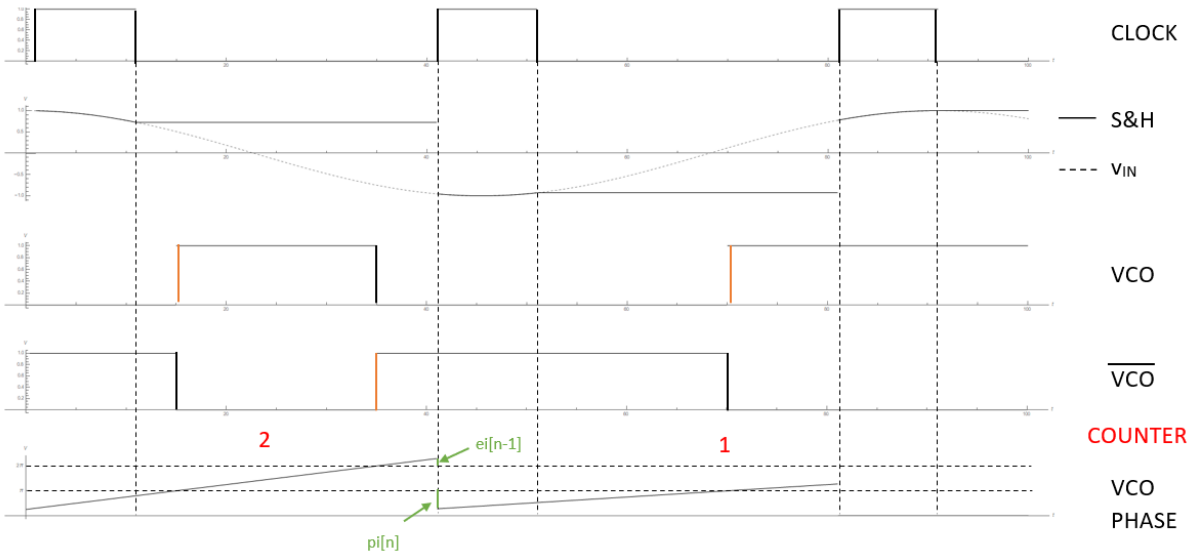
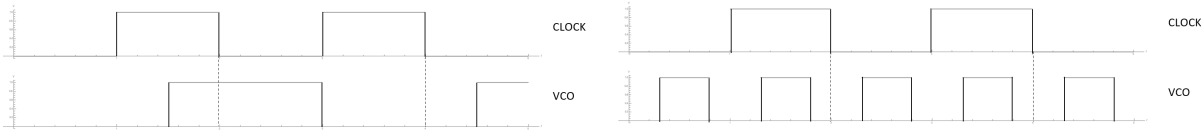


Figure 2.3: Phase's Quantization.

The example of figure 2.3 shows the phase's quantization, using a differential VCO. The VCO's output signal and its complement are used to quantify the phase once the Counter only counts the rising edges of those signals. As two outputs of the VCO are used, the phase is quantified in $2\pi/2 = \pi$ because $N_\Phi = 2$. If the Counter can count the rising and falling edges, only one phase would be necessary, but it would still be $N_\Phi = 2$ because there are two different information sources. In the first sampling period of the example on figure 2.3, there are two rising edges and so $\Phi[k] = 2 \times \pi$. However, a phase signal is periodic with a period equal to 2π. So, $2 \times \pi = 0$. In the second sampling period, there is one rising edge, and so $\Phi[k] = \pi$. It is possible to understand that to increase the resolution is necessary to increase the number of VCO output signals used, decreasing the size of the phase quantization step. As seen in figure 2.3, the quantization error in a sampling period becomes the initial phase at the following sampling period.

There are two types of quantization to quantify the phase of each VCO output, [3].



(a) One Bit Quantization, $f_{VCO} = \frac{2}{3} \times f_{clk}$.

(b) Multi Bit Quantization, $f_{VCO} = 2 \times f_{clk}$.

Figure 2.4: Quantization Types.

On the one hand, if the maximum frequency of the VCO is lower than the sampling frequency, $f_{max} < f_s$, figure 2.4(a), each VCO's output can have zero or one rising (or falling) edge at every sampling period, and so the quantization is done by detecting this edge. It is called one-bit quantization once each VCO's output only needs one bit to count the rising (or falling) edges that occur in one sampling

period. It quantifies the phase in 2π steps. If multiple VCO outputs are used, $N_\phi > 1$, the phase can be quantified in $\frac{2\pi}{N_\phi}$.

On the other hand, if the maximum frequency of the VCO is higher than the sampling frequency, $f_{max} > f_s$, figure 2.4(b), each VCO's output can have multiple rising (or falling) edges at every sampling period and so it is needed a multi-bit counter to count those edges. It is called multi-bit quantization and can quantify phase differences higher than 2π.

The one-bit quantization minimizes the VCO tuning range ($f_{tune} = f_{max,vco} - f_{min,vco}$) since the sampling frequency limits the maximum frequency of the VCO but maximizes the VCO's outputs used to quantify the phase since in this quantization the usage of all VCO's output phases is viable. The multi-bit quantization maximizes the tuning range but reduces the VCO outputs used (usually, this type of quantization only uses one VCO output).

In figure 2.2(a), the analog input, $u(t)$, is presented to an oscillator and will define its frequency. This oscillator converts the analog input into frequency. If the VCO is ideal, the transfer function between the VCO's input signal and its frequency $\Psi(t)$ is

$$\Psi(t) = 2\pi(K_o u(t) + f_o), \tag{2.1}$$

where K_o is the VCO gain ([Hz/V]) and f_o is the free-running frequency of the oscillator, [2, 4].

The phase signal, $\Phi[k]$, at every sampling period, [5], is described by

$$\Phi[k] = \int_{kT_s}^{(k+1)T_s} \Psi(\tau)d\tau + p_i[k], \tag{2.2}$$

where $\Phi[k]$ is the VCO's phase signal, $\Psi(t)$ is the VCO's frequency signal, and $p_i[k]$ is the initial phase at $t = kT_s$. As seen in figure 2.3, the initial phase is equivalent to the previous quantization error, $p_i(kT_s) = e((k-1)T_s)$. The phase is then the previous phase quantization error plus the phase variation, $\Phi_x(t) = \int_{kT_s}^{(k+1)T_s} \Psi(\tau)d\tau$, during the sampling period.

At the output of the counter, there is a flip flop (FF), to quantify phase signal at every instant $t = kT_s$,

$$\Phi_q[k] = \frac{N_\Phi}{2\Pi}(\Phi[k] - e[k]), \tag{2.3}$$

where $\Phi_q[k]$ is the phase quantified, $\Phi[k]$ is the phase, and $e[k]$ is the phase quantization error. The phase quantified, $\Phi_q[k]$, is an integer given by the counting of the Counter, and so there is the factor $\frac{N_\Phi}{2\pi}$ in (2.3) to translate the phase value to an integer.

The last block of this ADC type, figure 2.2(b), is a differentiator between the actual output phase quantified and the previous one. By differentiating phase with respect to time yields frequency. Since VCO's frequency is proportional to the input signal, the output of this differentiator is proportional to the input signal, described by

$$y[k] = \frac{N_\Phi}{2\pi}\left(\Phi_q[k] - \Phi_q[k-1]\right) = \frac{N_\Phi}{2\pi}\left[\Phi[k] - \Phi[k-1] - (\Phi_\epsilon[k] - \Phi_\epsilon[k-1])\right], \tag{2.4}$$

where N_Φ is the number of VCO's output phases.

When the analog input, $u(t)$, is directly the input signal of the VCO, assumed to be a sine wave, with frequency $w_{in} = 2\pi f_{in}[rad.s^{-1}]$, $u(t) = Asin(w_{in}t)$, [2], (2.4) becomes

$$y[k] = Gu(kT_s - T_s/2) + B + e[k] \tag{2.5}$$

where

$$G = N_\Phi K_o T_s sinc(f_{in}T_s),$$

$$B = N_\Phi f_o T_s \text{ and}$$

$$e[k] = -\frac{N_\Phi}{2\pi}(\Phi_\epsilon[k] - \Phi_\epsilon[k-1]).$$

The derivation of this expression is provided on Annex B. T_s is the sampling period, f_o is the free running frequency of the VCO, K_o is the VCO's gain, and f_{in} is the input signal's frequency. The output signal, described by (2.5), has an offset voltage due to the free-running frequency of the VCO. It is directly related to the input, $u(kT_s - T_s/2)$. It can be seen that the input-signal amplitude in the phase domain is a sinc function of the input frequency, where sinc(x) is defined as $sinc(\pi x)/\pi x$. This sinc relation shows that when the input signal is directly applied to the VCO, it has an inherent low pass filter that limits the input bandwidth.

When the input is first sampled, the analog signal presented to the VCO is $u(t) = v_{in}(t)x_a(t) \otimes p(t)$, where $v_{in}(t)$ is the ADC input analog signal, $x_a(t)$ is a sequence of equispaced Dirac impulses ($x_a(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$) and $p(t)$ is a square wave, with period T_s and with duty cycle of τ. The operation $\otimes$ is a convolution. Then, (2.4) becomes

$$y[k] = Hv_{in}(kT_s) + B + e[k] \tag{2.6}$$

where

$$H = N_\Phi K_o \tau,$$

$$B = N_\Phi f_o T_s \text{ and}$$

$$e[k] = -\frac{N_\Phi}{2\pi}(\Phi_\epsilon[k] - \Phi_\epsilon[k-1]).$$

The derivation of this expression is provided on Annex B. Equation (2.6) shows that when the input signal is first sampled, the output signal has a linear relation with the input signal, $v_{in}(kT_s)$, and the gain between the input signal and the output signal is related to the number of output phase, N_Φ, the VCO gain, K_0, and the duty cycle factor, $\tau =]0, 1[$.

The output signal, $y[k]$ in (2.4) has a term that is propotional to the analog input and a terma that shapes the error, $\frac{N_\Phi}{2\pi}(\Phi_\epsilon[k] - \Phi_\epsilon[k-1])$. It is important to analyze the frequency response of the output signal, to analyze the error's shape.

2.1.1 Frequency Response

In this section, the previous equations are analyzed in the frequency domain. Taking the z transform of (2.4) yields

$$Y(z) = \frac{N_\Phi}{2\pi}(1 - z^{-1})(\Phi(z) - \Phi_\epsilon(z)). \tag{2.7}$$

From (2.7), it is possible to take the noise transfer function, $NTF = \left(\frac{Y(z)}{\Phi_\epsilon(z)}\right)|_{\Phi(z)=0}$, and the signal transfer function, [2], $STF = \left(\frac{Y(z)}{\Psi(z)}\right)|_{\Phi_e=0}$, described by

$$\begin{cases} NTF(z) \approx \frac{N_\Phi}{2\pi}(1 - z^{-1}) \\ STF(z) \approx \frac{N_\Phi}{2\pi}\frac{(1+z^{-1})}{2}. \end{cases} \tag{2.8}$$

The *NTF* describes the relation between the output and the phase error if there is no input signal, and the *STF* describes the relation between the output and the frequency of the VCO if there is no phase error.

The *STF* shows that the output signal is just an average between consecutive samples. This leads to some problems. Analysing a sinusoidal input signal with period T_{in} and correspondent frequency f_{in}, as seen in the figure 2.5, it has symmetric values at time instants $t = T_{in}(\frac{1}{2} + k)$, i.e, $v_{in}(t) = -v_{in}(t + T_{in}(\frac{1}{2} + k))$.

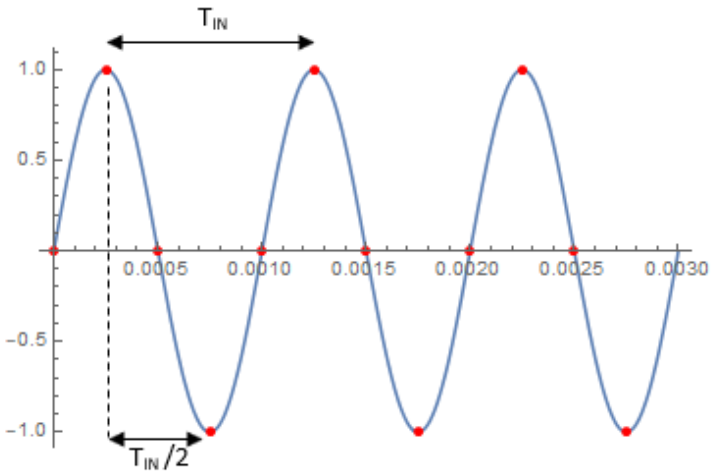


Figure 2.5: Input signal and samples at every $t = kTin/4$.

Since samples are taken at every T_s, if $T_s = T_{in}(\frac{1}{2} + k)$, the samples will always be symmetric. It means that if $f_{in} = f_s(\frac{1}{2} + k)$, the ADC's output signal will have no information about the input signal because the consecutive samples cancel each other due to the averaging. The cancellation is not a particularly bad thing once this frequency is the well known Nyquist frequency, $f_{nyq} = f_s/2$, which is the maximum bandwidth of an ADC. Figure 2.6 shows two examples, one with an input signal with low frequency ($f_{in} = 0.1f_s$) and other with a high frequency ($f_{in} = 0.48f_s$).

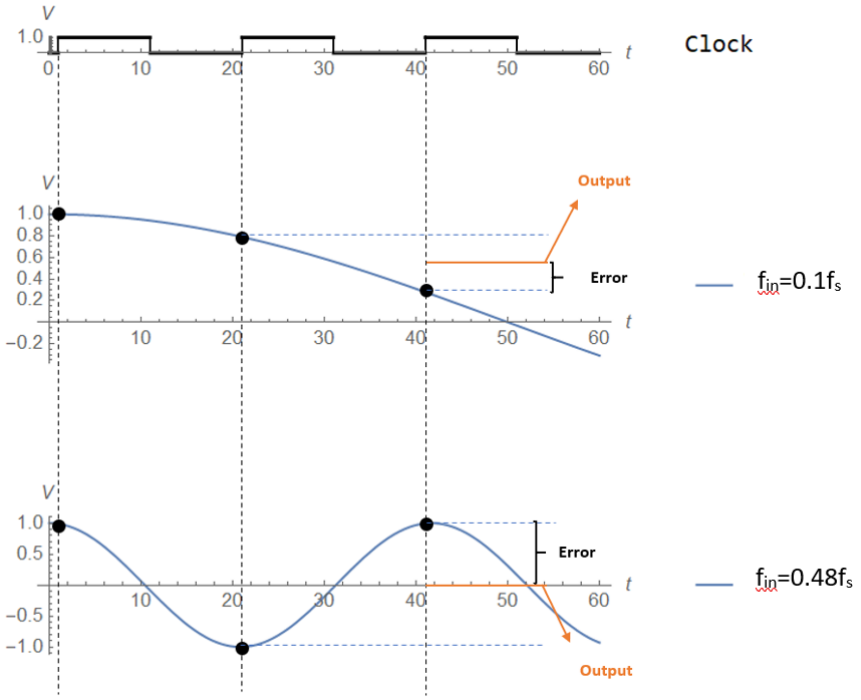


Figure 2.6: Sample Averaging and Error.

As seen in the figure 2.6, for a fixed sampling period, T_s, if the input frequency is low (for example, $f_{in} = 0.1 \times f_s$) two consecutive samples have similar values, the average between them near results in a value close to the samples' value leading a small error. As the input frequency increases to near $\frac{f_s}{2}$, the average of the consecutive samples converge to zero since they become near symmetric, and the error increases. For this reason, this type of ADC requires an oversampled input signal, which means that the maximum frequency of the input signal is much smaller than the sampling frequency. As the error increases with the increase of the input frequency, the ADC has a high pass characteristic.

To prevent the high pass characteristic and increase the input bandwidth there is possibility of time interleaving N identical ADCs. The sampling period of each ADC becomes $T'_s = N \times T_s$. The cancellation of samples, due to the averaging, now happens when $T'_s = NT_s = T_{in}(k + \frac{1}{2})$. It shows that with N time-interleaved ADC blocks if the input frequency is $f_{in} = \frac{f_s}{N}(k + \frac{1}{2})$ the output does not have information of the input signal, and the error is maximum. However, due to periodicity the input signal, is the smae at $t = kT_{in}$. Then, if $T'_s = NT_s = T_{in}k$, the samples will be equal, for each ADC. So if $f_{in} = \frac{f_s}{N}k$, the output signal does not have an error due to the averaging, which means that the signal transfer function is maximum and the error is null. Therefore, the high pass characteristic becomes a bandpass characteristic.

These results can be demonstrated mathematically. Generalizing (2.8) for an implementation of N Interleaved ADCs, where the transformation between the z plane and the frequency domain is made by $z = e^{sT'_s} = e^{jwT'_s} = e^{jwNT_s}$. It leads to

$$\begin{cases} NTF(\omega) \approx \frac{N_\Phi}{2\pi}\left(1 - e^{-j\omega N T_s}\right) = \frac{N_\Phi}{2\pi}\left(2je^{-j\omega N\frac{T_s}{2}} sin(\omega N\frac{T_s}{2})\right) \\ STF(\omega) \approx \frac{N_\Phi}{2\pi}\frac{\left(1+e^{-j\omega N T_s}\right)}{2} = \frac{N_\Phi}{2\pi}e^{-j\omega N\frac{T_s}{2}} cos(\omega N\frac{T_s}{2}). \end{cases} \tag{2.9}$$

From (2.9) is possible calculate the frequencies that correspond to the maximum and zeros of the *NTF* and *STF*:

$$|NTF(\omega)| = 0 \leftrightarrow \omega = \frac{i}{N}\omega_s,$$

,

$$|NTF(\omega)|_{max} \rightarrow \omega = \frac{\omega_s}{N}\left(\frac{1}{2} + i\right),$$

$$|STF(\omega)| = 0 \leftrightarrow \omega = \frac{\omega_s}{N}\left(\frac{1}{2} + i\right) \text{ and}$$

$$|STF(\omega)|_{max} \rightarrow \omega = \frac{i}{N}\omega_s$$

which is consistent to what was discussed before.

The fact that the STF has zeros for frequencies in the range of $[0, \frac{f_s}{2}]$ makes this type of ADC unable to produce an output that has information of the analog input signal for those frequencies.

In [6] is shown that increasing factor N increases the NTF but also increases the ADC's resolution and they cancel each other in the SNR calculation. Hence, a Frequency Based Quantization ADC is suitable for time-interleaving. Moreover, each time-interleaved ADC operates at 1/Nth the sampling frequency, relaxing the requirements for CMOS operating speeds. It should be also noted that for the zeros not at $\omega ==$ and $\omega = \pi$, the center frequency of the input can be placed exactly at the zero of the NTF. In those cases, the noise power is twice that of the half-bandwidth case since the noise is integrated over. Thus, placing the signal center frequency on the zero of the NTF results in an SNR increase of 6 dB, which is equivalent to 1 bit of ENOB.

2.1.2 ADC Design

When using a VCO and a counter, the resolution of the quantization block, [4–6] is

$$Resolution = log_2\left(\frac{f_{max} - f_{min}}{f_s}\right) + log_2(N_\phi). \tag{2.10}$$

As seen in (2.10), the resolution of this type of ADC depends on the sampling frequency (f_s), on the tuning frequency range of the VCO ($f_{tune} = f_{max} - f_{min}$) and on the number of outputs of the VCO (N_Φ).

By analyzing (2.10), the resolution increases with the increase of the number of outputs of the VCO, N_Φ. The maximum number of VCO's outputs is the number of delay cells, N_d. As, the maximum and minimum frequencies of the VCO are given by

$$\begin{cases} f_{max} = \frac{1}{2 \times N_d \times T_{d,min}} \\ f_{min} = \frac{1}{2 \times N_d \times T_{d,max}}, \end{cases} \tag{2.11}$$

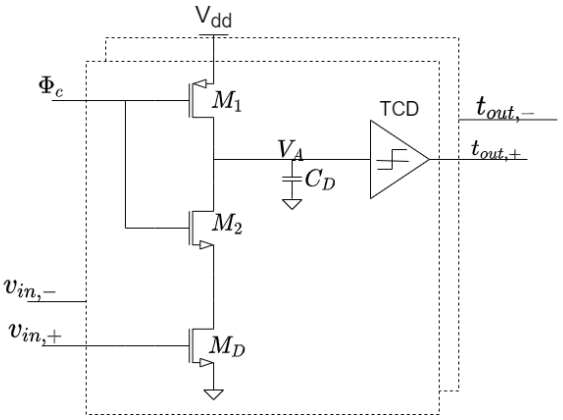
where $T_{d,min}$ is the minimum delay of a single delay cell in the oscillator and N_d is the number of delay stages, (2.10) becomes

$$Resolution = log_2 \left[\frac{1}{f_s} \times \frac{1}{2 \times N_d} \times \left(\frac{1}{T_{d,min}} - \frac{1}{T_{d,max}} \right) \right] + log_2(N_\phi). \tag{2.12}$$

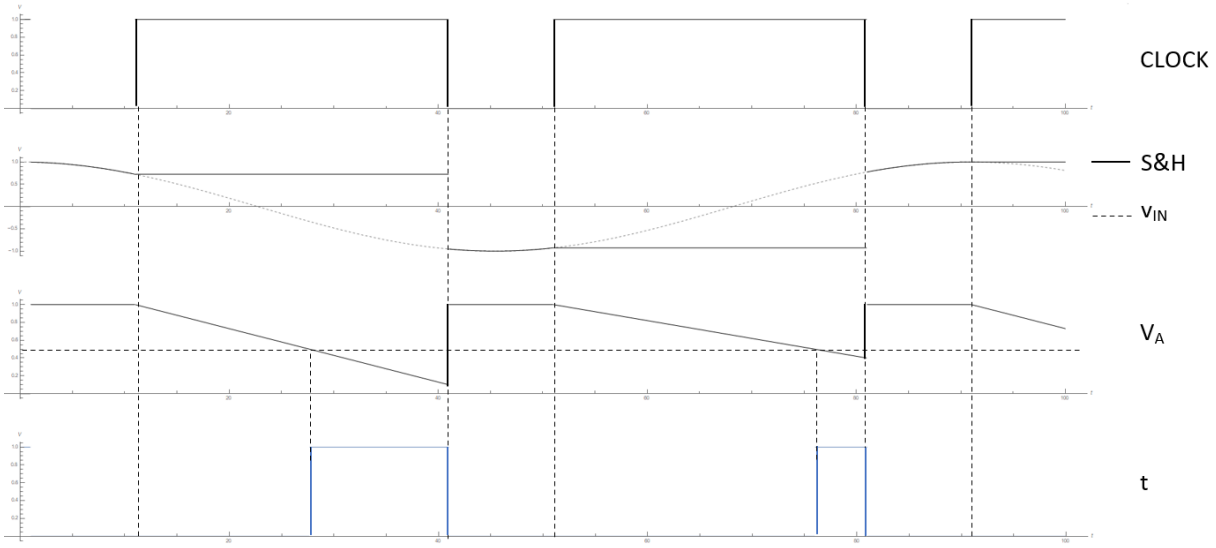
In (2.12) is possible to see that if the number of delay stages, N_d, increases, the resolution decreases. Then, there is a trade-off between the tuning range and the number of output phases of the VCO to get the resolution desired.

2.2 Time Interval Based Quantization

Another time-domain quantization is based on the time interval between two digital signals. These digital signals are the outputs of Voltage-to-Time Converters (VTCs). VTCs converts the amplitude of the analog input from the voltage domain to a time interval between the rising edge of two digital signals. For higher input signal amplitude, the higher is the time difference between the digital signals. A VTC type (CSI Based) is represented in figure 2.7, [1, 7].



(a) VTC basic circuit.



(b) Signals.

Figure 2.7: CSI Based VTC.

The working process, [1, 7], of the circuit represented in figure 2.7(a), is shown in the figure 2.7(b). When the clock signal $\Phi_c = 0$, the capacitor, C_D, is charged to the supply voltage, i.e, $V_A = V_{DD}$. Then, when $\Phi_c = 1$, the capacitor is discharged at a rate proportional to the corresponding analog input voltage, since this voltage controls the current flowing in transistor M_D.

Then, there is a threshold cross detector (TCD), whose output goes to the level logic High when the voltage V_A is lower than the threshold voltage (V_{TH}). Usually, this threshold voltage is half of the supply voltage ($V_{TH} \approx V_{DD}/2$). M1 and M2 are designed to not enter the triode region after the rising edge of the output signal, [8]. The input analog signal, assumed to be a sinusoidal signal defined by $v_{IN} = Asin(\omega t)$, is used as a differential signal,i.e, $v_{in} = v_{in,+} - v_{in,-}$, where $v_{in,+} = \frac{A}{2}sin(\omega t)$ and $v_{in,-} = \frac{-A}{2}sin(\omega t)$. Then, $v_{in,+}$ has a corresponding digital signal at the output of the VTC, $t_{out,+}$ and so does $v_{in,-}$, $t_{out,-}$. As seen in figure 2.7, the VTC is composed of two parallel blocks, represented by the dash lines. These blocks are named Voltage Controlled Delay Unit (VCDU), [1].

The time-domain quantization ADCs based on time interval can either use one VTC or multiple VTCs. If there is just one VTC, it is used to make the conversion between the voltage domain to time-domain

and then the quantization is all made in the time domain by a Time-to-Digital Converter (TDC). However, if there are multiple VTCs the conversion and the quantization are made simultaneously.

2.2.1 Single VTC

As said before, using a single VTC leads to all quantization of the analog signal be done in the time domain. To perform the quantization, there is a TDC, as represented in figure 2.8.

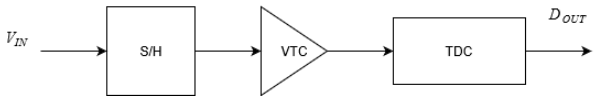


Figure 2.8: Time interval Based ADC, with a single VTC and a TDC.

This type of architecture is mainly used to replace traditional Flash architecture with Flash TDCs. Figure 2.9 represents a Flash TDC.

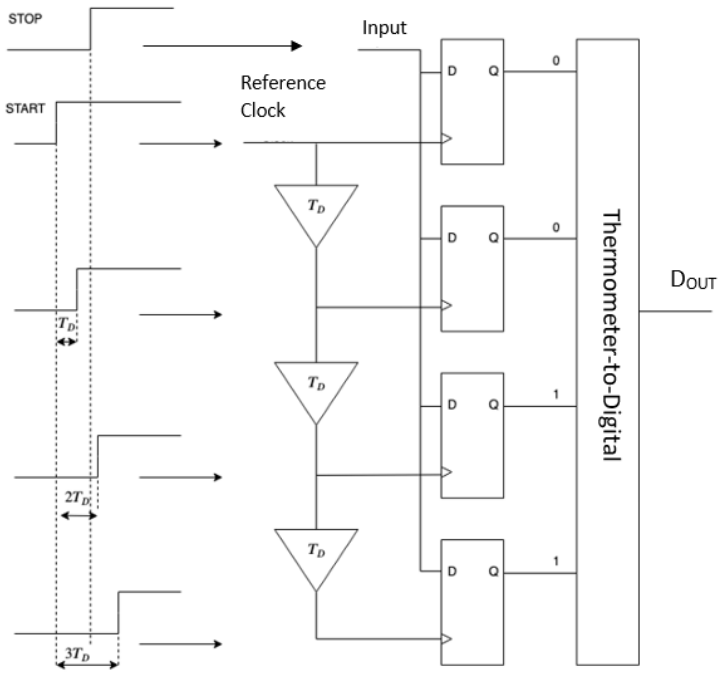


Figure 2.9: Flash TDC.

Comparing the Flash TDC of the figure 2.9 with the traditional Flash ADC, a delay cell ladder replaces the resistive ladder, and Flip Flops(FFs) replace the comparators. So, there are $2^{bits} - 1$ delay cells and 2^{bits} Flip Flops, where $bits$ is the ADC's resolution. In this type of architecture, the negative output of the VTC $t_{out,-}$, is usually labeled as *STOP*, and the positive output of the VTC, $t_{out,+}$, is labeled as *START*. As represented in figure 2.9, the thermometer code at the output of the Flip Flops represents the time interval between the rising edge of the *START* and the *STOP* signal, by time delays (T_D).

To ensure that T_D is known reasonably accurately, [1], the delay chain is often implemented and

stabilized by a delay-locked loop (DLL), figure 2.10.

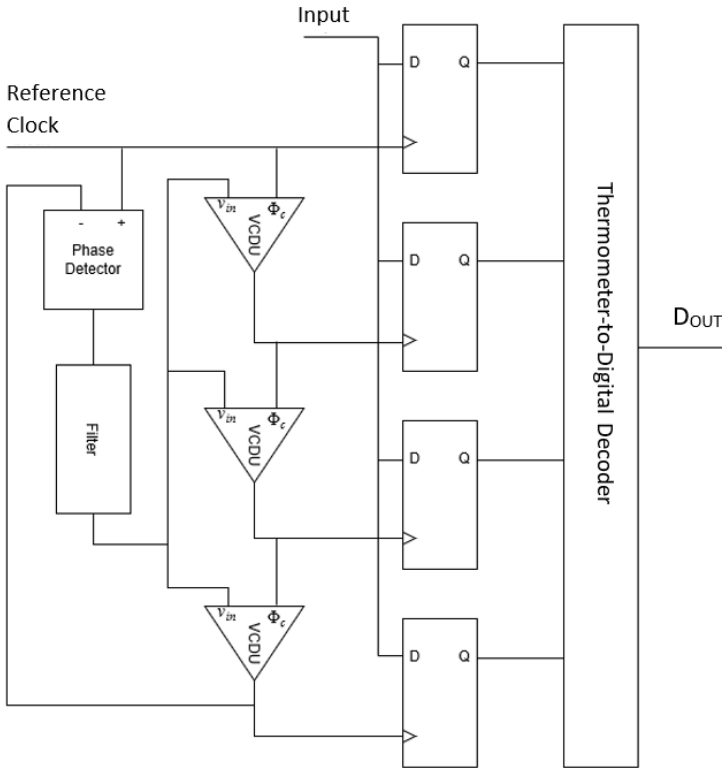


Figure 2.10: Flash TDC with DLL.

The delay chain is used to delay the clock signal. The delayed signal is compared with itself, and the phase difference is obtained. Then, there is a phase detector that controls the input voltage of the VCDUs, through negative feedback. The time delay (T_D) is controlled by controlling the input voltage of the VCDUs. The drawback of this implementation is the temporal resolution can be no higher than the delay through a single gate in the semiconductor technology used. To achieve a sub gate temporal resolution the flash converter can implement a Vernier delay line, as shown in figure 2.11.

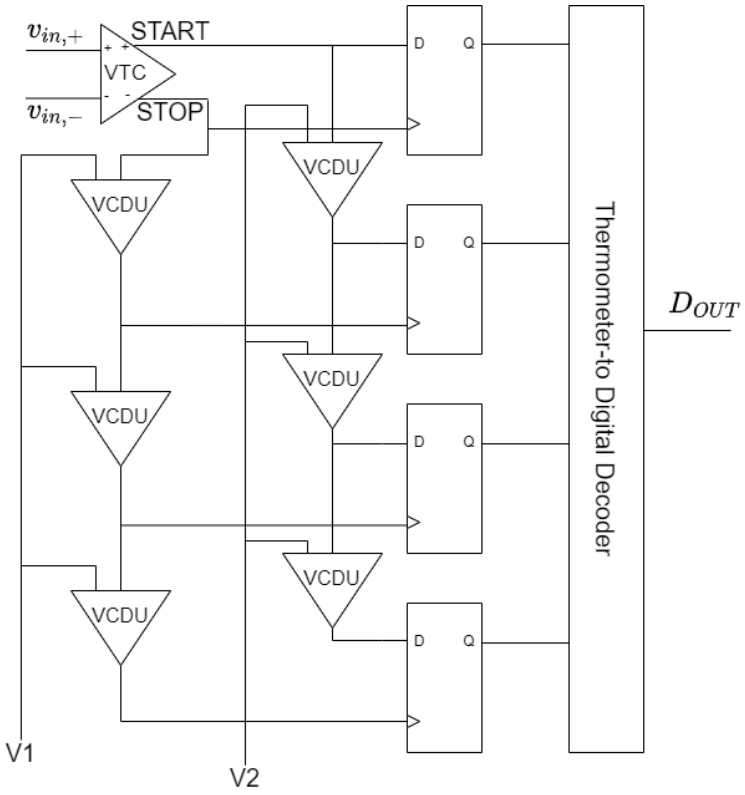


Figure 2.11: Flash TDC with Vernier Line.

The architecture achieves a resolution of τ_1-τ_2, where τ_1 is the time delay defined by the reference voltage $V1$, τ_2 is the time delay defined by the reference voltage voltage $V2$, and $\tau_1 > \tau_2$. Again, two individual DLLs should be implemented for each delay chain to make them reasonably accurate.

In this implementation, with Vernier lines, it is easy to see that there are 2^{bits} Flip Flops that act as time comparators and $2 \times (2^{bits} - 1)$ delay cells. So, to reduce the amount of Flip Flops and the number of delay cells, it is analyzed a folding approach, [7].

Time Domain Folding

The main idea of Folding is to quantify the most significant bits (MSBs) by a coarse quantizer, and the least significant bits (LSBs), by a fine quantizer, simultaneously, as seen in figure 2.12. This approach needs an auxiliary ring oscillator, which is part of the fine quantizer.

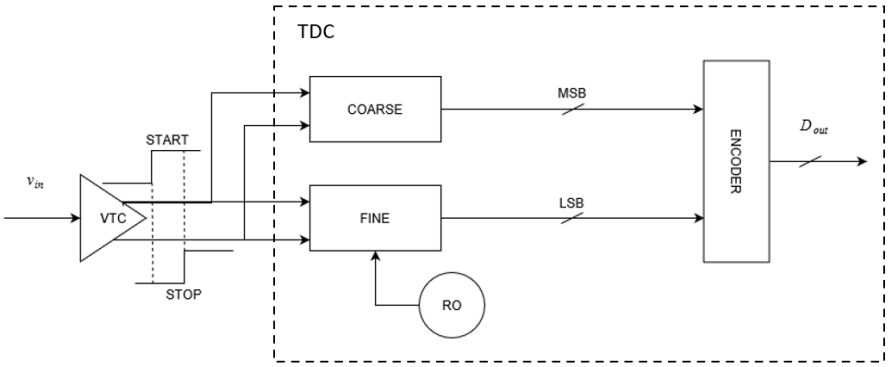


Figure 2.12: Basic time domain folding block diagram.

The operation of the folding circuit is illustrated in figure 2.13, where the transfer function of the folding circuit is given.

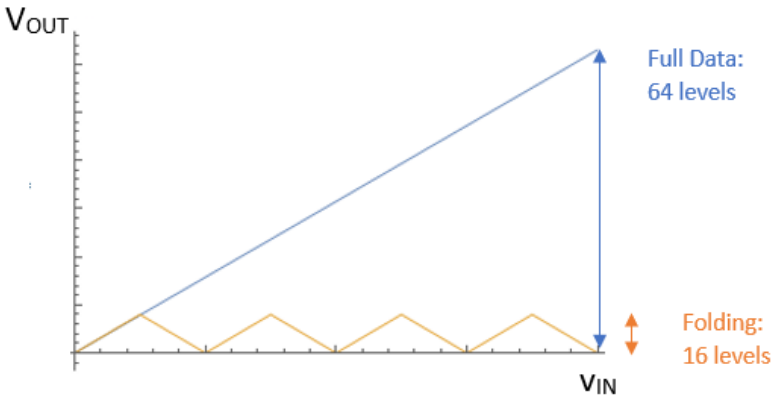
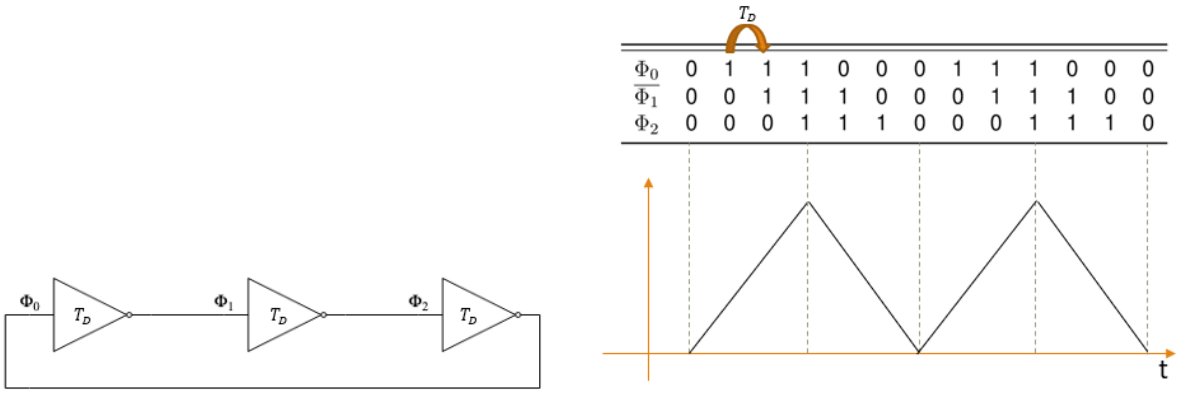


Figure 2.13: Transfer curve of folding circuit in comparison with transfer curve of a full ADC's output.

As seen in figure 2.13, the folding circuit folds the input range into 2^n folds, each with 2^{N-n} levels, where N is the full ADC's resolution, and n is the coarse quantizer resolution. In the example of figure 2.13, $N = 6$ and $n = 2$. The Folding codes correspond to the least significant bits (LSBs) of the ADC's output code. The n-bit coarse quantizer is required to identify to which fold the input voltage corresponds, generating the n most significant bits (MSBs). The coarse quantizer and the fine quantizer generate the n MSBs and the $N - n$ LSBs synchronously. The concept of time-domain folding is illustrated in figure 2.14, [7].



(a) Three stage Ring Oscillator.

(b) Fine Quantifier Transfer Function.

Figure 2.14: Concept of time-domain folding.

Let us take a three-stage RO as an example. The RO is free running, and periodic oscillatory waveforms appear on the three internal nodes, ϕ_0, ϕ_1, and ϕ_2. If we record ϕ_0, $\overline{\phi_1}$ (the inversion of ϕ_1) and ϕ_2 collectively for some time, we can observe a thermometer-like digital code (represented together by ϕ_0, $\overline{\phi_1}$ and ϕ_2) circulating among six codes per RO period. The repeating nature of the oscillation gives rise to the folding operation in the time domain. The time-lapse between two consecutive thermometer codes corresponds to exactly one inverter delay. Therefore, it represents the LSB size of the quantizer. Thus, RO provides a compact realization of signal folding and quantization in the time domain. Compared to voltage-domain folding operations, time-domain folding provides two distinctive advantages. First, voltage-domain folding is quite non-linear, while time-domain folding using RO results in an inherently linear operation. Secondly, time-domain folding, given enough conversion time, yields an infinite folding factor, whereas it is limited by the number of folding amplifiers in the voltage domain. Thus, time-domain folding is also very efficient.

As seen in figure 2.12, the ADC's architecture uses a VTC to convert the input signal from the voltage domain to the time domain, and a TDC that includes the folding circuit, with the coarse quantizer and the fine quantizer, and also includes the Encoder. The VTC generates two digital signals (*START* and *STOP*) and the time interval between them is proportional to the input signal amplitude. Each digital signal will sample a state of the folding circuit and the ADC's output signal is given by the difference between the two states. The ADC's output code is the variation of the folding codes between the rise of the digital signals at the VTC's output. Thanks to the free-running RO, the start and stop points of each quantization event are randomized from sample to sample, resulting in an inherent DEM operation. The DEM does not eliminate mismatch errors but converts them into white noise.

As said before, the coarse quantizer has the function to identify in each fold the amplitude of the analog input resides on. So, in the time-domain, a one-time quantization step in the coarse quantizer must be equal to the period of the fine transfer function characteristic, as illustrated in figure 2.15.

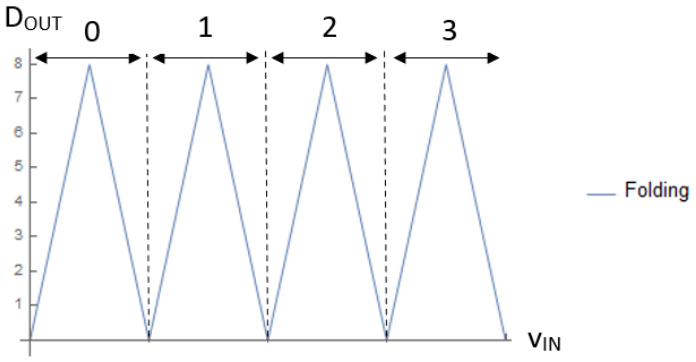


Figure 2.15: Fold identification by the coarse quantizer.

However, a mismatch between the coarse quantizer and the period of the fine's transfer function characteristic leads to an error in the output code. To prevent errors due to the mismatch usually is added a bit (redundancy bit) to the coarse quantizer. This bit allows the coarse quantizer to identify which slope corresponds to the input.

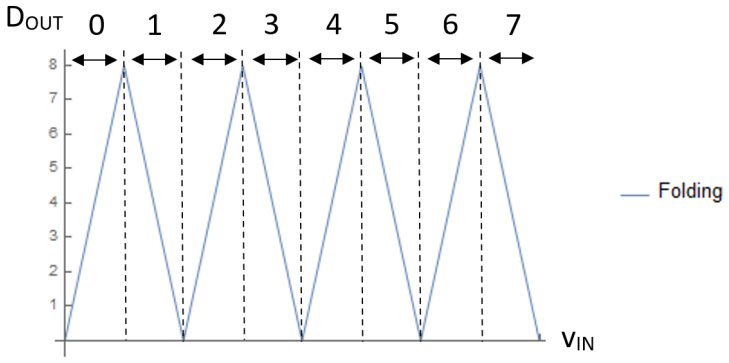


Figure 2.16: Fold identification by the coarse quantizer, with redundancy bit.

With a redundancy bit, is easier to identify mismatches between the coarse and the fine quantizer. This bit does not belong to the coarse quantizer resolution, once it is only used to prevent errors from the mismatch between the coarse and the fine quantizer. Therefore, in a N_{coarse} bits' coarse quantizer with a redundancy bit, the slope identification is done with $N_{coarse} + 1$ bits.

In ADCs that implement this folding approach, the input voltage full scale, V_{FS}, is limited by the maximum time interval that the TDC can process. If the total N bits of the ADC are divided into N_{coarse} bits to the coarse quantizer and N_{fine} bits to the fine quantizer, there are $2^{N_{coarse}}$ folds and in each fold there are $2^{N_{fine}}$ quantization steps, due to $2^{N_{fine}-1}$ delay cells in the RO. So, the maximum time interval that the TDC can quantify is $\Delta t_{max} = 2^{N_{coarse}} \times (2 \times 2^{N_{fine}-1} \times T_D)$, where $2 \times 2^{N_{fine}-1} \times T_D$ is the time interval of a single fold. The resulting resolution of this ADC is $N = N_{coarse} + N_{fine} + 1$, once the MSB can be determined by computation of the states' difference.

2.2.2 Flash ADC with Multiple VTCs

It is also possible to implement a Flash ADC in the Time Domain, with multiple VTCs as represented in figure 2.17, [9–13].

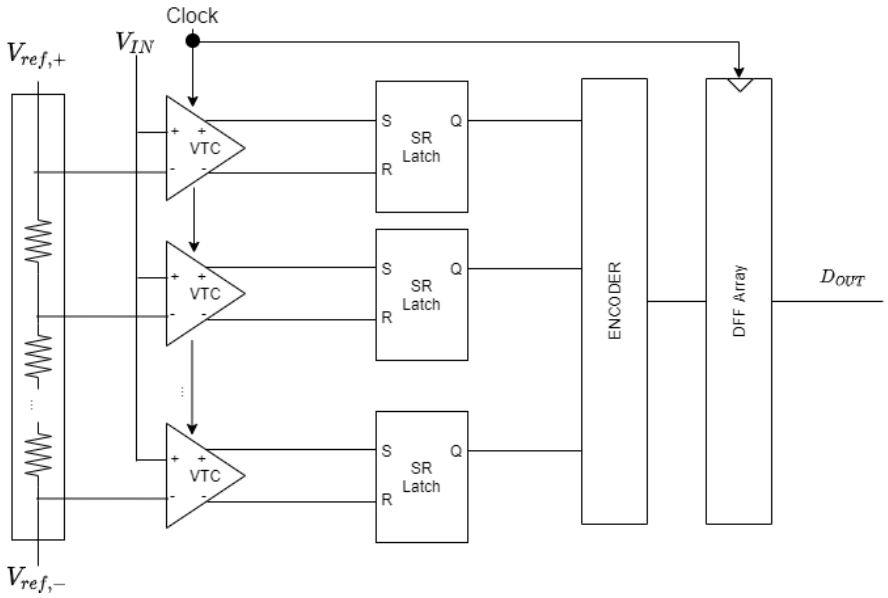


Figure 2.17: Flash ADC using VTCs.

The architecture of figure 2.17 is quite similar to most common Flash architectures in the voltage domain, but in this case, VTCs replace the comparators and latches make the decisions, acting as time comparators. If the amplitude of the positive input of a VTC is higher than the negative, the positive output will rise sooner. Consequently, as the Set input of the corresponding VTC's Latch has a rising edge sooner than the Reset input, it stores the logic level '1'.

As seen in figure 2.17, this flash ADC architecture needs 2^N VTCs and 2^N Latches for an N bit resolution ADC. It leads to a big area ADC with high consumption. On the one hand, a Time Domain Interpolation technique can reduce the number of needed VTCs and Latches. On the other hand, a Time Domain Folding can improve the area's efficiency and power consumption by reducing the number of Latches.

Time Domain Interpolation Flash ADC

The Flash ADCs are the fastest type. However, they have high energy consumption and high area occupation because, for an N bit resolution, they need 2^N VTCs and 2^N Latches in the Time-Domain. However, implementing interpolation in Flash ADCs reduces the amount of VTCs needed by an interpolation factor (IF), keeping the Flash ADC's speed. A Time-Domain Interpolation technique can reduce the number of VTCs and Latches, as illustrated in figure 2.18.

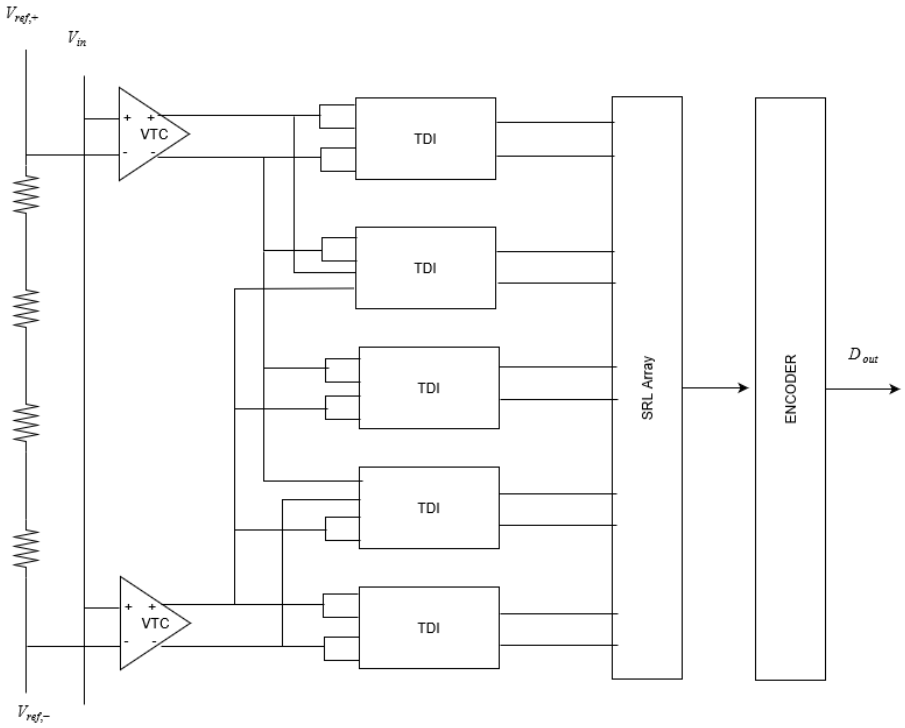


Figure 2.18: Basic block diagram of time domain interpolation Flash ADC.

As seen in figure 2.18, when implementing an interpolation approach, the number of VTCs reduces to $2^{bits}/IF$. In this example $IF = 4$. Interpolating the output of the existing VTCs generates the information of the eliminated VTCs. In the time domain, Time Domain Interpolators (TDI) perform the interpolation. The TDI circuit is in figure 2.19.

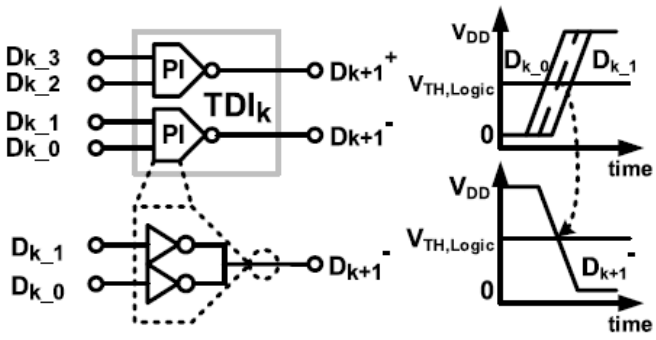


Figure 2.19: TDI Circuit, adapted from [9].

The TDI cell, shown in figure 2.19, is composed of two-phase interpolators. The interpolators are composed of two inverters with the outputs connected. If the input D_{K_0} rises from Low to High at time instant t_1 and D_{K_1} does it at t_2, the output of the phase interpolator falls from High to Low at $t = \frac{t1+t2}{2}$.

Time Domain Folding

In figure 2.20 is shown the transfer function characteristic of the folding approach with multiple VTCs. The horizontal axis is the differential amplitude of the analog input, v_{IN}. The vertical axis is the time instant the rises of the VTC's digital output signals occur.

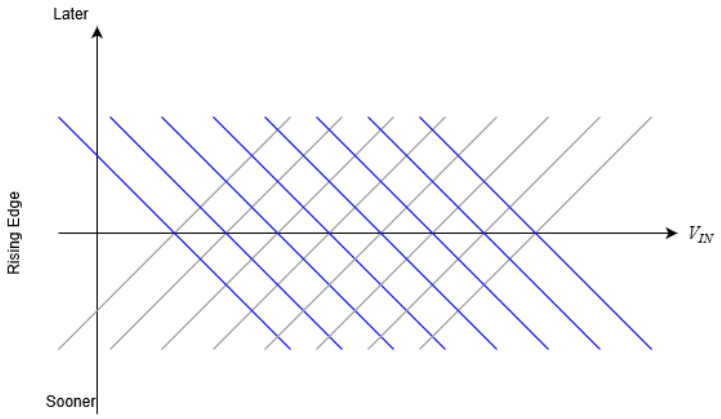


Figure 2.20: Dependence of the VTC's outputs with respect to the amplitude of the analog input.

In figure 2.20, the blue lines correspond to the signals of the positive output of the VTCs, t_+, and the grey lines to the negative output, t_-. Parallel lines correspond to different VTCs, with different differential amplitude inputs. The differential amplitude of the analog input (V_{IN}) relates with the inputs of the VTC by $V_{IN} = v_{in,+} - v_{in,-}$. So, if V_{IN} is increased by v_d, $v_{in,+}$ is increased by $\frac{v_d}{2}$ and $v_{in,-}$ is decreased by $\frac{v_d}{2}$. Then, when V_{IN} increases, the rise of $t_{out,+}$ will happen sooner, due to the increase of $v_{in,+}$ and the rise of $t_{out,-}$ will happen later, due to the decrease of $v_{in,-}$.

From a visual view, the folding approach combines different transfer functions (blue and grey lines) to produce a "zig-zag" shaped transfer function. For that, digital cells are used, OR and AND gates. Figure 2.21 represents the output of the logic gates for two input digital signals $t_{out,1}$ and $t_{out,2}$.

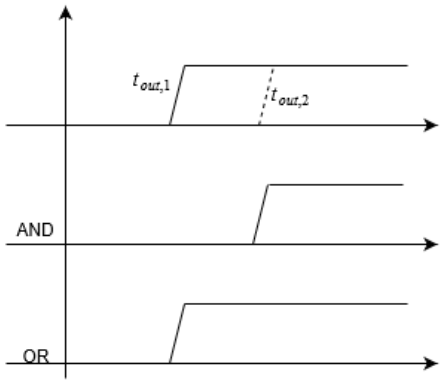


Figure 2.21: AND and OR gates as time selectors.

As seen in figure 2.21, the OR gate selects the signal, the one who has the rising edge that occurs first, and the AND gate selects the slower signal, the one who rises later. The usage of these digital

cells to create the transfer function is shown in figure 2.22.

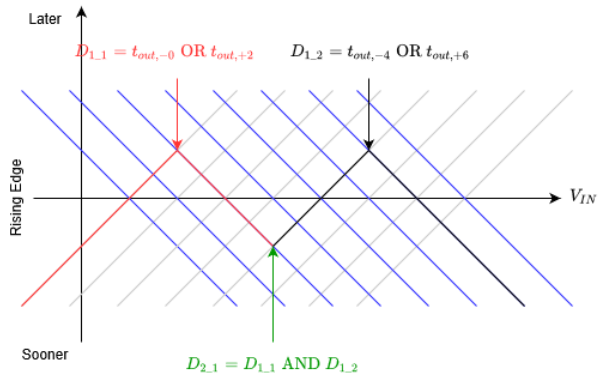
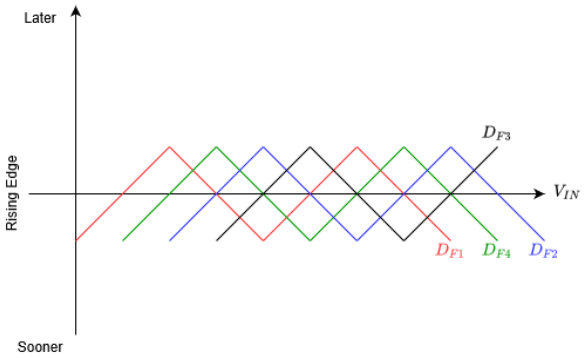


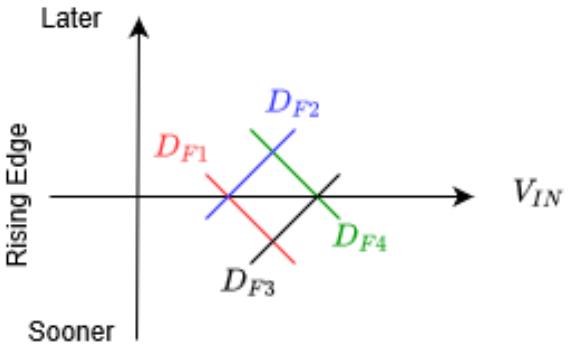
Figure 2.22: Folding result.

As illustrated in 2.22, first is made an OR operation between a negative output and a positive output of different VTCs, to define the peaks. Then, it is made an AND operation to define the minimums.

As seen in figure 2.22, the output of the OR gate selects the signal that is below the cross of two signals, and the AND the above one. One more AND operation produces periodic triangular waves, figure 2.23(a). Four triangular waves compose a fold, as illustrated in figure 2.23(b).



(a) Periodic Triangular Waves.



(b) Fold.

Figure 2.23: Folding with Digital Cells.

To produce quantization steps per fold, four triangular waves are interpolated two-by-two, as shown in figure 2.24.

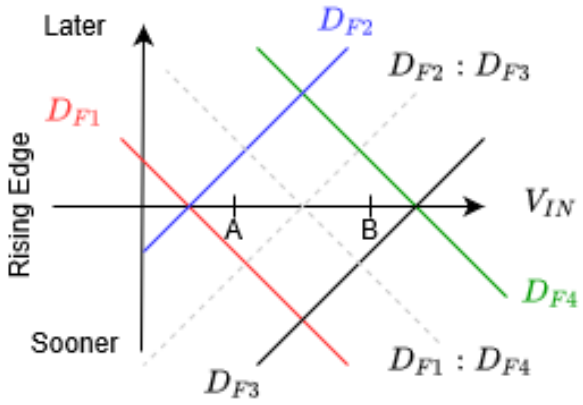


Figure 2.24: Interpolation to Produce Steps.

. One bit interpolation is shown in figure 2.24. The cross between the signals $D_{F1} : D_{F4}$ and $D_{F2} : D_{F3}$ divide the fold in two quantization steps, [14]. As seen in the figure, if the amplitude of the analog input is A, the rise of the signal $D_{F2} : D_{F3}$ occurs sooner then the rise of $D_{F1} : D_{F4}$, but if the amplitude of the analog input is B, the rise of the signal $D_{F1} : D_{F4}$ occurs first then the rise of $D_{F2} : D_{F3}$. Using an SR Latch, where the Set input is $D_{F2} : D_{F3}$ and the Reset input is $D_{F1} : D_{F4}$, if the amplitude of the analog input is A, the Latch will store the logic level HIGH, and if the amplitude of the analog input is B, the Latch will store the logic level LOW. To increase the number of quantization steps the interpolation must be multi-bit, once there are 2^n quantization steps in each fold with an n bit interpolation.

2.3 Two Step

Each of the previous ADC types can implement a two-step approach. Figure 2.25 shows the implementation of an ADC in a two-step approach, [8, 15, 16].

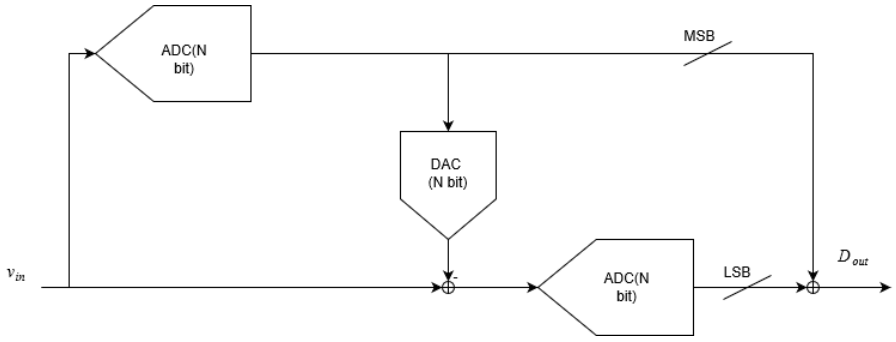


Figure 2.25: Two Step ADC.

In figure 2.25 there is a coarse quantizer and a fine quantizer. The coarse quantizer output is the input of a Digital to Analog Converter (DAC). The output of the DAC subtracts the analog input of the ADC. The fine quantizer quantifies the result of the subtraction. The overall resolution is the sum of

the coarse resolution and the fine resolution, where the resulting bits of the coarse quantizer is the MSB (Most Significant Bits), and the resulting bits of the fine quantizer are the LSB (Least Significant Bits). The usage of this type of ADC allows reducing the resolution requirements of each quantizer. For example, the resolution in a frequency-based ADC is $N = log_2(\frac{f_{max}-f_{min}}{f_s} = log_2(\frac{\Delta f}{f_s}$, where Δ_f is the VCO frequency interval where its transfer function is linear. If the resolution drops to N/2 and the sampling frequency (f_s) remains constant, the VCO frequency interval drops to $\Delta f/2$, which leads to an easier design of the VCO. In another example, an N bit resolution Flash ADC, without folding or interpolation in the time-domain needs 2^N VTCs and Latches. However, if the ADC implements a two-step approach, where each quantizer is responsible for $N/2$ bits, it only needs $2^{N/2}$ of both to each quantizer. Then, the number of VTCs and Latches reduces to $2 \times 2^{N/2}$. However, this approach leads to a conversion that needs two clock periods, one for each quantizer. In conclusion, a two-step N bit ADC has half of the conversion rate of a single N bit ADC, with the same quantization type.

2.4 State of Art

Figures of Merit allow comparing ADCs with different resolutions, power consumption, and sampling rates. The one used in this dissertation is the Walden Figure of Merit that yields the energy consumption by each conversion step, defined by

$$FOM_{walden} = \frac{P}{2^{ENOB} f_s}[J/conv.step], \tag{2.13}$$

where P is the total power consumption, ENOB is the effective number of bits and f_s is the sampling rate of the ADC.This Figure of Merit assumes, on the one hand, that the power consumption increase must be proportional to the sampling frequency (f_s), and on the other hand, each extra bit of ENOB must double the power consumption. These assumptions are not always accurate, and it does not take additional factors as the technology used. Table 2.1 resumes all Time Domain Quantization ADCs the architectures analyzed. The table identifies the ADCs' technology, once the decrease of the devices' size increases the velocity of logic gates and circuits that use time information. So, comparing the same architecture for different technologies allows seeing this evolution.

ADC Type		Supply[V]	Resolution	ENOB	f_s[GS/s]	FOM [fJ/s]	Power [mW]	Technology [nm]
Time Interleaved Frequency Based ADC	[17]	0.85	8	7.2	5	30.5	22.7	28
	[18]	1.8	10	9.13	0.005	845	2.36	180
	[5]	1	6	4.3	10	504	98	65
Single Frequency Based ADC	[4]	1.2	5	4.64	0.5	1010	12.6	130
	[19]	1.2	13	12.9	0.675	152	11.65	65
	[3]	-	12	11.3	0.150	4.3	0.46	28
Folding Flash TDC	[7]	1.3	6	4.3	10	504	98	65
Time Domain Interpolation Flash ADC	[9]	0.85	6	5.33	2.5	74.7	7.5	65
	[10]	1	6	5.39	3.4	89	12.6	65
	[11]	0.85	6	4.51	10	277	63	65
	[12]	1	5	4.06	5	94.6	7.8	65
	[13]	1.2	6	5.4	1	440	18.7	90
Digital Cells Folding Flash ADC	[14]	1.1	7	5.89	2.2	210	27.4	40
Two Step Time Interval Based ADC	[8]	1	7	6.34	4	36.2	11.7	28
	[16]	1	8	7.04	0.95	18.5	2.3	65
Two Step Frequency Based ADC	[15]	0.9	6	5.26	0.08	42	2.57	40

Table 2.1: State of Art.

Except for the Two-Step Time Interval Based ADC, for each ADC type, the lower FOM is achieved by an architecture implemented in the most recent technology, with the smaller transistor sizes. This fact shows that time-domain quantization ADCs benefit indeed with the decrease of the transistor sizes.

Between the frequency-based quantization ADCs, it is possible to see that the single ADC achieves a higher resolution, but the Time-Interleaved approach achieves a higher sampling frequency.

In the Time Interval Based Quantization ADCs, the resolution is between five and seven bits. The linearity of both folding approaches [7, 14] show more than one bit of difference between the resolution and the ENOB. It does not happen for any interpolation approach [9–14] (9-14), showing that the interpolation architectures have better linearity than the folding architectures. Except for [11], the interpolation flash ADCs have lower consumption than the folding architectures.

On the one hand, comparing the two step-time interval-based ADC with the single-step approaches [7, 9–14], the two-step can achieve higher resolution, lower consumption, and lower Figure of Merit. On the other hand, the two-step frequency-based ADC has a lower sampling frequency when compared with the single-step architectures [3–5, 17–19], except for [18]. The Time Domain Folding ADC is the one that has the worst FOM, but this implementation shows a linear folding and a DEM operation, which are features that can translate ADCs with good linearity.

Chapter 3

Time Interval Based ADC, with Folding TDC Implementation

The implementation chosen for this master dissertation is a 7 bit Time Interval Based ADC, with a TDC that implements a folding approach. The Time-Based ADC uses a VTC, an Asynchronous Counter, a Ring Oscillator, and a Decoder as seen in figure 3.1.

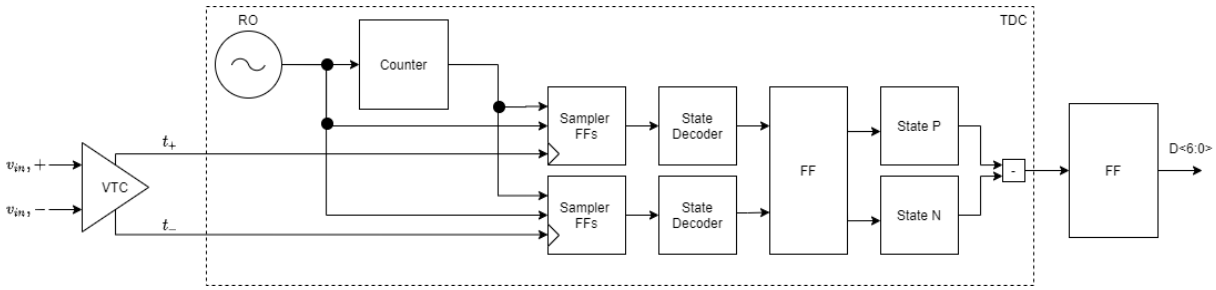


Figure 3.1: General Circuit of the ADC.

As seen in figure 3.1, the first block of the implemented ADC is a VTC. As the analog input signals are more frequently in the voltage domain, the VTC is an auxiliary circuit that translates the information in the voltage domain to the time domain by converting the input voltage amplitude to a time difference between the rising edges of two digital signals. The sample and hold circuit, responsible for sampling the input signal, is embedded in the VTC, as shown in the following section.

The next major block of the ADC represented in figure 3.1 is the TDC. The TDC quantifies the information coming from the VTC. It implements a folding approach, where Ring Oscillator signals make the fine quantization, and Counter signals make coarse quantization.

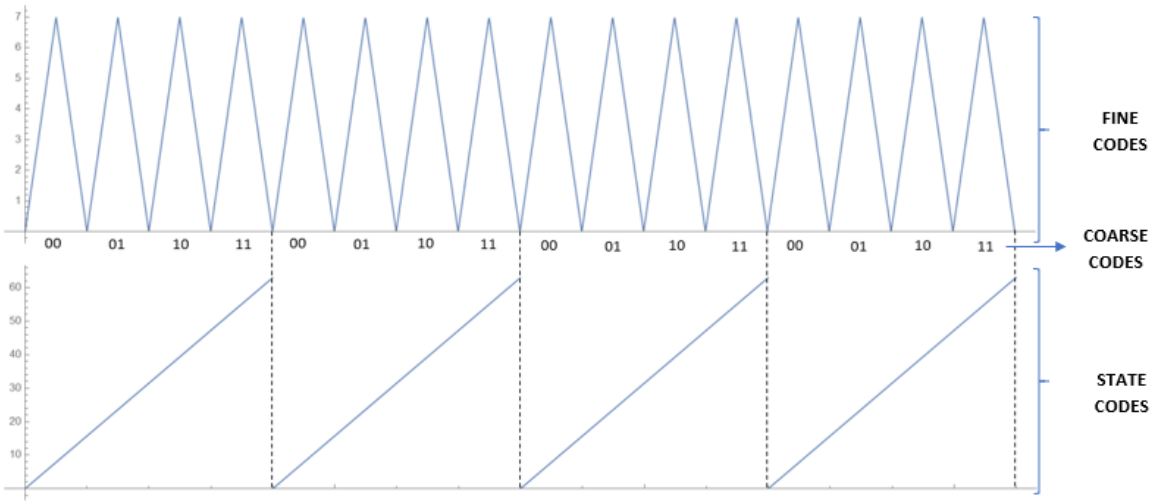


Figure 3.2: Fine, Coarse and State Codification.

The folding approach uses the periodic behavior of the RO output signals, as described in section 2.2.1. The implementation of this work uses an eighth-stage differential RO. So, the RO has sixteen outputs, $\Phi_i, i = 1, 2, ..., 8$ and $\overline{\Phi_i}, i = 1, 2, ..., 8$ and the corresponding RO's code is an eight-bit code defined by the concatenation of $\Phi_j, j = 1, 3, 5, 7$ and $\overline{\Phi_k}, k = 2, 4, 6, 8$. In figure 3.2, the vertical axis of the transfer function's fine codes is the total number of logic "1" at the RO's outputs. The output signal Φ_1 defines if the RO transfer function is increasing ($\Phi_1 = 0$) or decreasing ($\Phi_1 = 1$). The time instant that each digital signal at the output of the VTC occurs is the analog information to be quantized. As seen in figure 3.2, as this time instant occurs later, due to the periodic behavior of the RO's code, the transfer function between them and the time instant folds the analog amplitude in the time domain. Each fold is a RO period, and each fold has quantization steps, where a propagation time in a single delay cell in the RO defines each step variation. The fine quantization stores the RO code when the rise of the digital input signal occurred. However, this code can correspond to multiple folds. Then, the coarse quantizer identifies which fold corresponds to the input signal. After decoding the RO code in a 4-bit word and the coarse code in a 2-bit word, the state code aggregates the information, where the least significant bits of it are given by the RO code and the most significant bits by the coarse code.

As said before, the VTC converts the amplitude of the analog input signal in the time difference between the rising edge of the two output digital signal. If the input differential amplitude is positive, the positive output of the VTC, t_+, rises sooner than the negative output, t_-, and if the input differential amplitude is negative, t_- rises sooner. So, the TDC must quantize the time interval between them. Then, each digital signal at the output of the VTC defines a state code, and the difference between the states defines the TDC's quantization. The positive output of the VTC, t_+, defines the state EP by $EP[3:0] = Fine_P$ and $EP[5:4] = Coarse_P$, where $Fine_P$ is the corresponding fine code given by the RO code and $Coarse_P$ is the counter code. Similarly, the negative output of the VTC defines the state EN $EN[3:0] = Fine_N$ and $EN[5:4] = Coarse_N$. Each state has a quantization error, e_P and e_N with

maximum value equal to half of the quantization step's size, $|e| < \frac{1}{2}$LSB. Mathematically, the states are given by

$$\begin{cases} EP = T_D \times (16 \times Coarse_P + Fine_P) + e_P \\ EN = T_D \times (16 \times Coarse_N + Fine_N) + e_N. \end{cases} \tag{3.1}$$

The state difference is then given by $EN - EP = T_D \times [(Fine_N - Fine_P) + 16 \times (Coarse_N - Coarse_P)] + e_N - e_P$, where $|e_N - e_P| < 1$LSB. If the t_+ rises sooner than t_- when the input differential amplitude is positive, the state difference must be positive, and if t_- rises sooner, the state difference must be negative. Due to the double quantization error, the ADC's linearity is limited, as will be explained deeply in the section 4.2.2, once there is a 3 dB degradation of the SNR, and so the maximum linearity of the ADC is 6.5 ENOB.

This ADC implementation does not reset the RO nor the Counter at any time. Then, the state defined by each digital signal is always random. On the one hand, this allows having an inherent DEM operation, in which the LSB is not given by the propagation time of one single delay cell in the RO, but by the average between all of the propagation cells in the delay cells. The differences between those propagation times do not generate non-linearity but white noise. On the other hand, the codes generated from the folding approach are crescent and periodic. It means that the following code of the higher state value is the lower state value, as seen in figure 3.2. The example in figure 3.3 shows what can happen when there is a small-time difference between the output digital signals of the VTC.

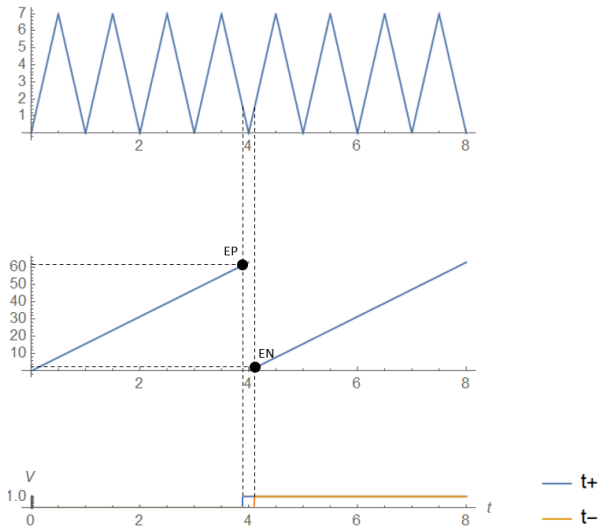


Figure 3.3: States generation example.

As the first state to occur is always random, the one defined by the t_+ can be a high-value state, close to the maximum value state. For the time interval of the example of the figure 3.3, EN, generated by the t_-, has a low value. The difference between the two, EN-EP, is negative, suggesting that the input differential amplitude is negative. As seen in figure 3.3, the negative state difference is wrong once the rise of the t_+ signal occurs sooner than the t_- signal. It is corrected by adding a bit to the counter,

redundancy bit, that defines if the states generated are from the same folding period. In this example, if the redundancy bit of the state N is '0', the redundancy bit of the state P is '1', or vice versa. This information will treat the result of the state difference as a positive value. This implementation allows the rising edges of the t_+ and t_- do not need to occur in a specific order.

The ADC implemented has a pipeline structure, where two clock periods are needed to compute the output code. In the first period, the VTC output digital signals are generated and used to sample the RO and Counter signals. In the second period, the RO and Counter signals are decodes and aggregated into the State values, and then the state difference is computed. Consequently, the ADC has latency.

3.1 ADC Linearity

The SNR evaluates the ADC's linearity. By definition, the signal to noise ratio in the time domain is given by

$$SNR = 20Log\left(\frac{t_{max}}{\sqrt{2}\sigma_{ADC}}\right) \tag{3.2}$$

where t_{max} is the maximum time interval between the digital signals at the output of the VTC that the TDC can quantify, defined by

$$t_{max} = \frac{2^N \times t_{LSB}}{2} \tag{3.3}$$

where N is the ADC resolution and t_{LSB} is the size of the Least Significant bit in the time domain and σ^2_{ADC} is the total jitter of the ADC.

To SNR be the relation between the RMS value of the maximum time interval and the RMS time noise, t_{max} is divided by $\sqrt{(2)}$ once it is considered a sinusoidal input.

The total jitter of the ADC, given by

$$\sigma^2_{ADC} = \sigma^2_{VTC} + \sigma^2_{TDC}, \tag{3.4}$$

where σ^2_{VTC} is the output jitter of the VTC and σ^2_{TDC} is the input-referred TDC jitter. The total jitter is the addition of those two terms, once the two terms are assumed to be independents.

Chapter 4

Block Implementation and Simulation Results

4.1 TDC

The TDC quantifies the time interval between the two digital signals at the output of the VTC by a folding approach. As seen in figure 3.1, the TDC is composed of a RO, an asynchronous Counter, and FFs.

4.1.1 RO Implementation

As seen before, the RO is responsible for a 4bit periodic code. To do so, it needs eight delay differential stages, using the negative and the output of the delay stage, consecutively, as seen in figure 4.1.

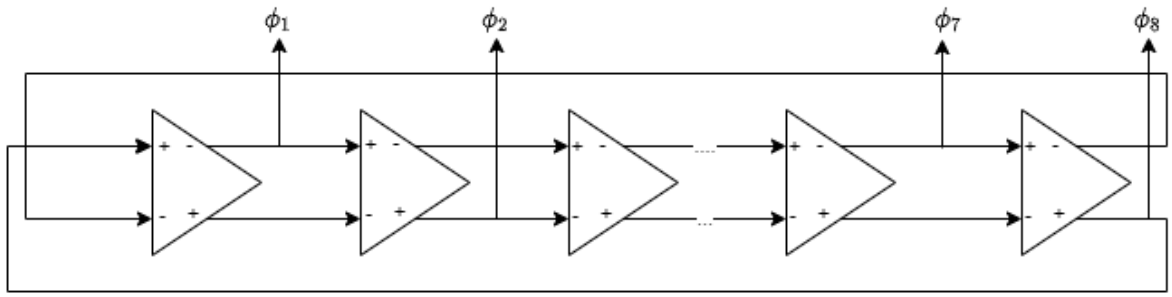


Figure 4.1: Differential RO.

The RO implemented has a main oscillator and a sub-oscillator, as seen in figure 4.2, [20].

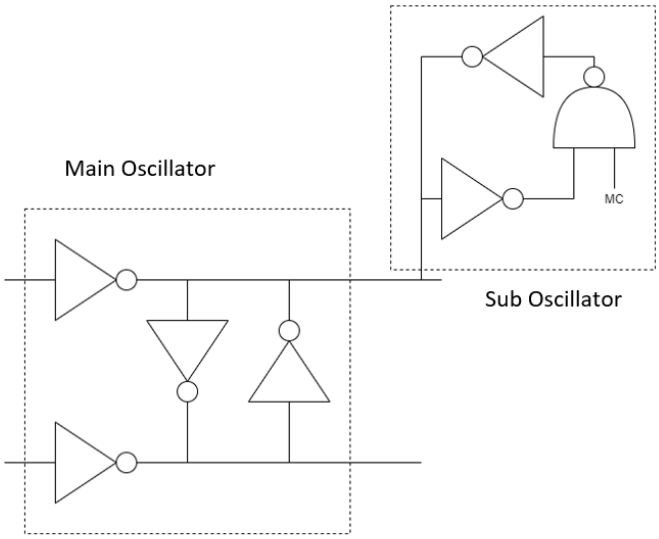


Figure 4.2: Main and Sub Oscillator.

The main oscillator is a conventional differential inverter, while the sub-oscillator has two inverters and a NAND gate. The MC signal controls if the sub-oscillator is active, $MC = 1$, or not, $MC = 0$. This control signal has the starting value of LOW then rises to HIGH to help the oscillator to begin to oscillate.

The transistors' sizes composing the main and sub-oscillator inverters assure that the RO oscillate at mode N+1. The oscillation mode translates the relation between the order of the waveform sequence and the delay stages' physical order. For example, in a RO with eight simple delay stages, there are eight nodes, $n_1 - n_8$, and eight corresponding waveforms, $W_1 - W_8$. Defining the oscillation mode 3, and assuming that the first signal is W_1, the waveform of n_1, the next waveform to appear is W_4, the waveform of n_4, followed by W_7, the waveform of n_7. On a differential RO composed by N delay stages, there are $2 \times N$ waveforms, where W_i is the positive output waveform of the node n_i and W_{i+N} is the negative output waveform of the same node. Therefore, the oscillation mode in an N delay stages' RO must be N+1, to use a positive and negative output of consecutive nodes, consecutively.[20] shows that to have an N+1 oscillation mode, the inverters of the main oscillator and the sub-oscillator can not have the same dimensions. At least, the sub oscillator's inverters must have twice the size of the main oscillator's ones. In [20] it is also shown that by increasing the sub oscillator's inverters, the oscillation frequency increases. As the counter must accept signals with at least the same frequency as the RO oscillation frequency, the inverters' sizes have the $2\times$ relation so that the RO frequency is not too high for the counter.

To reduce the charge effect of the rest of the ADC in the propagation time of the delay stages, the output phases of the RO go through buffers, figure 4.3.

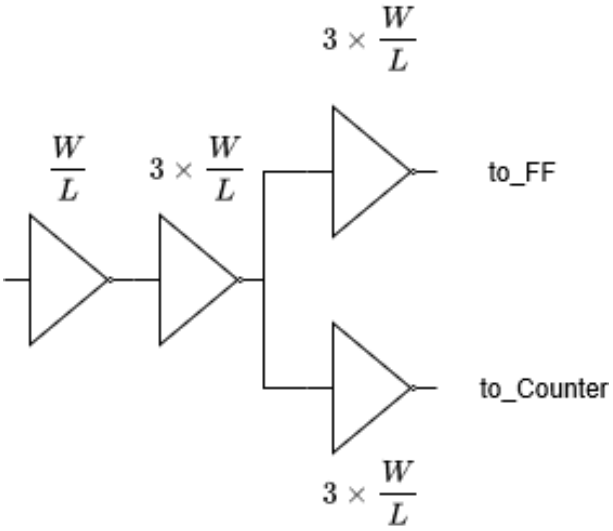


Figure 4.3: RO Output Buffers.

As the RO's output signal Φ_8 goes to the input of the counter and the input of a FF, while all the others only go to the FFs, the buffers are composed of four inverters, generating two different paths. Each path is composed of three inverters. One leads to the sampling FFs and the other leads to the input of the counter. The implementation assures the same charge in all stages sampled by the FFs, allowing that the propagation time of each become similar as possible. As seen in figure 4.3, each inverter's size is $3\times$ bigger than the previous one. There is an optimum size between consecutive inverters that minimizes the charge effect between them and the added delay. This optimum size is the neper number, $e \approx 2.71828$. The $3\times$ relation is a thumb rule used among analog designers.

There is a trade-off due to the inverters' size (RO inverters plus buffer inverters), between the mismatch and power consumption. In [7] is shown that as the inverters' size increases, the mismatch between the propagation times of each delay cell decreases with an exponential relation, but the power consumption increases linearly. Then, to assure the linearity specification of DNL, the RO's inverters are large, and then the consumption of this block becomes a concern.

RO Specification

As the RO is responsible for the fine quantization, a step-change in the RO leads to a step-change in the output code. It means that the RO defines the LSB, where a propagation time of a RO's delay stage differentiates consecutive codes. The propagation times of the RO's stages are all different due to variations in the carriers' concentration on the ADC layout. Due to the inherent DEM operation, the LSB is the average of those propagation times. However, as the ADC limitation due to the DNL is ± 0.5 LSB, the maximum variation between the average propagation time, $\overline{T_D}$, and each propagation time is $|T_{Di} - \overline{T_D}| = 0.5$LSB, which leads to a RO specification $T_{Di} = (1 \pm 0.5)$LSB.

The RO is responsible for two contributions to the linearity degradation: time noise due to the DEM

operation and periodic Jitter noise. The different propagation times of the RO stages translate time noise due to the DEM operation, where the mismatch between the delay stages converts to white noise. Smaller is the mismatch, so is the time noise. The other contribution is defined by

The time noise contribution of the RO is defined by, [7]:

$$\sigma_{RO}^2 = \frac{t_{in}}{T_{RO}} J_c^2 \tag{4.1}$$

where t_{in} is the time interval between the digital signals at the output of the VTC, T_{RO} is the RO period, and J_C^2 is the period jitter of the RO. These two-time noise contributions can not lead to a degradation of the TDC linearity bellow 37.88 dB of SNR, equivalent to 6ENOB.

4.1.2 RO Simulation Results

Start-up Precede

The figure 4.4 shows the startup precede where the signal v(r) is used as the RO supply voltage, performing as an enable signal, where it is OFF for the first 12.5ps and ON for the rest of the simulation. The RO takes some time to start oscillating and takes around 1ns to adjust the propagation times between cells. As the RO takes around 1ns to start oscillating with stable delay times between output phases, the ADC output signals will only be valid after this initial time interval.

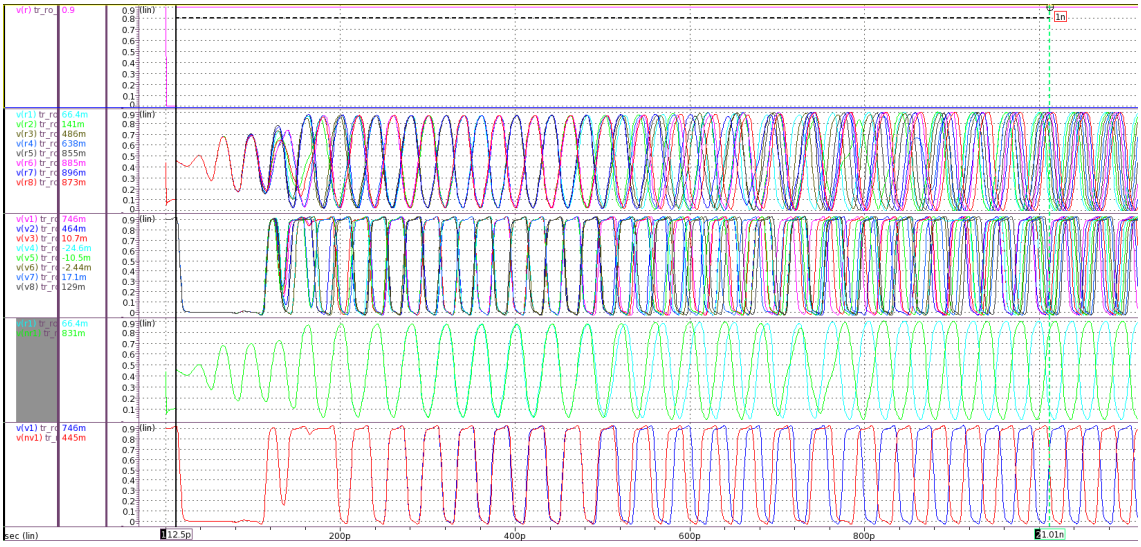


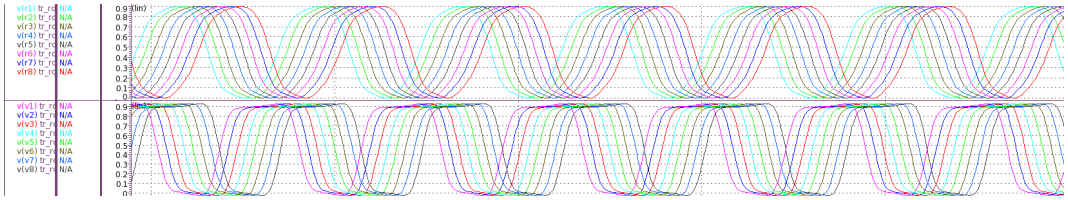
Figure 4.4: Startup Process.

In figure 4.4 the signals R* are the outputs of the RO, and the signals V* are the buffers' outputs. The signal r is an enable signal. In the figure 4.4 is possible to verify that the oscillation mode is 9 (N+1) after stabilization, as required, once the R* even signals ($R_i, i = 1, 3, 5, 7$) are the positive outputs of the nodes i and the R* odd signals ($R_j, j = 2, 4, 6, 8$) are the negative outputs of the nodes j. It is possible to see, in figure 4.4, that the sub oscillators start to oscillate later than the main oscillator, and only after the sub oscillators start to oscillate is that when the RO achieves the oscillation mode of $N + 1$. It is also

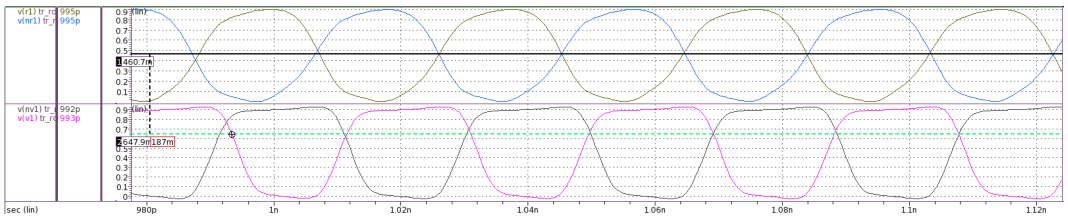
possible to see that the R1-R8 signals translate a thermometer type code, where the first code is every R* signals with logic level 0, the following code is every R* signals except the R1 signal that has logic level 1, in the following code, the R2 signal has logic level 1, and so on. When the R8 signal changes from HIGH to LOW, it marks the beginning of the folding codes. So, this signal is the output phase that is going to the input of the Counter.

Oscillation Stabilization

Figure 4.5(a) shows the RO's output and the buffers' outputs after stabilization.



(a) RO and Buffer Output Signals.



(b) Decision Levels.

Figure 4.5: Stable Oscillation Signals.

In figure 4.5(a) is shown the output signals of the RO (v(RX)) and the same signals after going through the buffers (v(vx)). In figure 4.5(b) is shown the output RO's signal Φ_1 v(r1) and the same signal at the output of the buffer. As seen in 4.5(b). the complementary signal of Φ_1 and Φ_1 himself cross at around 460mV ($\frac{V_{DD}}{2}$) and the same signals at the output of the buffer cross around 650mV. At those voltages, the signals of figure 4.5(a) have the same time delay between consecutive signals. It is the reason why the signals at the output of the RO seam symmetric to a horizontal axis at $\frac{V_{DD}}{2}$ and the outputs of the buffers do not look symmetric to that axis. This feature can lead to misdirection that sampling the signals at the buffers' outputs leads to additional quantization errors. However, it does not happen because the FFs that sample these signals compare the input with its complement, as will be demonstrated in section 4.2.

PVT Frequency Variation

Figure 4.6 shows the oscillation frequency for the different corners. The corners vary the supply voltage by $^{+}_{-}10\%$ (Vddmax and Vdd min), with nominal value of 0.9V, vary the temperature from $T = -40°$C (Tmin) to $T = 125°$C (Tmax), with nominal value of $T = 25°$C and vary the transistors, Process variations (Typ,SS,FF,SF,FS).

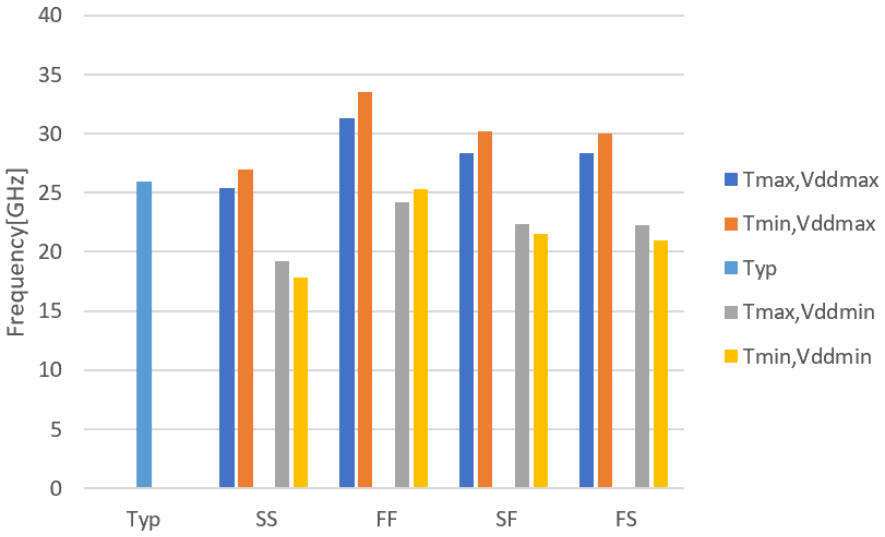


Figure 4.6: Frequency PVT Variation.

As seen in figure 4.6, the RO frequency is 25.91 GHz in typical conditions. As can be predicted, the higher frequencies happen for the FF (Fast Fast) process variation. The frequency is more supply voltage dependent than temperature-dependent. The oscillation frequency increases with the increase of the supply voltage. This result is justified once for higher supply voltage faster are the digital cells. The frequency variation goes from 17.86GHz to 33.56GHz, which leads to a TDC maximum interval from 119.2 ps to 224 ps. It shows that the time interval maximum between the two digital signals at the output of the VTC is 224 ps. As the sampling clock period is 400 ps, it can be divided into 100 ps to sample the input and 300 ps to produce those digital signals, and the sampler FFs have enough time to store the values from the oscillator and the counter.

RO Mismatch

The difference between propagation times of the delay cells is important to analyze to check the DNL specification and evaluate the noise that the RO produces that degrades the ADC's linearity. It is done Monte Carlo Simulations, with 1000 runs. The standard deviation of the propagation time of each delay stage results are in the figures 4.7 - 4.11.

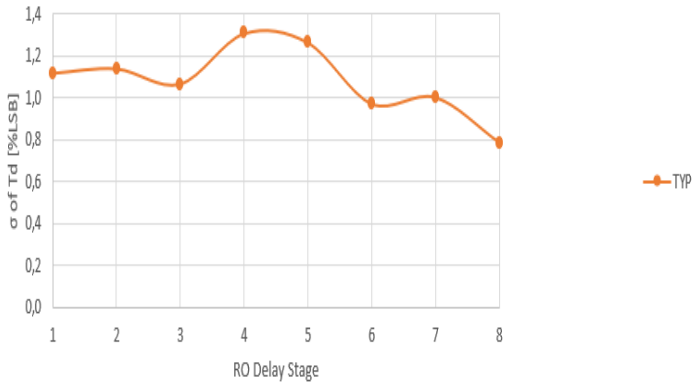


Figure 4.7: Typical Conditions.

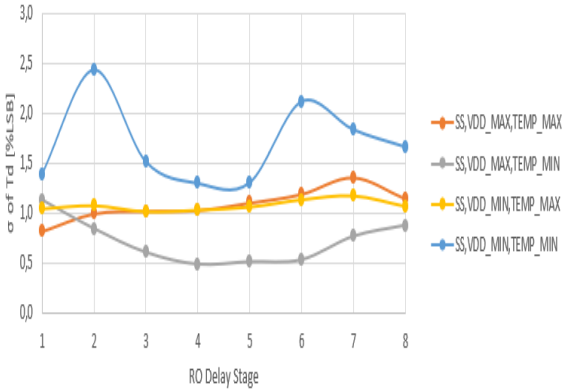


Figure 4.8: SS Process.

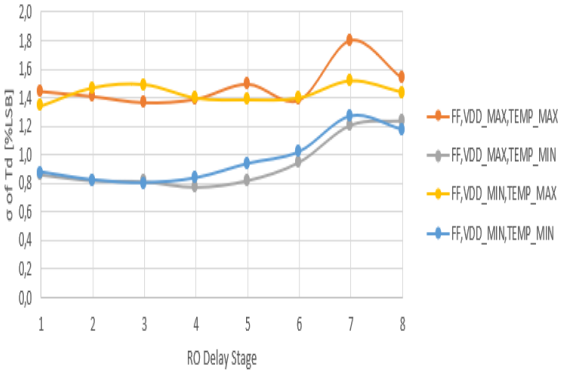


Figure 4.9: FF Process.

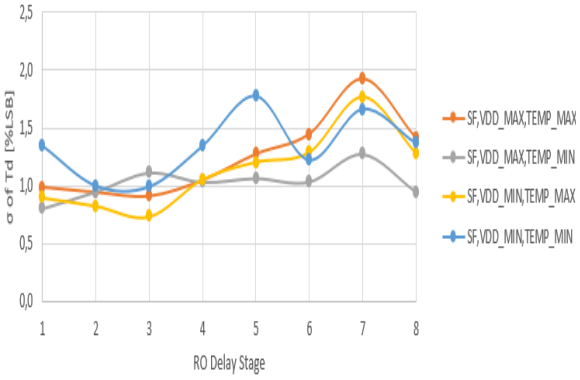


Figure 4.10: SF Process.

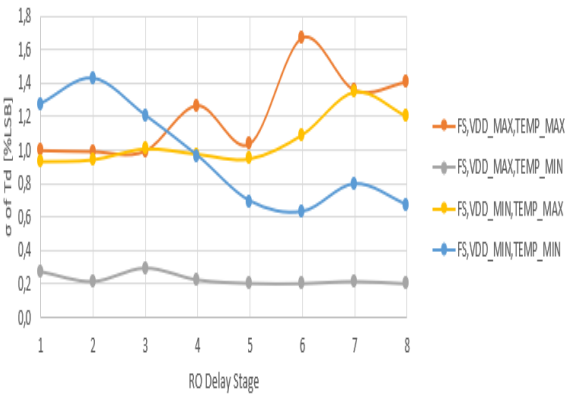
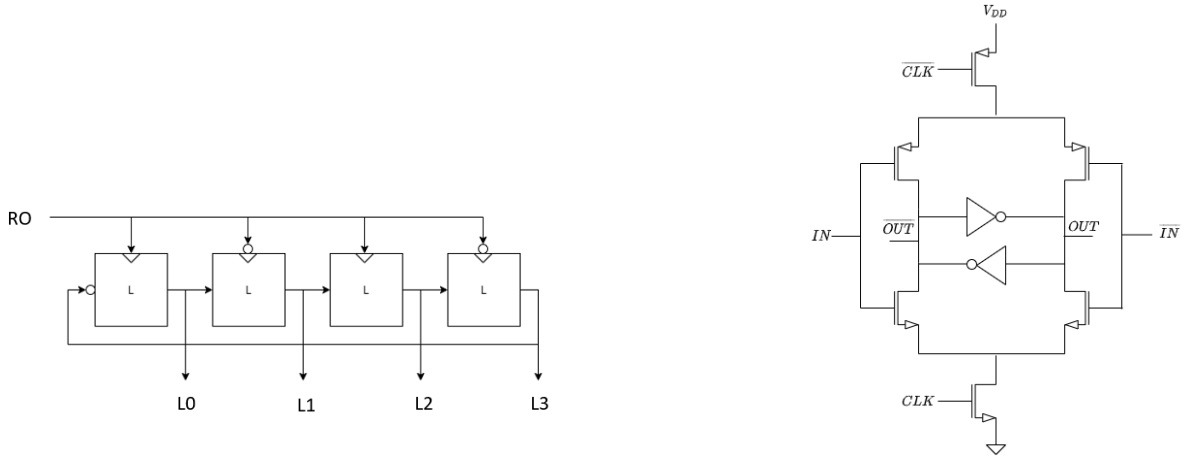


Figure 4.11: FS Process.

As seen in the results of the figures 4.7 - 4.11, the mismatch of the propagation times of the single delay cells of the RO is very low ($< 3\%LSB$), which shows that the implementation meets the RO specification for all the corners. It also shows that the inherent DEM operation does not create much white noise from this mismatch. This result is achieved due to the large size of the inverters of the RO output buffer. By simulation, if those inverters reduce their size, the counter will have a high charge effect on the RO and will not let it oscillate. In conclusion, there is almost no mismatch, but these buffers have high consumption.

4.1.3 Counter Implementation

The Counter identifies in which fold the time difference between the digital outputs of the VTC resides. To do so, it counts the number of periods of the RO, with a divide-by-four structure, [17]. Figure 4.12(a) shows the divide-by-four structure and the latch schematic circuit is in figure 4.12(b). To understand how the circuit works, figure 4.13 shows the signals.



(a) Divide-by-four structure.

(b) Latch Schematic Circuit.

Figure 4.12: Counter.

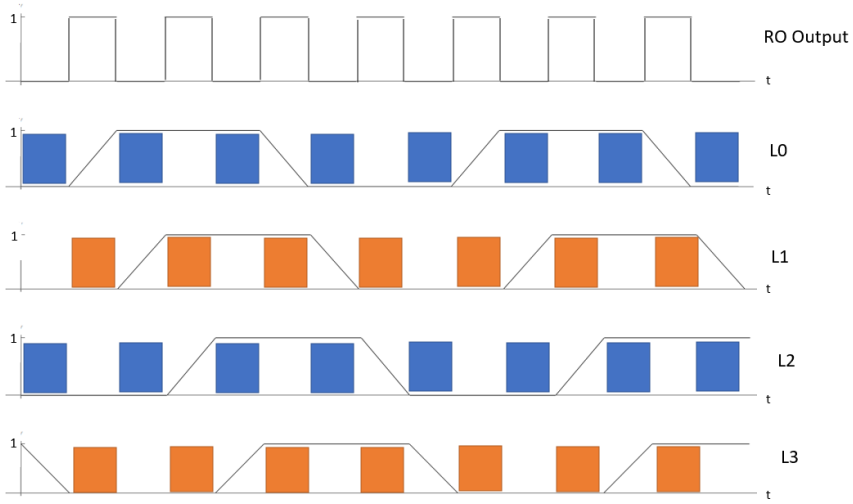
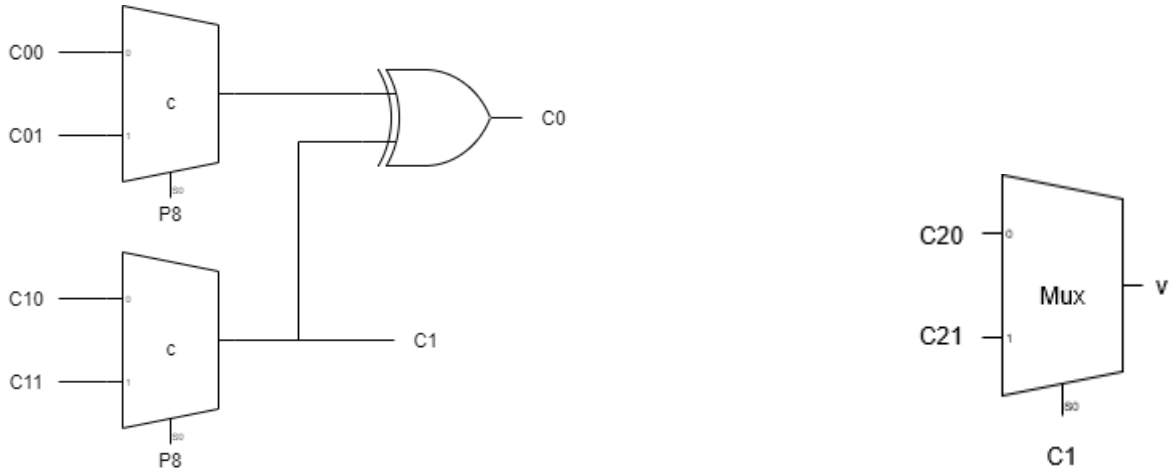


Figure 4.13: Counter Signals.

As seen in figure 4.13, the divide-by-four structure outputs four signals, L0-L3. Each has the same frequency, which is $1/4$ of the RO signal frequency, and they are a half period of the RO signal shifted between each other. At each half period of the RO signal, there is a variation in one of the counter output signals. Those variations are consecutive and periodic: first changes L0, then L1, then L2, then L3, then L0, and so on. Assuming that each variation takes a whole half RO period, each signal is stable for three half periods. If the even signals (L0 and L2) are sensitive to the half periods where the RO signal is HIGH, and the odd signals (L1 and L3) are to the half periods where the RO signal is LOW, the even are stable when the RO signal is HIGH, and the even ones are stable when the RO signal is LOW. The signals L0-L3 and Φ_8 RO's signal are sampled and decoded to compute the 2-bit word of the coarse code. In figure 4.14 is shown the counter's signals decoder.



(a) Two Least Significant Bits.

(b) Most Significant Bit.

Figure 4.14: Counter Decoder.

In figure 4.14(a), C00-C11 are the sampled signals of L0-L3, and P8 is the sampled RO's signal Φ_8. As L1 and L3 are stable when $\Phi_8 = 0$ and L0 and L2 are stable when $\Phi_8 = 1$, to compute the coarse

code, P8 is the selection bit of two multiplexers, L0 and L2 are the LOW inputs, and L1 and L3 are the HIGH inputs. L1 and L3 are guaranteed to be stable when P8=1, and so the multiplexers choose stabilized signals. L0 and L2 are guaranteed to be stable when P8=0 and the multiplexers also choose stabilized signals. Both multiplexers' inputs are guaranteed to be stable when P8 is metastable, and so the multiplexers can choose either one.

The redundancy bit's generation uses the same approach to, figure 4.14(b). There is a divide-by-two block in which the signal that controls the velocity is the L3 signal of the previous block, and then the selection bit is the selected signal between L2 and L3, which is the output signal C1 of the divide-by-four block.

As seen in figure 4.3, the outputs of each RO's stage go through buffers. Each buffer creates two paths. All of the RO's output signals only need to use one to go to the FFs' input, except for Φ_8. This phase uses both. One connects it with the FF(v8) and the other with the counter (v81). The v8 signal computes the counter's output signal, which is controlled by v81. So, V8 and V81 can not differ too much because it leads to a mismatch between the decoded counter signal and the actual counting value. An error on this codification leads to an output error of 2^4 or 2^5. So, let us check figure 4.15.

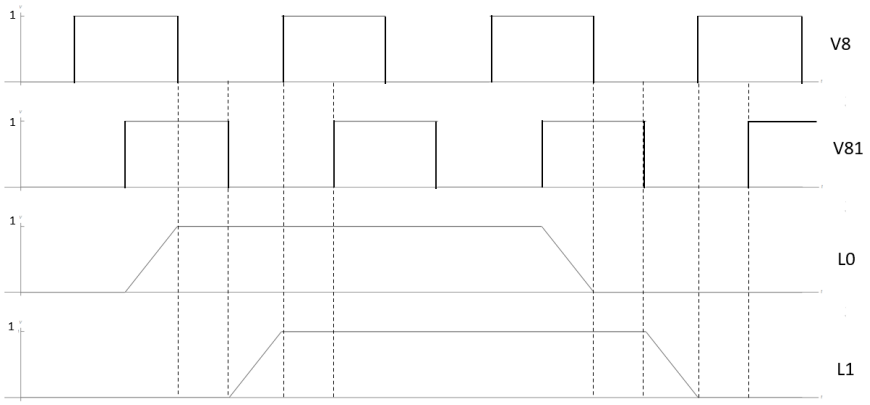


Figure 4.15: Time Difference Between the Φ_8 Signals that goes to the Counter, v81, and that goes to the FF, v8.

In figure 4.15, the signal v8 is the RO's phase 8 that is the FF's input, and the signal v81 is the counter's input signal. This figure analyzes the maximum time that the two can be apart and does not lead to quantization errors. As the selection bit, v8, does the codification of the counter's signal, selecting L0 and L2 when it is LOW and selecting L1 and L3 when it is HIGH, the implementation of this counter works if L0 and L2 are stable when V8 is LOW, and L1 and L3 are stable when v8 is HIGH. Figure 4.15 shows that the decisions are correct if the variations of L0 and L1 are fast enough so that those signals are stable before the edges of the v8. Then, if the L signals take t_{Lc} to change between stable values and if the RO period is T_{R0}, the two signals can differ by

$$\Delta t = T_{RO}/2 - t_{Lc}. \tag{4.2}$$

In the figure 4.15, the L signals take a quarter of the RO period to change, so the two signals can be

displaced in time by $\Delta t = T_{RO}/2 - T_{RO}/4 = T_{RO}/4$.

Counter Specification

This ADC uses an asynchronous Counter composed of two different blocks. The first one has to operate at the RO frequency. At every half period of the RO's signal, there is a variation in one of the four output signals, leading to the frequency of each be $1/4$ of the RO's frequency. The second block must operate at the frequency of the previous block frequency. The variations of the two output signals of the second block occur at every half period of the first block signals, which leads to the frequency of each be $1/8$ of the RO's frequency. Therefore, the counter's specification is related to the maximum input frequency, which must be higher than the RO frequency.

As the counter also works as an oscillator, the time noise contribution of the counter is given by

$$\sigma^2_{Counter} = \frac{t_{in}}{T_{Counter}} J_c^2 \tag{4.3}$$

where the $T_{Counter}$ is the period of the Counter. The Counter degrades the SNR through the time interval that a period of the Counter varies from its nominal value, and so it also can not lead to an SNR degradation bellow 37.88 dB.

4.1.4 Counter Simulation Results

Maximum Input Frequency

To assure that the counter works well with the output of the RO in its input first is evaluated the PVT variations maximum input frequency, figure 4.16.

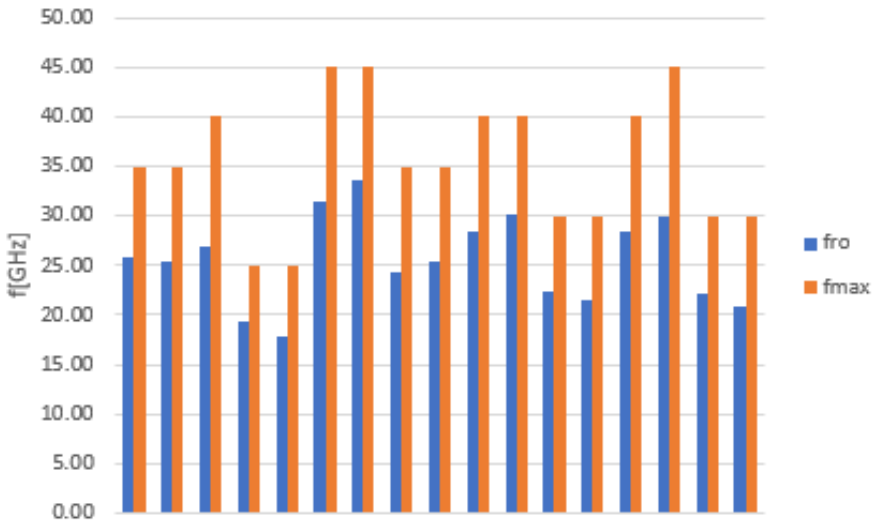


Figure 4.16: Maximum Input Frequency Vs RO Frequency.

As seen in figure 4.16, the counting of the RO's periods operation is assured once the RO frequency is always lower than the maximum frequency allowed in the counter's input. Furthermore, the results

showed in figure 4.16 suggest that the RO's frequency could be higher by increasing the sub-oscillator inverters' sizes. However, simulation results showed that increasing those sizes would, for some corners' variations, make the oscillator start to oscillate in a different mode than N+1 and, for other variations, the RO's frequency would become higher than the maximum frequency allowed in the counter's input. For those reasons, the inverters' size can not increase.

Counter Operation

Figure 4.17 shows counter's signals, COO-C11, and the two signals corresponding to phase 8 that goes to the counter and that goes to the DFF, v81, and v8 respectively of the RO.

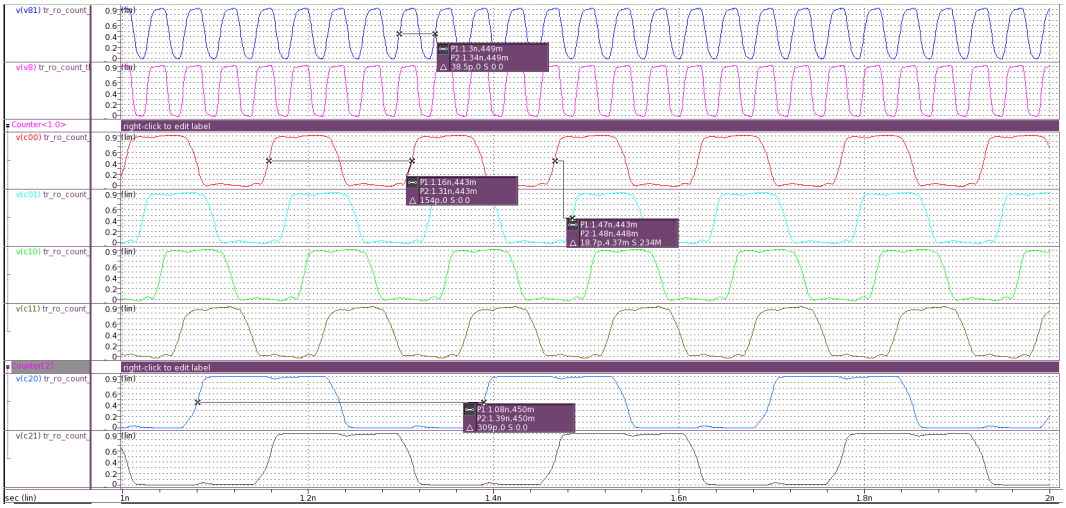


Figure 4.17: Counter Signals.

As can be seen in the figure 4.17, the period of the counter signals, C00-C11, is $T_C = 154ps$ and the period of the RO signal is $T_{R0} = 38.5ps$ which leads to $T_C = 4 \times T_{RO}$ confirming the good operation of the divide-by-four block. By its time, the period of the most significant signals of the counter signals, C20 and C21, is $T_{C2} = 308ps$, which leads to $T_{C2} = 2 \times T_C = 8 \times T_{RO}$, also confirming a good operation of the divide-by-two block.

In figure 4.17 is seen that, although the signals v8 and v81 are different, v8 is stabilized at HIGH when C01 and C11, corresponding to L1 and L3 in 4.13, are stable, and it is stable at LOW when C00 and C10, corresponding to L0 and L2 in 4.13, are stable.

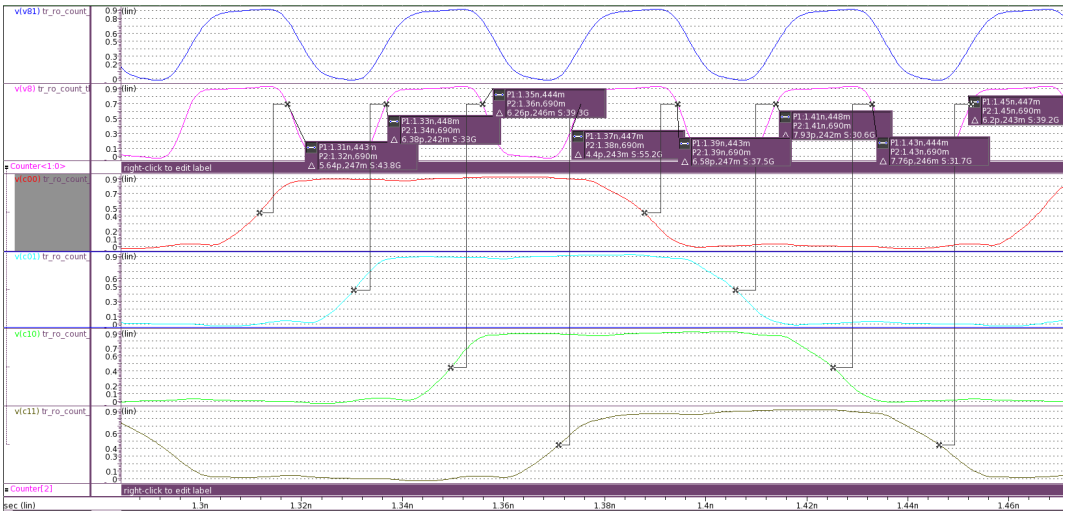


Figure 4.18: Demonstration of the Good Relation Between Signals.

As said before, on the one hand, the buffers' output signals (V*) cross with their complement at around 650mV and so assumes that it is stable at HIGH if $V* > 650mV$ and it is stable at LOW if $V* < 650mV$. On the other hand, the counter's output signals (C*) cross with their complement at around 450mV, and so they are stable at HIGH if $C* > 450mV$ and stable at LOW if $V* < 450mV$. Then, to the V8 decisions as selection bit of the multiplexers do not select not stabilized signals, the C* signals' transitions by 450mV must occur sooner than the V8 by 650mV. The results in figure 4.18 confirm this operation by showing the time instants that the transitions of V8 by 650mV and the transitions of C* by 450 mV to calculate the maximum time interval between V8 and V81 allowed.

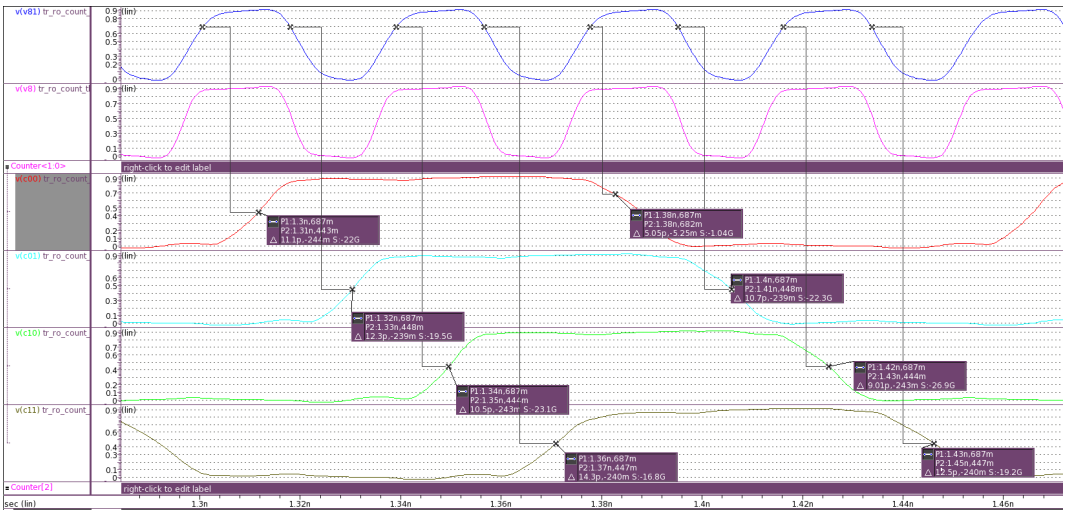


Figure 4.19: Propagation time of C* Signals.

As seen in the figure 4.19, the maximum propagation time of the C* signals is $t_{LC} \approx 14.3ps$. So, the maximum time interval between V8 and V81 is $\Delta t \approx 4.95ps$. The figure 4.20 shows that this time interval is $\Delta t \approx 2.33ps$, which is less than the maximum allowed.

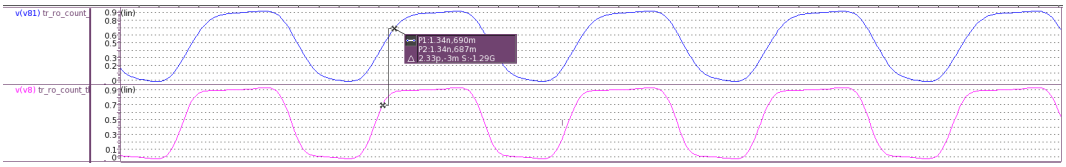


Figure 4.20: Time Interval between V8 and V81.

4.2 Sampler FF

A regular DFF based on logic gates can not be used to sample the RO's and the Counter's signals because it can not be assured a setup time. Then, to sample those signals is used a sense-amplifier-based FF consisting of a strong-arm comparator and an SR latch, as seen if the figure 4.21, [21].

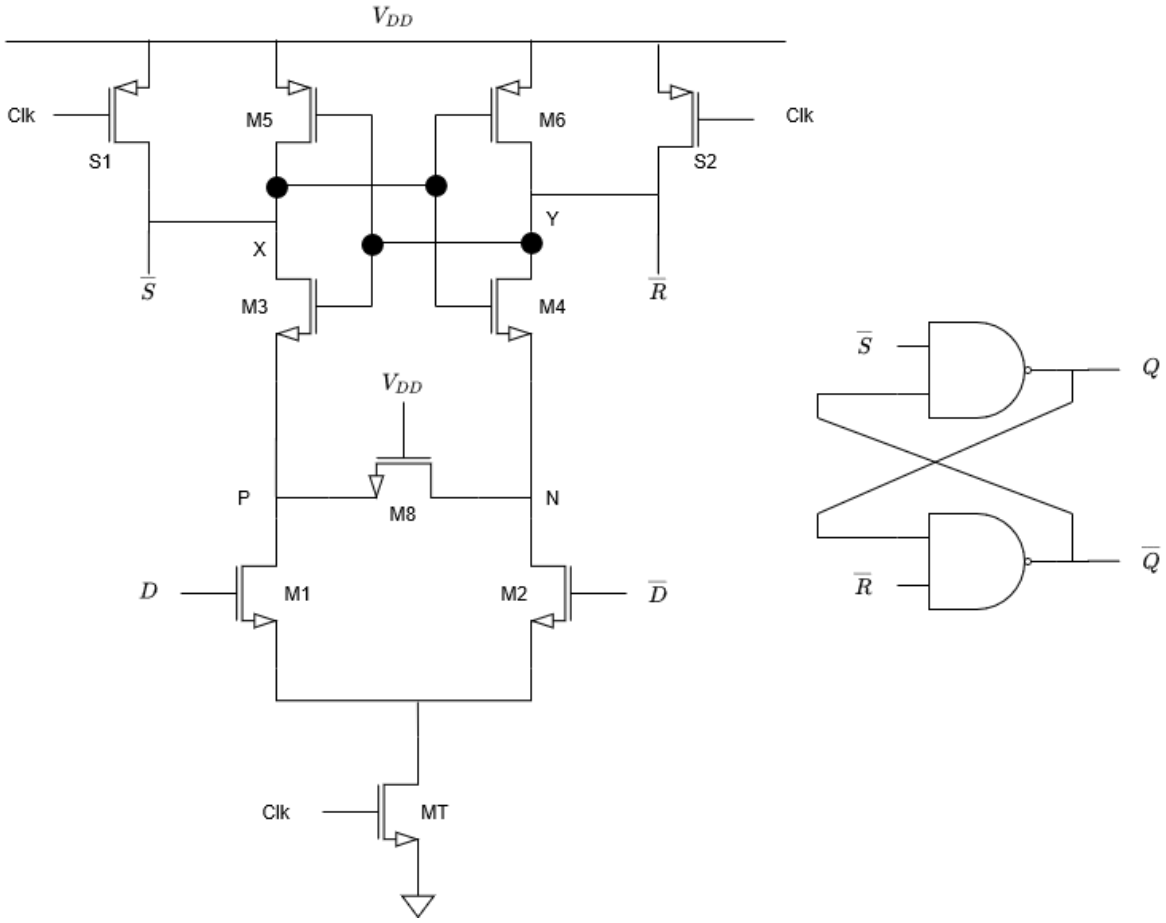


Figure 4.21: Strong Arm Latch Based FF.

The FF shown in the figure 4.21 samples the value of D at the rising edge of the CLK signal, which is going to be one of the digital outputs of the VTC, by comparing the D signal with its complement, $\overline{D}$. If $D > \overline{D}$ the output, Q, stores the logic level HIGH. As this FF needs the input and its complement, there is an advantage in implementing a differential RO because it outputs the signals and their complement

without adding logic, which would translate to a higher consumption but can lead to quantization errors that degrade the ADC's linearity. The counter implemented also allows to access the output signals and their complement.

The process of this sense-amplifier-based FF has four phases, figure 4.22.

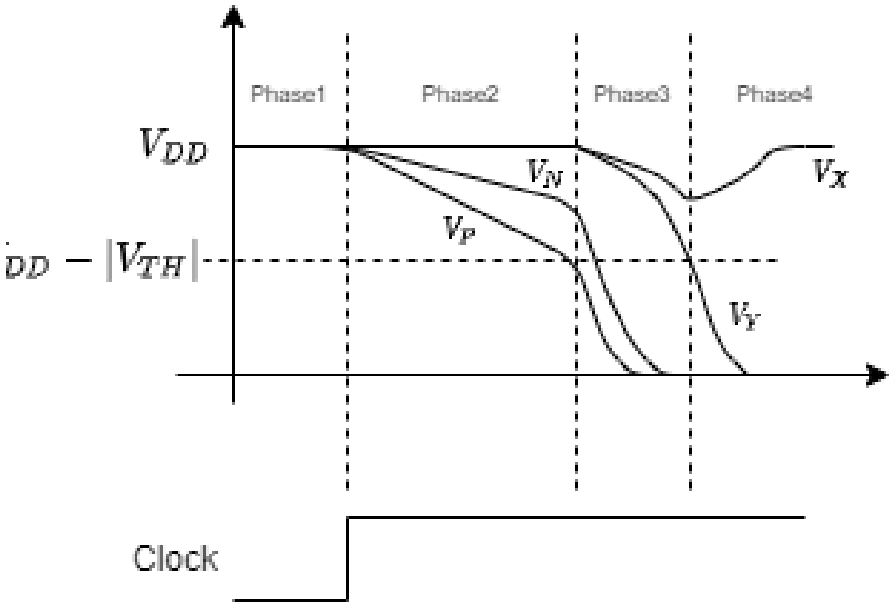


Figure 4.22: FF main signals.

As seen in figure 4.22, the FF process begins with the clock signal LOW. In the first phase, M1 and M2 transistors are OFF, and the voltages at the nodes X and Y are charged to V_{DD}, as the voltages at the nodes P and N. The rising edge of the clock signal begins the second phase, where the switches S1 and S2 turn OFF. In this phase, the transistors M1 and M2 turn ON and produce a current proportional to the input $D - \overline{D}$. As the M3-M6 transistor is initially OFF, the current flows through the parasitic capacitors of M1 and M2, C_P and C_N, respectively, allowing that $|V_P - V_N|$ grows and exceeds $|D - \overline{D}|$. There is a voltage gain, and so this is called the amplification mode phase. As V_P and V_N fall to $V_{DD} - V_{TH}$, M3 and M4 transistors turn ON, allowing that part of the drain current of M1 and M2 flow from X and Y. V_X and V_Y keep falling until one of them reaches $V_{DD} - |V_{TH}|$ turning ON M5 and M6. At this moment, the last phase begins where the positive feedback set V_X or V_Y to V_{DD} and the other to the ground.

In figure 4.21, the M3 and M4 transistors cut off the DC path between V_{DD} and ground in the last phase, avoiding static power drain, translating an advantage of this implementation. The M5 and M6 transistors restore the output's HIGH level to V_{DD}. Without them, the common-mode discharge in X and Y would lead to a degraded high level if the differential input $|D - \overline{D}|$ is small. The switches, S1 and S2, pre-charge the voltages at X and Y to V_{DD} assuring that the M5 and M6 remain OFF during the initial amplification and neglect the offset effect.

As the Strong Arm Latch generates invalid output during almost half of the clock cycle, a NAND based latch produces the output by detecting falls from V_X or V_Y. The NAND based latch has the truth table 4.1.

$\overline{S}$	$\overline{R}$	Output
1	1	No change
1	0	$Q = 1$
0	1	$Q = 0$
0	0	Invalid State

Table 4.1: Nand Based Latch Truth Table.

The input-referred noise of the sampler FF is computed as in [21]. The switches S1 and S2, in figure 4.21, allow reducing this noise with their pre-charge action. Most of the input-referred noise is generated by M1 and M2 and by the $\frac{kT}{C}$ noise deposited by S1 and S2 comes into play only after significant gain has accrued. The circuit acts as an integrator in the amplification mode, generating an output noise from M1 and M2. The amplification model lasts $t = \frac{C_{P,Q}}{I_{CM}} V_{TH,N}$, where $C_{P,Q} = C_P = C_Q$, C_P is the capacitance of the node P, C_Q is the capacitance of the node Q and I_{CM} is the common-mode current. Summing the noise from S1 and S2, dividing the result by the square root of the voltage gain, the input-referred noise is given by

$$\sigma_{FF}^2 = \frac{V_{GS} - V_{TH,N}}{V_{TH,N}} \left(\frac{4KT\gamma}{C_{P,Q}} + \frac{V_{GS} - V_{TH,N}}{V_{TH,N}} \times \frac{kT}{2C_{P,Q}} \right) \tag{4.4}$$

where $\frac{4KT\gamma}{C_{P,Q}}$ is the noise from M1 and M2.

4.2.1 Simulation Results

In figure 4.23, is shown the simulation result signals of the FF.

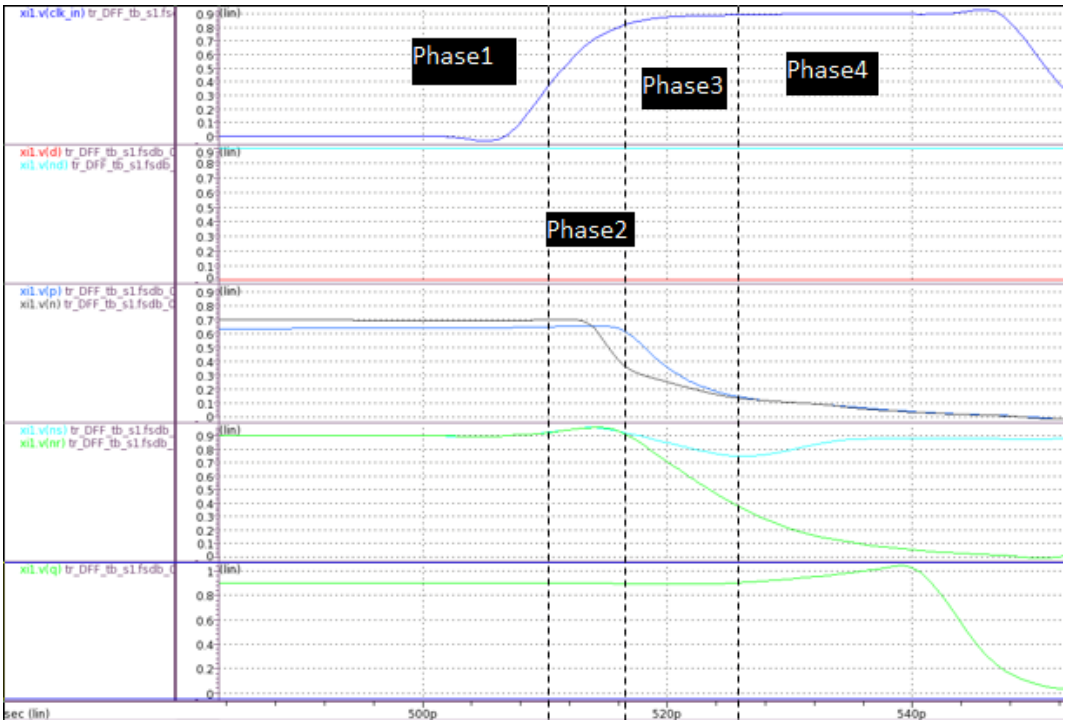


Figure 4.23: FF Signals Simulation.

Comparing the signals of figure 4.23 with the signals of figure 4.22, the signals V(x) and V(y) of figure 4.22 are the signals V(ns) and V(nr), respectively, of figure 4.23. As seen in figure 4.23, after the positive feedback set v(ns) to V_{DD} and set v(nr) to ground, it takes some time for the output, Q, to store the correct logic level. This time is the propagation time of the NAND-based Latch, and phase 4 only ends when the output is stable. It is important to evaluate the propagation time PVT variations, to assure that there is enough time to generate the signals at the output of the VTC and sample the signals from RO and the Counter. Monte Carlo Simulation is done, with 1000 runs, to evaluate the propagation time of the FFs, and the results are in figure 4.24.

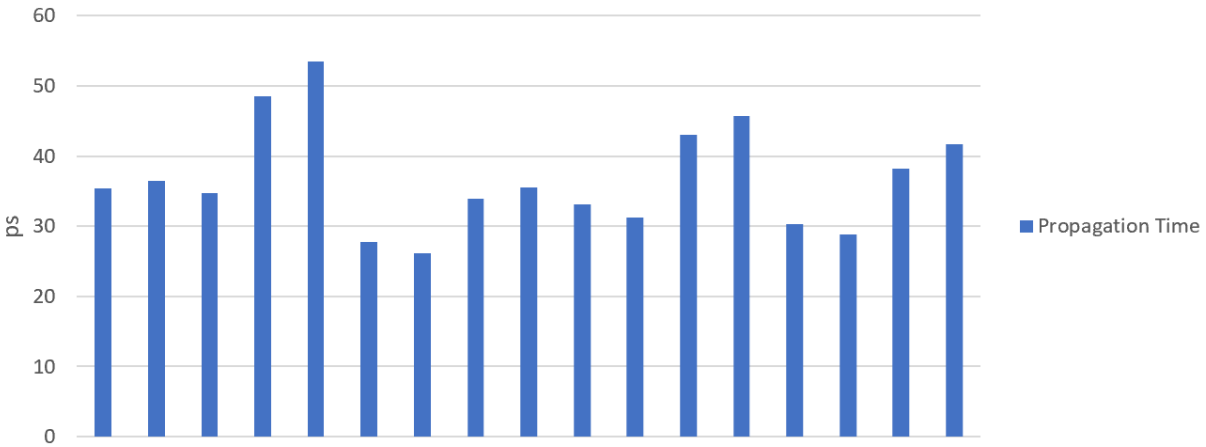


Figure 4.24: FF Propagation Time.

The results in figure 4.24 show that the FF's slower propagation time is 54ps. In the corner of the slower propagation time, the maximum time that the TDC can quantify is 224ps. Adding these two results leads to 278 ps, which is too close to 300 ps. It can lead to some problems because after 300ps from the beginning of the generation of the output VTC signals, the values stored in the FFs' will be sampled by other FFs to perform a pipeline approach. The new FFs' outputs decode the RO's and Counter's signals, the state values, and consequently the state difference. To solve this problem, the clock signal of the last FFs will not be the clock signal, but its complement, allowing to have additional 100 ps to the first FFs store the correct values and not lose information from the RO nor the counter.

4.2.2 TDC Linearity

The input-referred TDC jitter is given by

$$\sigma_{TDC}^2 = 2 \times (\sigma_q^2 + \sigma_{FF}^2) + \sigma_{RO}^2 + \sigma_{Counter}^2 + \sigma_{DEM}^2, \tag{4.5}$$

where σ_q is the RMS value of the quantization noise, σ_{FF} is the input-referred jitter of the DFF, σ_{RO}^2 is the RO jitter, $\sigma_{Counter}^2$ is the counter jitter, and σ_{DEM}^2 is the white noise converted from the mismatch, of the RO delay stages, due to the inherent DEM operation. Due to the quantization of the two states, the contribution of the quantization error, σ_q, and the input-referred RMS noise of the FF, σ_{FF}, are doubled, [22]. It leads to a limitation on the ADC linearity. If all blocks are ideal and do not presently jitter, the signal to noise ratio becomes

$$SNR = 20Log\left(\frac{t_{max}}{\sqrt{2}\sigma_q}\right) \tag{4.6}$$

where the quantization error, σ_q, is defined by

$$\sigma_q = \frac{t_{LSB}}{\sqrt{12}}. \tag{4.7}$$

The SNR becomes $SNR \approx 6.02(N-1)+4.77dB$, showing that there is a 3dB degradation due to the double sampling, corresponding to a 0.5-bit degradation in the ENOB. Then, the maximum linearity of this ADC is 6.5 ENOB. To check the linearity specification of the ADC, the linearity of the TDC, imposed by the quantization error and by the contributions of the RO jitter noise, the Counter jitter noise, the DEM white noise converted by the RO delay cells mismatch and by the input-referred noise of the FFs, should show an SNR above 37.88 dB, corresponding to 6ENOB.

4.2.3 TDC Simulation Results

The total noise of the TDC, (4.5), evaluates the TDC's linearity. To compute the RO jitter (σ_{RO}) and the counter jitter ($\sigma_{Counter}$), Monte Carlo Simulations are used to evaluate the RO period and the Counter period variation results. The RO jitter (σ_{RO}) is $3\times$ the standard deviation of the Monte Carlo Simulation results of the RO period, and the Counter jitter ($\sigma_{Counter}$) is $3\times$ the standard deviation of the Monte Carlo Simulation results of the Counter period. To evaluate the white noise converted from the mismatch, σ_D, it is performed Monte Carlo Simulations evaluating the propagation time of the RO delay cells, and is computed the average, which is the LSB size in the time domain (t_{LSB}), and the standard deviation is computed (σ). The white noise converted from the mismatch, σ_{DEM}, is $3 \times \sigma$. All these noise contributions are combined by

$$\sigma_{noise} = \sqrt{2 \times \sigma_{FF}^2 + \sigma_{RO}^2 + \sigma_{Counter}^2 + \sigma_{DEM}^2} \tag{4.8}$$

Process	Supply Voltage	Temperature	t_{LSB}[ps]	σ_q[ps]	$\sigma_{noise,TDC}$[ps]	SNR[dB]	ENOB
typ			2.41	0.696	0.387	40.3	6.40
ss	MAX	MAX	2.47	0.712	0.374	40.3	6.41
		MIN	2.32	0.670	0.284	40.5	6.44
	MIN	MAX	3.25	0.938	0.507	40.3	6.40
		MIN	3.50	1.010	0.902	39.4	6.26
ff	MAX	MAX	2.00	0.576	0.395	40.0	6.35
		MIN	1.86	0.537	0.264	40.4	6.42
	MIN	MAX	2.43	0.701	0.479	40.0	6.35
		MIN	2.47	0.712	0.371	40.3	6.41
sf	MAX	MAX	2.21	0.638	0.454	39.9	6.34
		MIN	2.99	0.862	0.289	40.7	6.46
	MIN	MAX	2.82	0.814	0.565	40.0	6.34
		MIN	2.91	0.839	0.571	40.0	6.35
fs	MAX	MAX	2.21	0.637	0.416	40.1	6.36
		MIN	2.08	0.601	0.082	40.9	6.49
	MIN	MAX	2.81	0.811	0.499	40.1	6.38
		MIN	2.99	0.862	0.467	40.3	6.40

Table 4.2: TDC Noise.

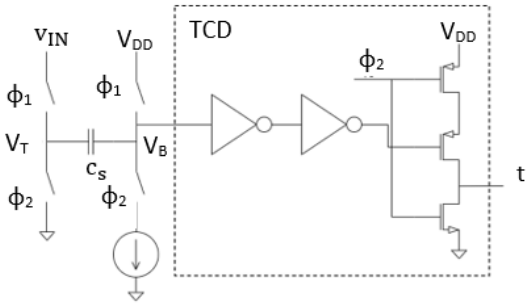
As seen in table 4.2, the TDC linearity is always higher than the 6 ENOB specification. It is also possible to see that the quantization noise degrades the most TDC's linearity. The simulation results show that the TDC's linearity is robust about process variation, variations on the supply voltage, and temperature variations.

The TDC's linearity is almost independent of the input signal, once the blocks that implement the folding approach of the TDC (RO and Counter) are not dependent on the input signal, once the RO oscillates at a free-running frequency, which is independent of the input signal, and the Counter works at the RO frequency. It shows that only the VTC's linearity dependence on the input frequency limits the full ADC's linearity dependence on the input frequency.

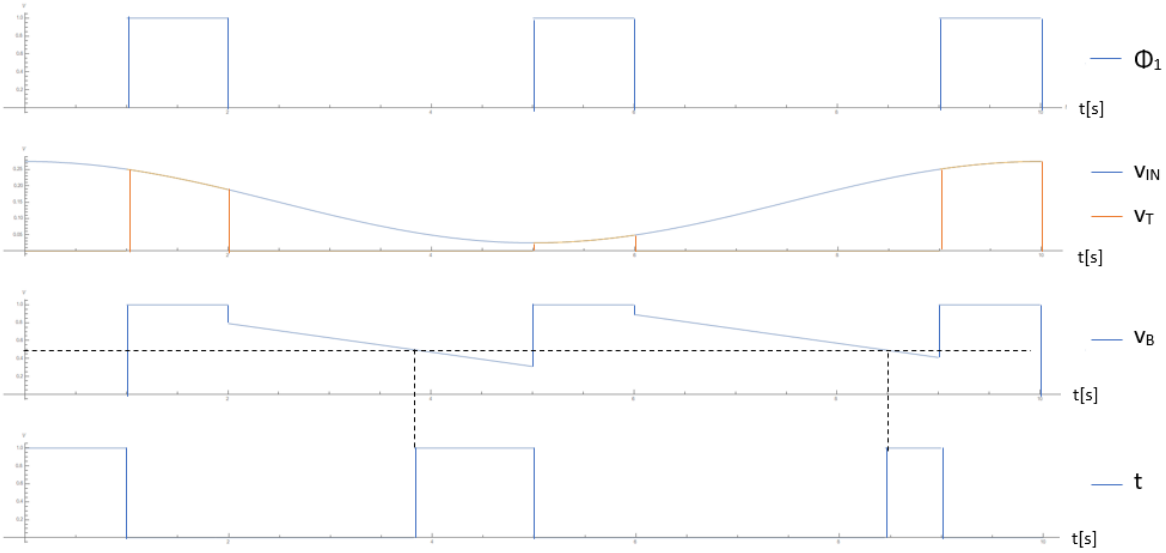
Finally, the TDC's results allow concluding that on the contrary of the folding approach on the voltage domain, which is nonlinear and to improve linearity it must use multiple architectures, increasing the folding architecture area and consumption, folding on the time domain is linear. It is an advantage because benefits with the decrease of the technology, once the digital cells, RO and Counter, become faster and so is possible to achieve smaller LSB size, which can lead to design higher resolution ADCs with the folding approach.

4.3 VTC

The input analog signals are more frequently in the voltage domain. Then, there must be an auxiliary circuit that converts the voltage domain's amplitude into a time variable, which is the time difference between the rising edge of two digital signals. The VTC used is represented in figure 4.25(a), [23, 24]. In figure 4.25(a), $\phi_2 = \overline{\phi_1}$. To understand how this VTC works, figure 4.25(b) shows the main signals.



(a) Schematic Circuit.



(b) Main Signals.

Figure 4.25: Implemented VTC.

The VTC implemented, shown in figure 4.25(a), is composed of four switches, a capacitor, a reference current source, and a Threshold Cross Detector (TCD). The TCD is composed of two simple inverters and a true phase inverter. As seen in figure 4.25(b), the process begin with the left terminal of the capacitor C_s follows the input signal, $V_T = v_{IN}$, while ϕ_1 is HIGH and the right terminal of the capacitor is charged to the supply voltage, $V_B = V_{DD}$. Then, as the left terminal of the capacitor discharges to the ground, the right terminal must discharge the same amount, once the differential potential between the two terminals of the capacitor can not change instantaneously, and so $V_B = V_{DD} - v_{IN}$. Then, the node V_B discharges by a constant current. When V_B crosses the threshold voltage of the first inverter, the output digital signal becomes HIGH.

As seen in figure 4.25(b), the time that takes the output signal, t, to rises is longer for a small amplitude signal of the input sample. Assuming an ideal capacitor, which current-voltage relation is $i_C = C\frac{dV}{dT}$, results:

$$\Delta t = \int \frac{C}{i_C} dV. \tag{4.9}$$

In (4.9) C is positive and constant and i_c is negative and constant. From (4.9) results:

$$\Delta t(t_k) = -\frac{C}{|i_C|}(v_f - v_i), \tag{4.10}$$

where v_f is the threshold voltage of the cross detector, v_{TH} and $v_i = V_B(t_k) = V_{DD} - v_{IN}(t_k)$. Then:

$$\Delta t(t_k) = \frac{C}{|i_C|}(V_{DD} - v_{TH}) - \frac{C}{|i_C|}v_{IN}(t_k), \tag{4.11}$$

which translates a linear relationship between the input signal and the rising time instant and shows that higher input amplitude, $v_{IN}(t_k)$, results in a higher time interval. However, the VTC generates two output digital signals that translate the differential input amplitude through the time difference between their rising edges. So, if the positive input is defined by $v_{in,+} = V_C + \frac{v_d}{2}cos(2\pi f_{in}t)$, where V_C is the common-mode voltage, v_d is the differential input amplitude and f_{in} is the input frequency, the negative input is defined by $v_{in,-} = V_C - \frac{v_d}{2}cos(2\pi f_{in}t)$, the time interval between the outputs of the VTC is defined by

$$\Delta t_{VTC}(t_k) = t_- - t + - = \frac{C}{|i_c|}v_d cos(2\pi f_{in}t_k). \tag{4.12}$$

The time interval between the outputs of the VTC is linear in respect to the input signal, and the gain of the VTC is $\frac{C}{|i_C|}[s/V]$, which translates the relation between the input voltage amplitude and the time interval between the rising edges of the two digital signals at the output of the VTC.

There are some difficulties when implementing a linear VTC. The first one is that the current must remain constant for $V_B > V_{TH}$. It happens if by ensuring that the transistor used as the current source remains in saturation, neglecting the channel length modulation. The channel length of this transistor is large to reduce this channel length modulation. In this case, it is used the maximum length possible, but it still is possible to see the channel length modulation effect. Other difficulty is that the threshold voltage of the cross detector, v_{TH}, must be lower than the minimum V_B voltage at the beginning of each discharge, i.e, $v_{TH} < V_{B,init,min} = V_{DD} - v_{IN,max}(t_k) = V_{DD} - V_C - \frac{v_d}{2}$. This threshold voltage is not constant for the process, temperature, and supply voltage variations, and then the input common voltage, V_C, must be chosen to guarantee the previous condition. The last difficulty is that the discharge current of the VTC must be high enough to generate the digital outputs of the VTC that take more time before the next clock period. As the gain is defined by $\frac{C}{|i_C|}$, increasing the current will decrease the gain. Then, to assure that the VTC always produces two digital signals at the output of the VTC, the maximum time interval between the two digital signals can be lower than the maximum time interval that the TDC can quantify, which results in a reduction in the output amplitude.

There are some advantages that this type of VTC has when compared with the CSI based VTC, shown in figure 2.7. The first one is that the VTC used does the sampling of the input voltage, while the CSI based VTC needs an auxiliary Sample and Hold circuit. The second one is that the time interval between the output signals of the VTC implemented has a linear relation to the input voltage. Although the time interval between the output signals of the VTC is also given by $\Delta t_{CSI} = t_- - t_+$, and the time interval that takes to each output signal to rise is also (4.10), the discharging current is the major difference between the two implementations. In the CSI based VTC, neglecting the channel length modulation, the discharging currents of each VCDU is given by $I_x = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS,x} - V_t)^2$, where $V_{GS,1} = v_{in,+}$ and $V_{GS,2} = v_{in,-}$ for the two VCDUs. Then, the time interval is given by

$$\Delta t_{CSI} = -C(V_{DD} - V_{TH})\left(\frac{1}{I_1} - \frac{1}{I_2}\right) = -C(V_{DD} - V_{TH})\frac{I_2 - I_1}{I_1 \times I_2}, \tag{4.13}$$

where V_{DD} is the supply voltage, V_{TH} is the threshold voltage of the detector, and C is the capacitor. The current difference is given by

$$I_2 - I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}2 \times (V_C - V_t)v_d cos(2\pi f_{in} t_k), \tag{4.14}$$

which translates a linear relation between the current difference and the input signal. However, the current multiplication is given by

$$I_1 \times I_2 = \left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right)^2\left[(V_c - V_t)^2 - \left(\frac{v_d}{2}cos(2\pi f_{in})\right)^2\right]^2, \tag{4.15}$$

which translates a nonlinear relation and so (4.13) does not translate a linear relationship between the input signal and the time interval between the output signals of the VTC.

The last advantage of the VTC used is that it has higher freedom to control the gain, to follow the PVT variations of the maximum time interval that the TDC can quantify, by controlling the discharging current PVT variations.

4.3.1 Current Reference

As seen in (4.12), the current defines the VTC's gain. The VTC's gain must align with the maximum time interval that the TDC can quantify. So, the current is the variable that assures it. The TDC's full scale is given by $4 \times T_{RO}$, where T_{RO} is the inverse of RO's frequency. The circuit used as current reference is represented in figure 4.26, [25].

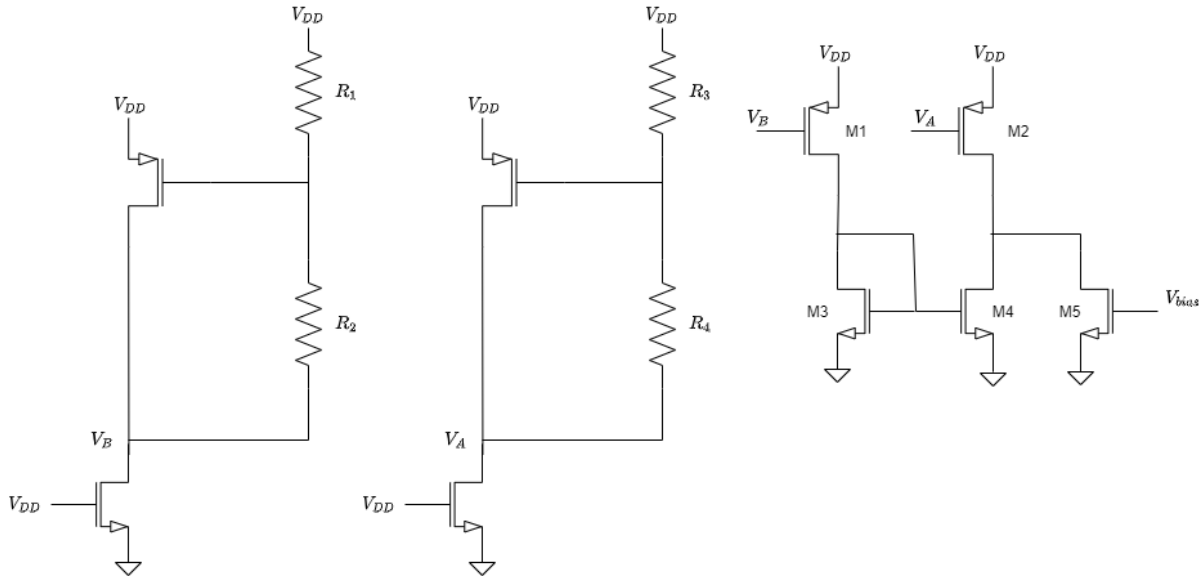


Figure 4.26: Current Reference Circuit.

The current that flows the transistor M5 is the bias current reference, which then is mirrored to the VTC. The current is the difference between the one that flows thought M1 and M2, I_{D1} and I_{D2} respectively. Neglecting the channel length modulation, these currents are defined by:

$$\begin{cases} I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{DD} - V_B - V_{TH})^2 \\ I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{DD} - V_A - V_{TH})^2. \end{cases} \tag{4.16}$$

To the currents be defined by (4.16), the channel length of the transistors M1 and M2 must be high enough to neglect channel length modulation. It is used $L_1 = L_2 = L = L_{max}$ The voltages V_A and V_B are defined by

$$\begin{cases} V_{DD} - V_B = \left(1 + \frac{R_2}{R_1}\right) V_{TH} \\ V_{DD} - V_A = \left(1 + \frac{R_4}{R_3}\right) V_{TH} \end{cases} \tag{4.17}$$

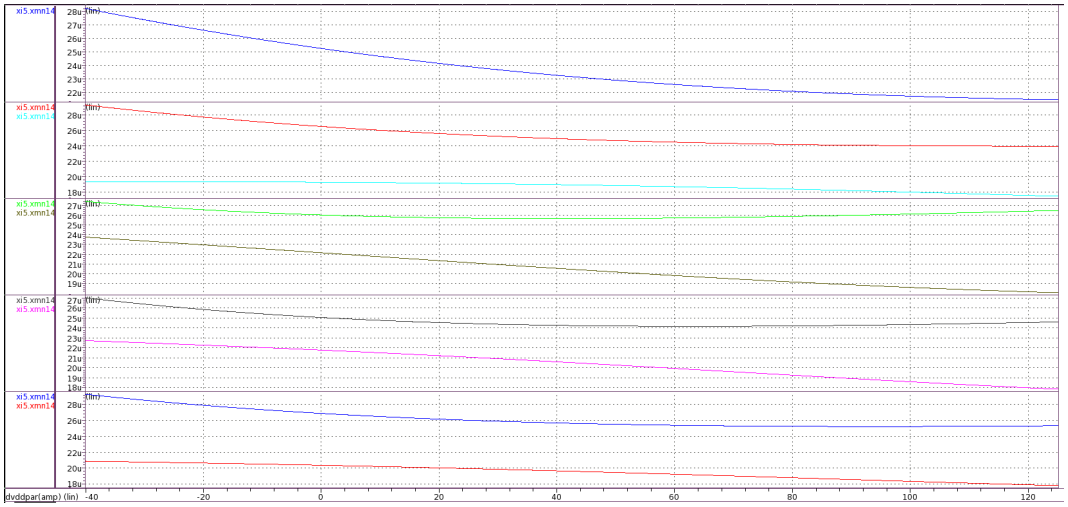
Assuming $R_1 = R_3 = R$, the output current is then defined by

$$i_{OUT} = \frac{1}{2}\mu_n C_{ox}\left(\frac{V_{TH}}{R}\right)^2\left(\frac{R_2^2 W_1 - R_4^2 W_2}{L}\right) \tag{4.18}$$

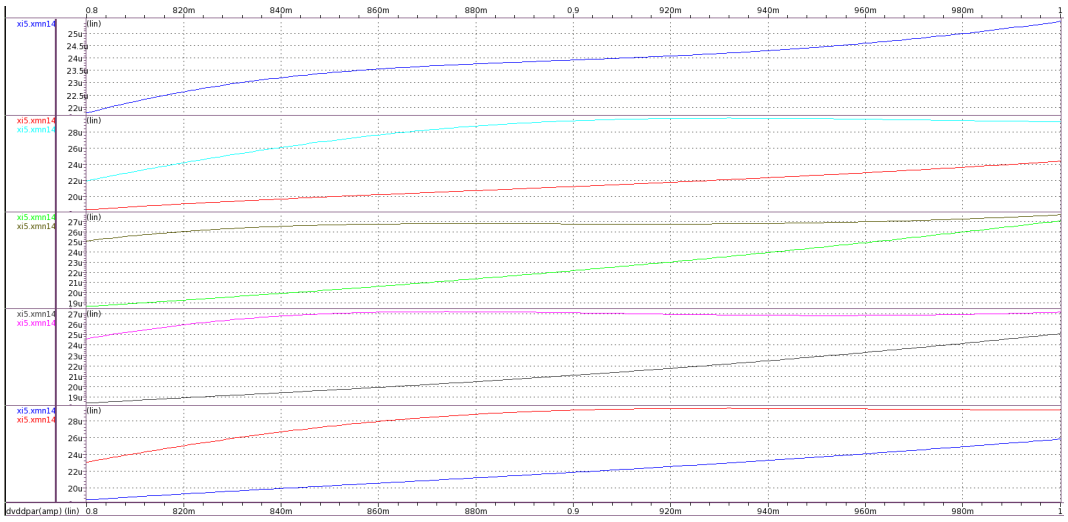
The output current (4.18) is dependent on the carrier's mobility (μ_n) and the threshold voltage (V_{TH}). The carrier mobility is roughly proportional to $T^{-1.5}$, where T is the absolute temperature, and the threshold voltage also decreases with the increase of the temperature. In this technology, the resistors do not change significantly with the temperature. So, it results in a temperature negative coefficient current.

Current Reference Results

The current reference is the principal responsible circuit to control the VTC gain. As said before, the generated current has a negative temperature coefficient. This result is in figure 4.27.



(a) Temperature Variation.



(b) Voltage Supply Variation.

Figure 4.27: Current Simulation.

The results in figure 4.27 show that the current reference has a negative temperature coefficient, once as the temperature increases, the current decreases, and a positive supply voltage coefficient, once as the supply voltage increases, increases. These results show that the current has the required behavior to match the PVT variations of the RO frequency, which control the TDC's full scale, with the VTC's gain.

4.3.2 VTC Linearity

The VTC voltage noise is given by, [7]:

$$V_{n,VTC}^2 = \frac{kT}{C_s}\left(1 + 2\gamma\frac{g_m}{I_C}\right) \tag{4.19}$$

where k is the Boltzmann constant, T is the absolute temperature, C_S is the VTC capacitor, γ is the thermal coefficient of the transistor that operates as current source, g_m is its transconductance and I_C is the discharging current. The VTC output jitter is defined by the noise voltage divided by the slew rate, SR_{VTC}, at the threshold-crossing point,

$$\sigma_{VTC}^2 = \frac{2V_{n,VTC}^2}{SR_{VTC}^2} = \frac{\frac{2kT}{C_S}\left(1 + 2\gamma\frac{g_m}{I_D}\right)}{\left(\frac{I_C}{C_S}\right)^2}. \tag{4.20}$$

The VTC output jitter described by (4.20) show that the sampling capacitor, C_S, must be as small as possible to reduce the jitter, the discharging current and the I_C must be as high as possible. As the VTC gain is $\frac{C}{|i_C|}[s/V]$, it must be as low as possible to improve the VTC linearity by reducing the output jitter.

4.3.3 VTC Specification

The VTC is the auxiliary circuit that converts the input analog signal from the voltage domain to the time domain, and so it should not limit the ADC linearity. As this is a 7-bit resolution ADC, the VTC linearity should be higher than 7 ENOB. As the signal to noise ratio of the VTC is given by

$$SNR_{VTC} = 20Log\left(\frac{t_{max}}{\sqrt{2}t_{n,VTC}}\right) \tag{4.21}$$

where t_{max} is the maximum time interval between the two digital signals on the VTC output and t_{noise} is the RMS jitter noise of the VTC, $t_{n,VTC}$, given by the jitter of the two rising edges of the signals at its output.

4.3.4 VTC Interfaces

VTC-TDC

The VTC, as said before, translates the input analog signal into a time interval. However, the TDC is the block that defines the maximum time interval that can be quantified. So, the amplitude of the output signal depends on the tuning between the maximum time interval between the digital signals at the VTC's output ($t_{max,VTC}$) and the time interval that the TDC can quantify ($t_{max,TDC}$).

The maximum time interval that the TDC can quantify is the time interval that takes four folds to occur. As each fold is a RO period, the maximum time interval that the TDC can quantify is $t_{max,TDC} = 4\times T_{RO}$, where T_{RO} is the inverse of the RO's frequency.

On the one hand, if the VTC has a high enough gain so that the maximum time interval between the two digital signals ($t_{max,VTC}$) is higher than $t_{max,TDC}$, the output code will saturate. On the other hand, if the VTC gain gives a maximum time interval lower than $t_{max,TDC}$, the output code will not be

fully scaled. Due do the specs, table 1.1, the VTC gain must be controlled so that the amplitude of the output signal does not vary (in corners) more than 20%.

VTC-FF

The VTC has another specification which relates to the time interval that the FF clock signal must be HIGH to finish the last three phases, figure 4.22. It is equivalent to the FF propagation time. To assure it, the minimum time interval that the output digital signals of the VTC must be high after their rising edge is equal to the propagation time of the FF.

4.3.5 VTC Results

Operation

To analyze the VTC's operation, it is used a low-frequency input signal, to consecutive time intervals between the digital outputs of the VTC do not vary too much, allowing to verify the maximum time interval of the VTC.

Figure 4.28, shows the signals in each VCDU block of the VTC.

Figure 4.28: VCDU Signals.

The operation of the VCDU signals is in figure 4.28. The signal V_T has enough time to follow the input signal ($V_T = v_{in}$). The node of the signal V_B is first charged to the supply voltage and then discharges at a constant rate. The threshold voltage is lower than the V_B voltage at the beginning of the discharge and is high enough that the discharge rate of V_B remains constant when the digital signal rises. Figure 4.28 shows that (4.12) is the equation that translates the time interval between the two digital signals at the output of the VTC.

Linearity

A block is created with Verilog-A code to test the linearity of the VTC. The clock signal and the two digital signals at the output of the VTC are the three inputs of this block. At each clock period, this block registers the time instant that the VTC's output signals cross 50% of the supply voltage in a rising edge and compute the time difference between those time instants. At the output of the block, there is a signal that behaves as the input signal. At each clock period, the block outputs the time interval, in picoseconds, between the two VTC's digital signals. A sinusoidal signal at the ADC's input, with frequency f_{in}, leads to the signal generated also be a sinusoidal signal with the same frequency, figure 4.29.

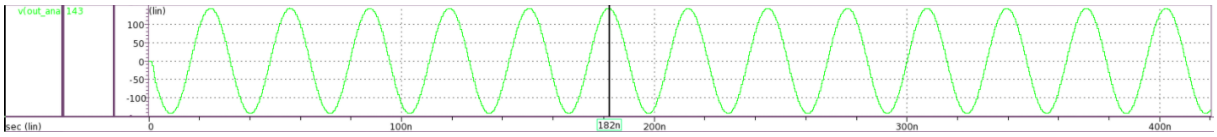


Figure 4.29: Verilog-A Signal Generated with Sinusoidal Input.

The simulator takes the Verilog-A generated signal and evaluates its linearity through the FFT and the SNR computation. The linearity given by the simulation can be predicted by the relation between the amplitude of the signal generated by the Verilog-A block and by the time noise, jitter, related to the time interval that the same digital signal at the output of the VTC can occur. Monte Carlo simulations are used to quantify the time noise. As the linearity of the VTC is (4.21), the maximum time interval and the time noise are composed to compute the predicted SNR, and then it is compared with the given SNR from the simulator.

Process	$V_{DD]}$	Temperature	t_{max}[ps]	t_{noise}[ps]	SNR_{calc} [dB]	SNR_{sim} [dB]	ENOB
typ			123	18.11	64.1	61.7	9.96
ss	MAX	MAX	116	13.41	66.2	57.8	9.31
		MIN	103	14.93	64.2	54.4	8.74
	MIN	MAX	154	11.00	70.4	51.7	8.30
		MIN	143	38.28	58.9	51.5	8.27
ff	MAX	MAX	98	8.48	68.7	56.4	9.08
		MIN	101	13.67	64.8	64.9	10.48
	MIN	MAX	146	19.33	65.0	54.6	8.78
		MIN	127	17.28	64.8	40.9	6.50
sf	MAX	MAX	111	16.39	64.1	56.4	9.07
		MIN	107	18.61	62.6	59.6	9.60
	MIN	MAX	153	7.46	73.7	46.5	7.44
		MIN	129	36.13	58.5	37.0	5.85
fs	MAX	MAX	105	14.97	64.4	56.2	9.04
		MIN	97	12.10	65.5	58.0	9.33
	MIN	MAX	145	26.11	62.3	56.4	9.07
		MIN	132	38.08	58.2	47.6	7.61

Table 4.3: VTC Linearity.

As seen in table 4.3, the linearity, translated by the SNR, computed is always higher than the linearity given by the simulator. It happens for mainly two reasons. The first reason is that there are other noise sources in this circuit, such as the clock signal or the current reference. The second reason is the channel length modulation on the transistor that behaves as a current source, which increases the VTC's non-linearity. The channel length modulation generates variations in the current during the discharging processes, and so the relation between the input signal and the time interval between the digital signals is not exactly (4.12). The channel length affects more the corners where the threshold voltage of the cross detector is lower (minimum temperature and minimum supply voltage) because the v_{DS} voltage of the current reference transistor is not high enough to assure that this transistor remains in the saturation for all the discharging process.

There two cases that the VTC's linearity did not meet the specification (minimum temperature and supply voltage, processes FF and SF). In those cases, for high amplitude voltage, the threshold voltage of the VTC is lower than the initial voltage V_B, so the output of the corresponding VCDU instantaneously rises, then this rise time is not defined by (4.11). For those cases, the relation between the input voltage and the time interval at the VTC's output is not (4.12), for all the amplitude of the input signal, justifying the degradation of the VTC linearity. The threshold voltage of the cross detector could increase to solve the limitation, by increasing the size of the PMOS transistor of the first inverter. However, it leads to an increase in the threshold voltage of the cross detector of every corner, and for some of them, when the input voltage is small, the VCDU would have not enough time to generate the output digital signal. The

discharging current could increase to solve the problem. However, increasing the current will lead to a lower gain and, consequently, the maximum time interval between the two digital signals, which leads to a reduction of the ADC output amplitude. So, the decision was to assume the nonlinearity of those corners, keeping the good results of the other ones.

VTC-TDC

Another aspect studied is the maximum time interval at the output of the VTC and the maximum time interval that can be quantified by the TDC. The figure 4.30 show the amplitude of the time interval between the digital signals at the output of the VTC and the maximum time interval that the TDC can quantify.

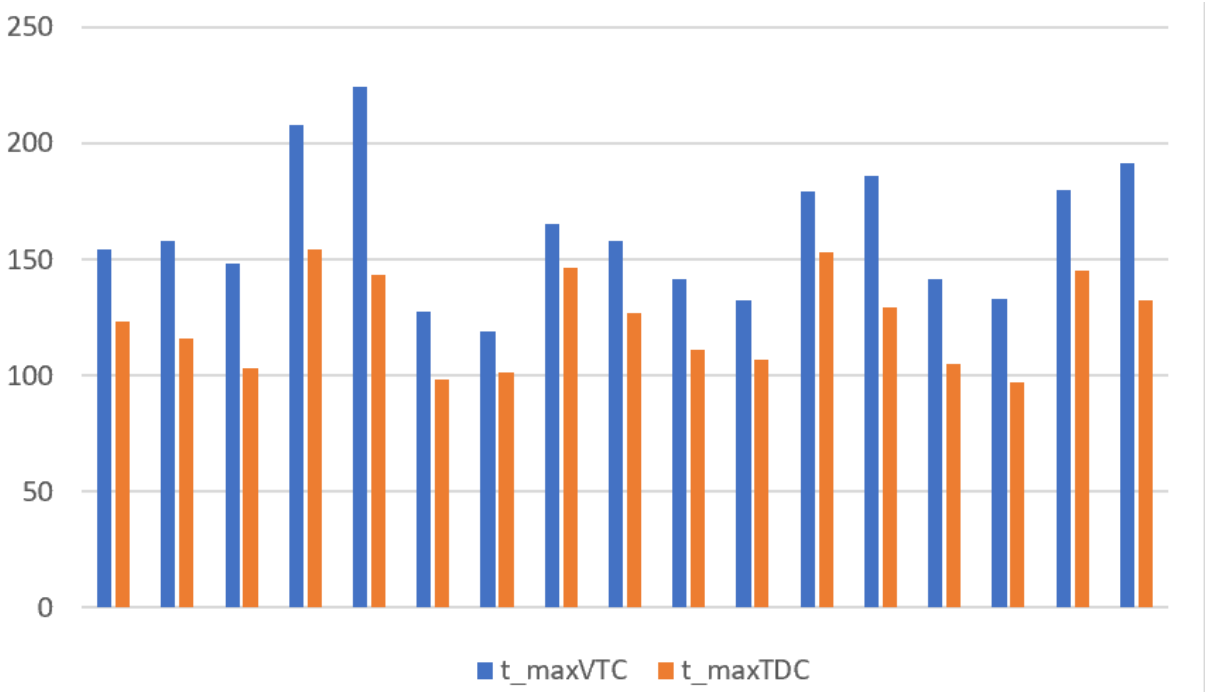


Figure 4.30: TDC and VTC Maximum Time Intervals.

In figure 4.30, the maximum time interval at the VTC's output is always lower than the maximum time interval the TDC can quantify, showing that there is no saturation. It also shows that the amplitude of the ADC's output will not be fully scaled. In figure 4.30, the maximum amplitude is 57, $\approx 94\%$ of the maximum, and the minimum amplitude is $\approx 82\%$. Then, there is 12% variation between the maximum and the minimum amplitude, confirming the specification.

This result also allows for the evaluation of the SNR values. To better describe the linearity of the VTC, the SNR value must scale for the maximum time interval allowed at each corner. So, the linearity is now computed by

$$SNR_{VTC} = 20Log(\frac{t_{LSB} \times 2^N}{2\sqrt{2}t_{noise}}), \tag{4.22}$$

where $\frac{t_{LSB} \times 2^N}{2}$ is the maximum time interval that the TDC can quantify.

Process	V_{DD}	Temperature	t_{max}[ps]	SNR_{sim}[dB]	ENOB	SNR_{cor}[dB]	ENOB
typ			123	61.7	9.96	63.7	10.29
ss	MAX	MAX	116	57.8	9.31	60.5	9.75
		MIN	103	54.4	8.74	57.5	9.26
	MIN	MAX	154	51.7	8.30	54.3	8.73
		MIN	143	51.5	8.27	55.4	8.91
ff	MAX	MAX	98	56.4	9.08	58.7	9.46
		MIN	101	64.9	10.48	66.3	10.72
	MIN	MAX	146	54.6	8.78	55.1	8.87
		MIN	127	40.9	6.50	42.8	6.81
sf	MAX	MAX	111	56.4	9.07	58.5	9.42
		MIN	107	59.6	9.60	64.6	10.44
	MIN	MAX	153	46.5	7.44	48.0	7.68
		MIN	129	37.0	5.85	40.1	6.38
fs	MAX	MAX	105	56.2	9.04	58.7	9.47
		MIN	97	58.0	9.33	60.7	9.79
	MIN	MAX	145	56.4	9.07	58.2	9.38
		MIN	132	47.6	7.61	50.8	8.14

Table 4.4: VTC Linearity Correction.

The results of table 4.4 allow concluding that the VTC does not limit the ADC linearity bellow the 6 ENOB specification.

VTC-FF Interface

In figure 4.31 it is compared the FF propagation time with the minimum width of the digital signal at the output of the VTC.

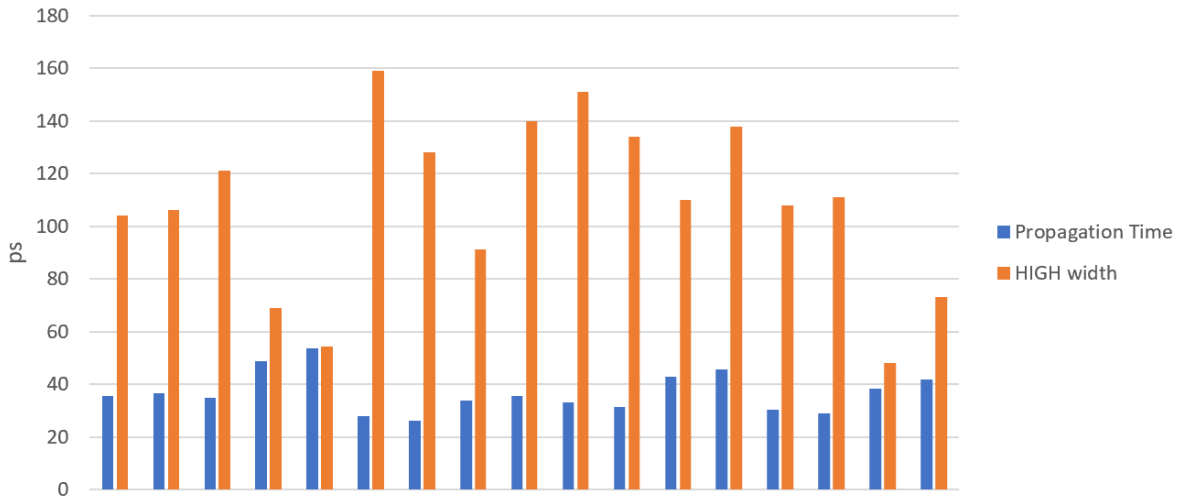


Figure 4.31: FF propagation time VS minimum width of the digital signal at the output of the VTC.

As seen in figure 4.31, the VTC-FF specification meets for all the corners. However, there is a corner that FF's propagation time and the width of the digital signal are close. In this corner, on the digital signals that translate the maximum time interval, the first signal occurs too late, and the second signal occurs almost at the end of the clock period. Then, when it happens, V_B is already being pre-charged at V_{DD} and so the output signal (t) only has the propagation time of the threshold cross detector to keep the logic level HIGH. If the first rise occurs sooner, there would be no issue, but it could lead to one out of two things: either a reduction of the VTC gain, which would lead to a reduction of the amplitude of the output ADC signal; either an increase of the threshold voltage of the cross detector, which would lead to in some corners, more than those that already happens, the threshold voltage becomes higher than the initial V_B at the beginning of the discharge and so the digital signal, t, is not related to the input amplitude, but it rises right after the initiation of the discharging, and it leads to nonlinearities on the VTC.

4.4 Decoder

The decoder decodes the state sampled by the signals t_+ and t_- and then compute the difference between those two states. Each state has two bits from the Counter, which are the most significant, and four bits from the ring oscillator. The Counter signal's decoder is in figure 4.14. C0 and C1 are the two signals that also are the two most significant bits of the state, and V is the redundancy bit that helps to identify the folding period of each state. The RO decoder is in figure 4.32.

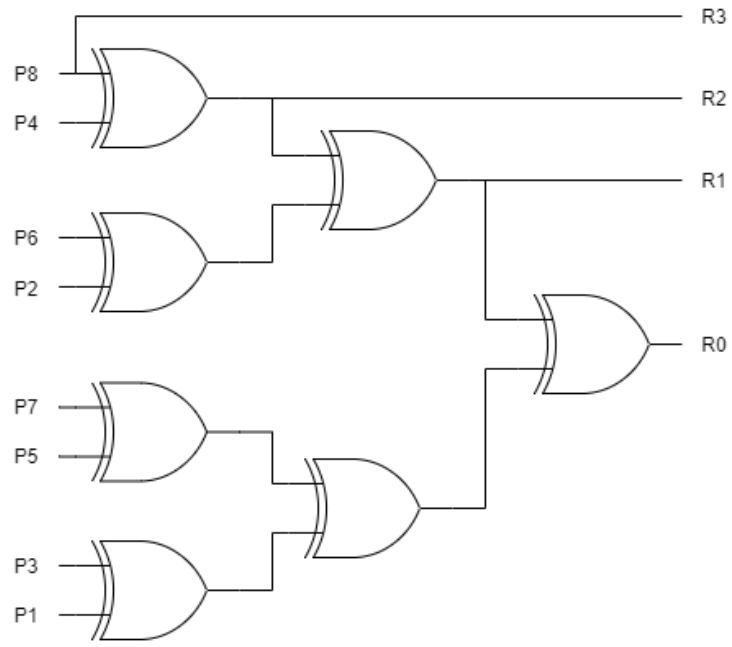


Figure 4.32: RO Decoder.

In figure 4.32, the signals P1 to P8 are the sampled signals of the RO output phases.

The implementation uses a 6-bit Ripple Carry Adder to compute the difference between the two states, defined by t_+ and t_-, figure 4.33(a).

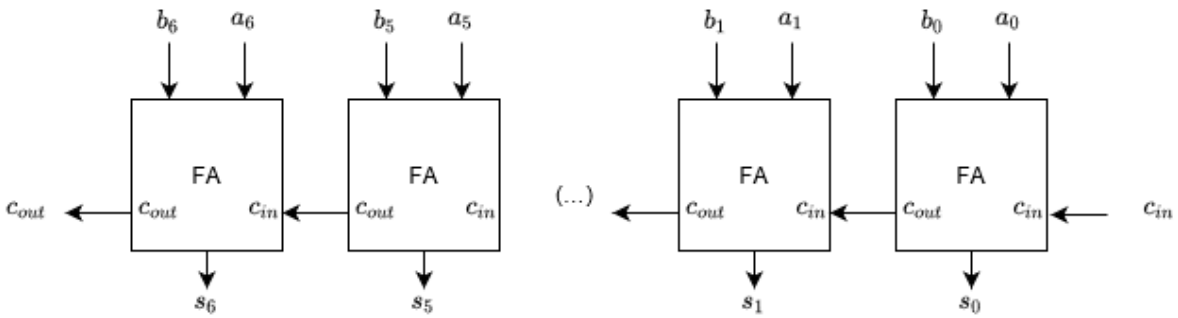


Figure 4.33: State Differentiation and MSB Generation.

The ripple carry adder is composed of six full adder structures, shown in figure 4.34.

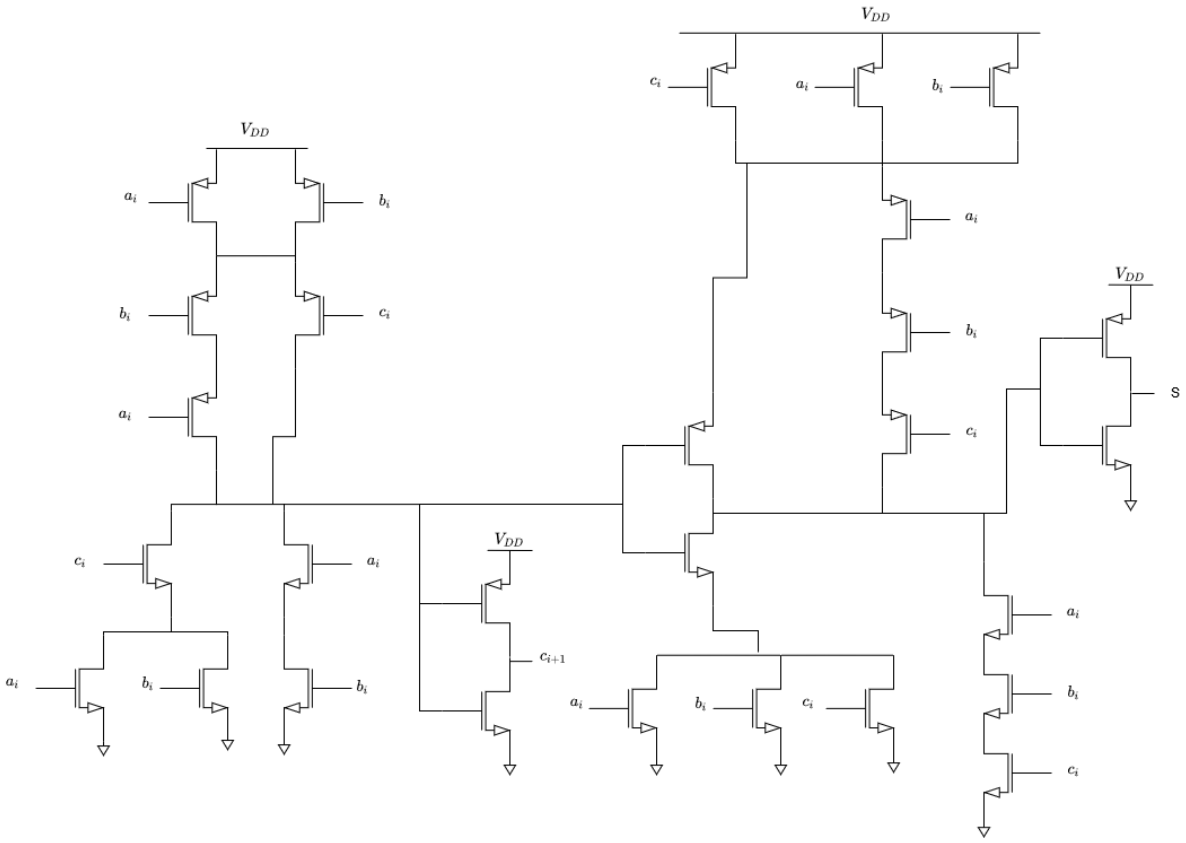


Figure 4.34: Ripple Carry Adder.

To compute the difference between the state defined by t_-, EN, and the state defined by t_+, EP, it is computed $EN + \overline{EP} + 1$, as seen in figure 4.35.

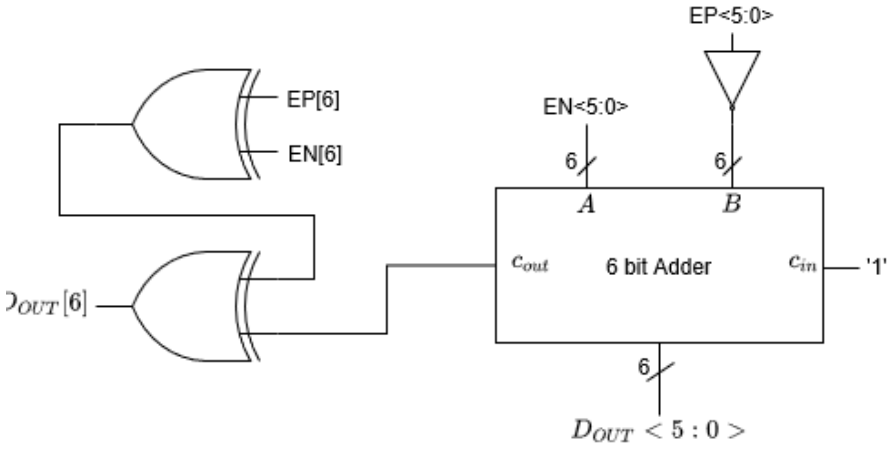
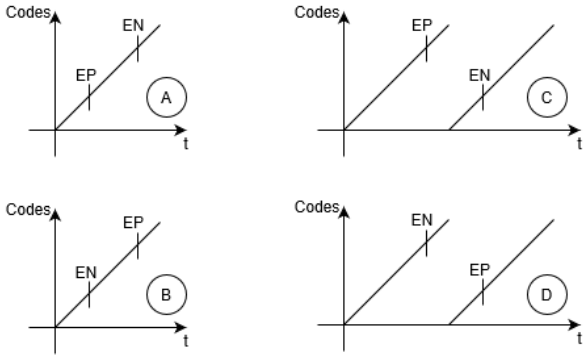


Figure 4.35: State Differentiation and MSB Generation.

In figure 4.35, the MSB of each state, $EP[5]$ and $EN[5]$, are the redundancy bit of the Counter that identify if the two stages belong to the same period of the folding codes or not.



Ex.	1^{st} State	Same Cycle ($0 =$ yes)	Carry Out	MSB
A	EP	0	1	1
B	EN	0	0	0
C	EP	1	0	1
D	EN	1	1	0

Figure 4.36: MSB Generation.

As shown in figure 4.36, to define the output MSB, first is checked if the states belong to the same folding period with an XOR operation. If the XOR is HIGH, it means that they belong to different periods. Then it is used the carry out of the adder that identifies if the resulting signal of the subtraction between EN and EP is positive or negative. If the carry out is HIGH, the subtraction result is positive. Then, another XOR operation combines these two pieces of information, defining the output MSB.

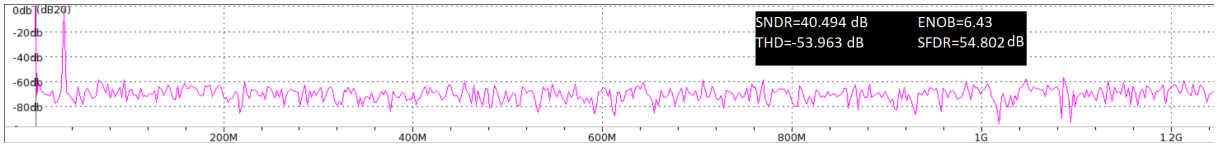
The MSB is a result of the computation of the difference between states. Therefore the ”0” code has double the size of the remaining ones. It happens because the ”0” code results when EN and EP are equal, and they are equal if t_+ and t_- differs one LSB. However, this difference can happen if t_- occurs first or t_+ occurs first. It can be corrected if at each quantifier is added a negative offset of half LSB.

Chapter 5

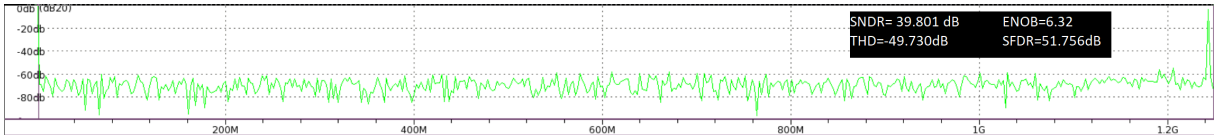
Pre Layout Simulation Results

5.1 Linearity

In order to evaluate the ADC's linearity in typical conditions, it is evaluated the output for a sinusoidal input, with two different frequencies, $f_{in} = 31.738MHz$ figure 5.1(a) and $f_{in} = 1242.676MHz$ figure 5.1(b). The frequency 1242.676MHz is the higher frequency close to the Nyquist frequency that assures a coherent sampling for a 1024 point simulation.



(a) $f_{in} = 31.738MHz$.



(b) $f_{in} = 1242.676MHz$.

Figure 5.1: Linearity Simulation.

As seen in the results of the figure 5.1, the harmonic distortion is very low, translated by the THD results, confirming that the VTC linearity is high enough to assure a high-resolution ADC.

In figure 5.1, the FFTs show that the degradation of the ADC linearity is mainly from the noise floor and not from the harmonic distortion. On the one hand, there is harmonic distortion if the mathematical relations between the input and the output of ADC's blocks show components of a high order, which does not exist. On the other hand, the noise floor is justified by the quantization error, which has the same amplitude among the full frequency bandwidth as white noise. These FFTs also show that the SNDR and the ENOB results are almost constant for all input frequency signals, once there are almost none harmonic components that degrade the ADC linearity. The inherent DEM operation leads to good linearity results once the SFDR is very high for all the frequency bandwidth.

To evaluate the robustness of the linearity, it is performed the same simulation for PVT variations.The proccess variation simulation results are in the figure 5.2, the supply voltage variation ($\pm 10\%$) simulation results are in the figure 5.3(a) and the temperature variation ($-40°C/125°C$) simulation results are in the figure 5.3(b)

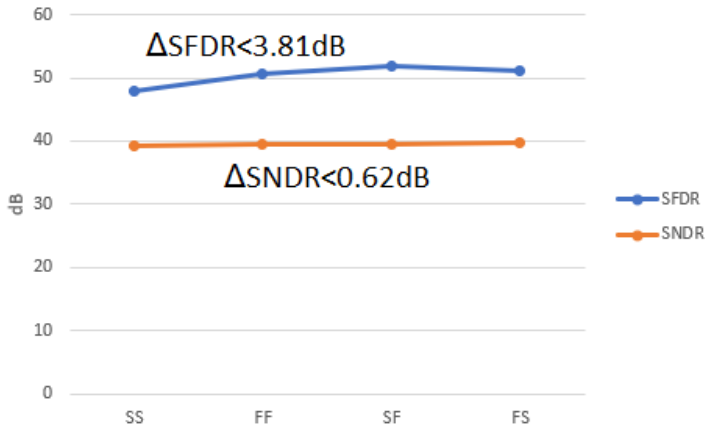
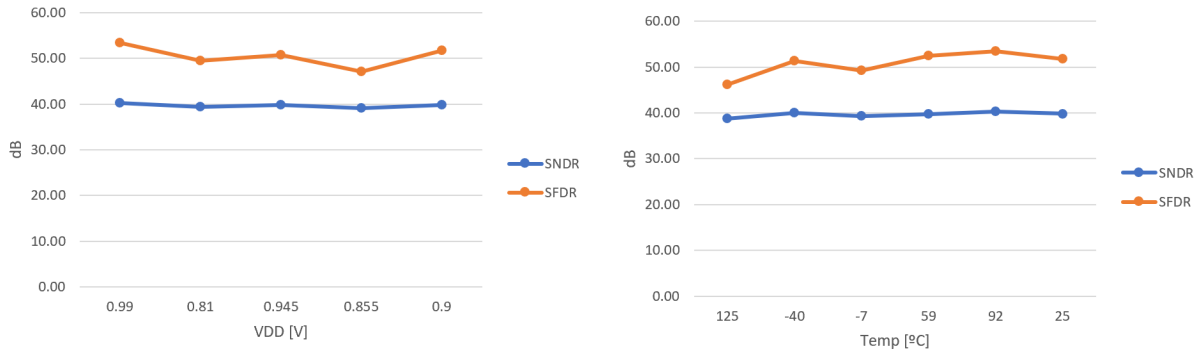


Figure 5.2: Process Variations.



(a) Supply Voltage Variation.

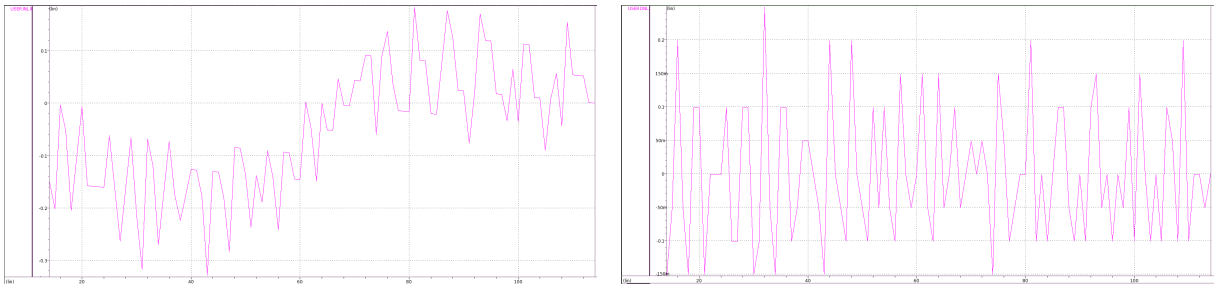
(b) Temperature Variation.

Figure 5.3: VT Variation Simulation Results.

The results of figure 5.2, show that, in terms of process, the SNDR varies about 0.62dB, and consequently that the ADC is robust in those terms. The results of figure 5.3 show that variations on the supply voltage lead to a variation of 1.03 dB on the SNDR, and the temperature's leads to 1.47 dB, which allows concluding that the ADC is robust in terms of those variations.

5.2 INL DNL

To evaluate the INL and DNL, the input of the ADC has generated a ramp signal. As the sampling frequency is $f_s = 2.5GHz$, the ADC outputs a new value every 0.4ns. As it is a 7 bit ADC, there are 128 output codes. Performing a 2048 point simulation allows that at each code there are 16 samples. The ramp signal takes $0.4 \times 128 \times 16 = 819.2$ ns to rise to evaluate the INL and DNL, figure 5.4.



(a) INL. (b) DNL.

Figure 5.4: INL and DNL Simulation.

As seen in figure 5.4, DNL$= -0.151/0.249$ LSB and INL$= -0.182/0.329$ LSB, for the 2048 point simulation. The results show that the inherent DEM operation of the folding architecture translates to highly linear ADC.

5.3 Consumption

Running at Nyquist Frequency, the overall power consumption is 33.6mW. Figure 5.5 represents the power consumption breakdown.

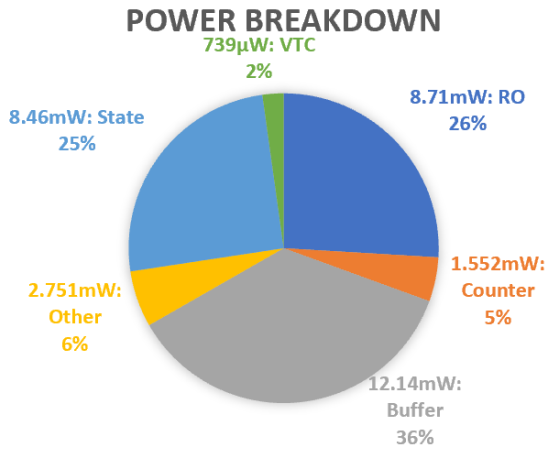


Figure 5.5: Power Breakdown.

The power consumption shown in figure 5.5 shows that output buffers of the RO and the RO are the blocks with higher consumption. The power consumption of an oscillator is given by

$$P = f_{osc} \times C_L \times V_{DD}^2 \tag{5.1}$$

where f_{osc} is the oscillation frequency, C_L is the oscillation capacitance, and V_{DD} is the supply voltage. The capacitance is a function, among other things, of the transistor sizes. So, for a high-frequency oscillator, power consumption is inevitably high. The power consumption described by (5.1) show why the buffer output has higher power consumption than the RO once the oscillation frequency is the same,

the power supply of each circuit is also the same, but the transistors of the buffer are larger than the transistors of the RO.

The results in figure 5.5 also show that the VTC has low consumption, and so the main voltage domain-dependent block of this ADC is the one with lower power consumption. This fact allows concluding that it can be designed a Time Domain Quantization ADC, based on Time Interval quantization, with low power consumption and become more competitive with the State of the Art in terms of Walden Figure of Merit.

5.4 Bandwidth

To evaluate the Bandwidth of the ADC and its PVT variation, the SNR is evaluated for six different frequencies, figure 5.6.

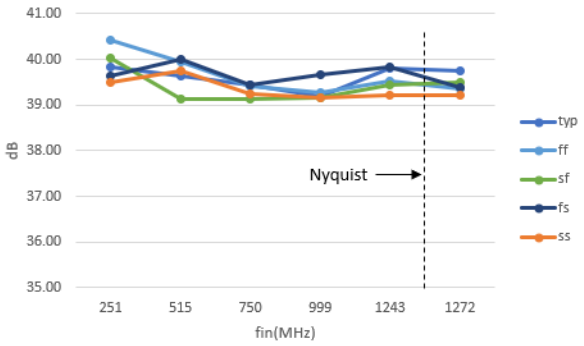


Figure 5.6: Bandwidth Evaluation.

The frequencies assure a coherent sampling for 1024 points simulations. The higher frequency is higher than the Nyquist frequency ($= f_s/2 = 1.25GHz$). As seen in figure 5.6, the ADC's bandwidth does not change in with PVT variation, and the 3dB bandwidth is higher than the Nyquist frequency. This result can also be predicted evaluating the FFT of the output signals, figures 5.7-5.11.

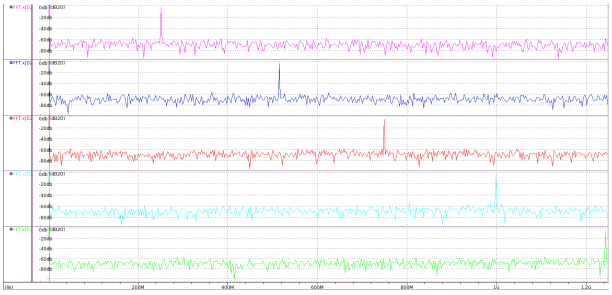


Figure 5.7: FFTs Typ Simulation.

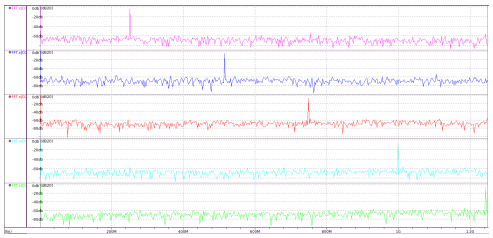


Figure 5.8: FFTs SS Simulation.

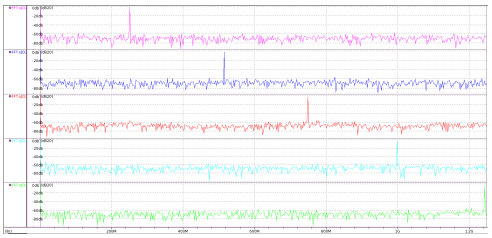


Figure 5.9: FFTs FF Simulation.

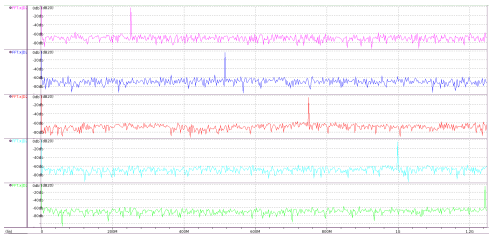


Figure 5.10: FFTs SF Simulation.

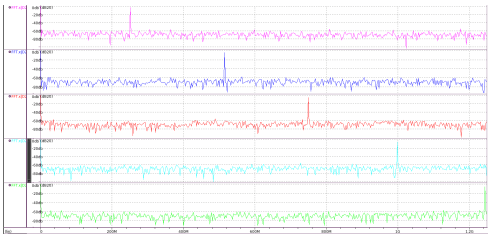


Figure 5.11: FFTs FS Simulation.

As seen in 5.7-5.11, the FFTs show that the signal to noise ratio is degraded mostly by the ground noise and not by the harmonics power. It leads to an SNR almost constant all over the Nyquist band.

The results allow concluding that the ADC's bandwidth is independent of the process variation, confirming the ADC's robustness. The results show that the Nyquist frequency is not the frequency with 3dB degradation of the SNR. It means that this is a Nyquist ADC, once it can be used any input frequency from 0Hz up to $f_s/2$ and the linearity remains almost constant.

5.4.1 Output Signal

In figures , there are two signals. A Verilog-a module generates signal v(out_analiser). At each period of the clock, the signal v(out_analiser) has the value of the time difference between the time instant that two signals at the output of the VTC rise. The signal D2Av(d) is the output of the ADC.

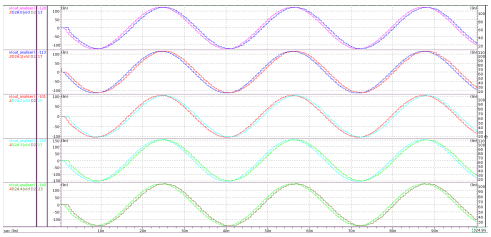


Figure 5.12: Typical and SS Simulation.

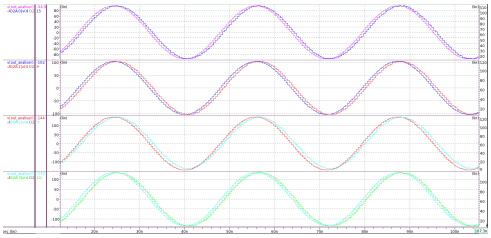


Figure 5.13: FF Simulation.

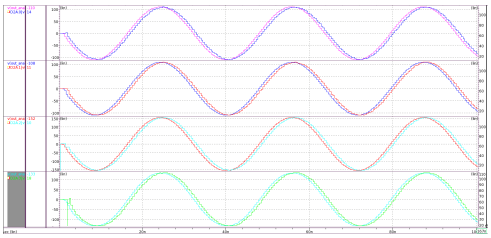


Figure 5.14: SF Simulation.

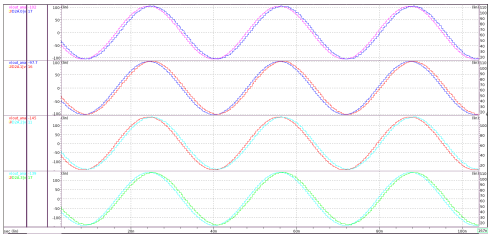


Figure 5.15: FS Simulation.

The figures show that the output of the ADC track the time interval amplitudes, displaced in time due to the pipeline operation, in which the output signal is related to the time interval of the previous clock signal. However, it is also possible to see that sometimes, the output signal has more changes than the changes on the time interval between the rising edges at the output of the VTC. It happens, once to have an output variation, there must be a variation of one LSB on the time interval between the digital signals. However, the signal computed (by the Verilog-A code) allows to show any change, and so there are variations smaller than one LSB. In other words, the signal computed is not affected by the quantization error, but the output of the ADC is, which justifies some differences between the two.

Chapter 6

Conclusions

The results of this dissertation show that Time Quantization ADCs are a solution to fight the problems due to the ever-decreasing size of the technology's devices, but they have some limitations. The first limitation is due to the conversion of the analog information from the voltage domain to the time domain, which needs to use an auxiliary VCO, converting it to frequency, or an (or multi) auxiliary VTC(s), converting it to a time interval between digital signals. These auxiliary circuits are voltage dependents, which is almost paradoxical once the point of this type of ADC is to be voltage-independent.

When the option is to quantify the frequency, which uses a VCO, the ADC will never have a Nyquist Bandwidth, as the input frequency will never be able to vary from $f_{in} = 0Hz$ to $f_{in} = f_s/2$. There are two options when choosing to quantify the frequency. The first option is to use one single channel ADC, and, inevitably, presenting a high pass first-order error shape, in which the quantization noise is amplified, for frequencies near the Nyquist frequency. This type of ADC has a lower input bandwidth. The other option is to use multiple channels of this ADC, where the first-order error shaping becomes a bandpass type, but there are some frequencies that the ADC's output does not have any information about the input signal.

Otherwise, when the option is to quantify the analog information by quantifying a time interval between two digital signals, if the implementation chosen is FLASH type, there will be a need for 2^N VTCs and 2^N FF, keeping the same area and consumption limitation of the traditional FLASH architectures of the voltage domain. It is possible to implement an interpolation approach to avoid having too many VTCs, but the area efficiency will still below, and the information about the analog information will be in only two out of the 2^N FFs.

Finally, when the decision is to use only a VTC, it is necessary to think out an architecture that the final result is not given by the difference between two quantifications, once it leads to an ADC linearity limitation of $\frac{N-1}{2}$ ENOB. The results of this work allow concluding that it is possible to design a highly linear VTC with a higher resolution than 7 bit and a TDC with sufficiently good linearity that shows linearity close to the ideal.

6.1 Achievements

The results of the ADC are shown in table 6.1.

	Specification	Result
INL	$\pm 0.5LSB$	$= -0.151/0.249$ LSB
DNL	$\pm 0.5LSB$	$-0.182/0.329$ LSB
ENOB	6	6.32 (@ $f_s/2$)
Output Amplitude Variation	$\pm 20\%$	$\pm 18\%$

Table 6.1: ADC Specification VS Results.

This work presents a 2.5 GS/s 7 bit time-domain folding ADC. It achieves highly competitive area efficiency among all recent ADC works of similar sample rate and resolution. The VTC presents high linearity and has low consumption, allowing an ADC design of high linearity for a 7-bit resolution. The RO-based folding TDC achieves high area efficiency and high speed simultaneously. The inherent DEM of the RO-based TDC is also highly linear, manifested by DNL of -0.151/–0.249 LSBs, INL of -0.182/+0.329 LSBs. Due to the double sampling limitation linearity of 6.5 ENOB for a 7-bit resolution ADC, the ADC achieves high linearity of 6.32 ENOB at Nyquist input frequency, ($f_{in} = f_s/2$), with a 33.6mW power consumption, leading to a Walden Figure of Merit $FOM_W = 168.1fJ/step$, which is an improvement when comparing with the architectures that implement time domain folding, [7, 14].

6.2 Future Work

The next step to implement this ADC is to design the layout. The total area should be small due to the area efficient folding approach.

However, for this ADC to be more competitive with the State of the Art, the consumption should be decreased, maybe abdicating of some linearity. Another improvement in this ADC should be the better control of the current PVT's variations to improve the scaling of the output signal's amplitude.

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Appendix A

Derivation of Equations

A.1 Derivation from (2.4) to (2.5)

$$\Phi[k] = \int_{-\infty}^{kT_s} \Psi(\tau)d\tau$$

$$\Phi[k] - \Phi[k-1] = \int_{-(k-1)T_s}^{kT_s} \Psi(\tau)d\tau$$

$$= 2\pi f_o T_s + 2\pi K_o \int_{-(k-1)T_s}^{kT_s} Asen(w\tau)d\tau$$

$$= 2\pi f_o T_s + 2\pi K_o A \frac{sen(wkT_s) - sen(wkT_s - wT_s)}{w}$$

$$2j(sen(wkT_s) - sen(wT_s(k-1)) = e^{jwkT_s} - e^{-jwkT_s} - e^{jwkT_s - jwT_s} + e^{-jwkT_s + jwT_s}$$

$$= e^{jwkT_s}(1 - e^{-jwT_s}) - e^{-jwkT_s}(1 - e^{-jwT_s}) = (1 - e^{-jwT_s})(e^{jwkT_s} - e^{-jwkT_s})$$

$$= e^{-jw\frac{T_s}{2}}(e^{jw\frac{T_s}{2}} - e^{-jw\frac{T_s}{2}})(e^{jwkT_s} - e^{-jwkT_s})$$

$$= (e^{jw\frac{T_s}{2}} - e^{-jw\frac{T_s}{2}})(e^{jwT_s)K - \frac{1}{2}} - e^{-jwT_s)K - \frac{1}{2}})$$

$$= 2jsen(w\frac{T_s}{2})2jsen(jwT_s)K - \frac{1}{2})$$

$$2\pi K_o A \frac{sen(w\frac{T_s}{2})2jsen(jwT_s)K - \frac{1}{2})}{w}$$

$$= 2\pi K_o A T_s \frac{sen(\pi f T_s)}{\pi 2 f T_s} 2sen(wT_s)K - \frac{1}{2})$$

$$= 2\pi K_o A T_s sinc(fT_s)u(T_s(k - \frac{1}{2}))$$

$$y[k] = N_\phi K_o A T_s sinc(fT_s)u(T_s(k - \frac{1}{2})) + N_\Phi f_o T_s + \Delta\Phi_\epsilon$$

A.2 Derivation from (2.4) to (2.6)

$$\Phi[k] = \int_{-\infty}^{kT_s} \Psi(\tau)d\tau$$

$$\Phi[k] - \Phi[k-1] = \int_{-(k-1)T_s}^{kT_s} \Psi(\tau)d\tau$$

$$= 2\pi f_o T_s + 2\pi K_o \int_{-(k-1)T_s}^{kT_s} u(t)d\tau$$

In figure A.1 is shown the input signal of the ADC, $v_{in}(t)$, and the signal after the sampling block, $u(t)$, which is the input signal of the VCO.

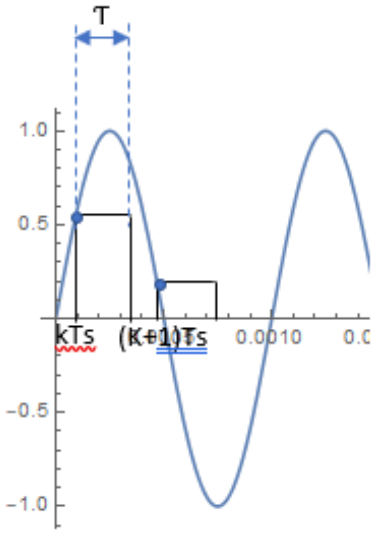

Figure A.1: Sampling a sinusoidal wave with retention.

From A.1 it can be seen that

$$\int_{-(k-1)T_s}^{kT_s} u(\tau)d\tau = \tau u((k-1)T_s)$$

$$\Phi[k] - \Phi[k-1] = 2\pi f_o T_s + 2\pi K_o \tau u((k-1)T_s)$$

$$y[k] = N_\Phi f_o T_s + N_\Phi K_o \tau u((k-1)T_s) + \Delta\Phi_\epsilon$$