Power Conditioning Unit for a Harvester Circuit
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Abstract—This work presents a Power Conditioning Unit (PCU) for autonomously powered devices. Autonomous powered devices are passive systems and require an harvester circuit followed by a PCU to manage the power delivered to a load circuit. These systems assume a relevant role in the design of biomedical implants and wireless sensor networks. As different energy sources are accountable (sunlight, vibrations, RF) and its power is dependent on external conditions, it is important that the passive systems are tolerant to the harvested power variability. For this reason, the proposed PCU applies an intermittent load activation control and a power limiting functionality. Furthermore, it has to have a negligible idle power dissipation, when compared to the low power output provided by state-of-the-art harvesters (< 1 µW). The PCU uses a voltage sensor with hysteresis and a voltage limiter to control the load activation and define the maximum voltage. The load activation and deactivation voltages, and maximum voltage are known as transition voltages. Both blocks are based on a low voltage circuit composed by a pico-watt reference and a CMOS inverter, providing a voltage sensing, while imposing a maximum steady state current equal to 2 nA. The PCU is designed in a 130 nm process at simulation level and is able to control the transition voltages with a ±10 % precision on a −25 °C to 90 °C range.

Index Terms—Energy Harvesting, Voltage Sensor, Voltage Limiter, Low Power, Temperature Compensation.

I. INTRODUCTION

Wireless power transmission is a relevant research field for its role on the development of autonomously powered devices. These correspond to electronic devices that only require the energy provided by harvesting to operate. The circuit responsible for providing the energy to the system is known as energy harvester. Nowadays, the temperature gradients, vibrations, sunlight, and Radio Frequency (RF) waves are some of the accountable external sources that can be harvested.

The combination of an harvester and a load circuit is known as passive system. In order to store the harvested energy, usually a capacitor is used at the harvester output. Considering previous studies [1], it is verified that the RF harvesters provide less power than other external sources. As verified by the state-of-the-art [2], [3] the RF harvesters power output is approximately 1 µW for a 10 µW input. Based on these facts, a major focus is given to the RF harvesters in this work.

Commonly RF harvesters are used to supply low power circuits, such as front-end interfaces, memory cells and sensors. The Radio Frequency Identification (RFID) systems [4]–[6] are one of the examples, which are used for shopping tags and Smart Card transportation tickets. Another applications are the Wireless Sensor Networks (WSNs) [7], which can be applied for forest surveillance, and the biomedical implants [8], [9].

As stated by the Friis formula, the power that arrives to the RF based passive system, depends on its distance from the RF source. Therefore, the power provided by the harvester presents an undesired variability to the load. To counter this problem, Power Conditioning Units (PCUs) are applied in the passive system between the energy harvester and the load circuit. In order for the circuit to operate correctly and not be damaged, a PCU stabilizes and limits the power delivered to the load. Moreover, it controls the activation of the load circuit. This last characteristic is a key function for low power harvesters, once that it allows the passive system to operate intermittently. When an intermittent operation is applied, the passive system is based on charge and discharge cycles [7]. Hence, on the charge phase, the system harvests the energy and stores it in the capacitor. When the capacitor charge is sufficiently high to deliver the power required by the load, the system is discharged.

The state-of-the-art PCUs [7], [10] are based on three functions: stored energy evaluation, load activation and power delivery. The energy evaluation function, corresponds to the sensing of the voltage at the capacitor terminals. Depending on that voltage, the load is activated or deactivated. Finally, when the load is activated, the power delivered to the load has to be regulated and limited. Therefore, the circuit blocks used to implement such functions are voltage sensors, voltage regulators and voltage limiters.

Due to its advantages, the developed PCU applies a voltage sensor circuit to implement an intermittent load operation. It assumes that the load can be activated for a supply equal to 1.2 V, and must be deactivated for a supply lower than 0.4 V. To ensure that an overvoltage does not occur, the PCU also contains a voltage limiter, which imposes a maximum voltage of 1.5 V. Although a voltage regulator is critical for a correct load operation, the implementation of this feature is not included in this work. Based on the state-of-the-art RF harvesters, it is imposed that a 1 µA current output can be provided to a 1.2 V load. For the passive system to be considered power efficient, the power required by the PCU has to be lower than the harvested. Thus, a 10 nW power specification is imposed to the PCU design. Although a major focus is given to RF, the assumed circuit design considerations can be applied to other types of energy harvesters. The PCU is implemented at simulation level in the UMC 130 technology with high speed transistors only, to reduce the Integrated Circuit (IC) cost. Furthermore, a ±10 % precision tolerance is imposed for the transition voltages (0.4 V, 1.2 V and 1.5 V) considering a temperature range from −40 °C to 100 °C and fabrication process corners.
Once the motivation and research goals are defined, the structure of this work is defined as follows: Section II introduces the passive system internal structure and reviews the state-of-the-art PCUs; Section III proposes a transistor level review on the circuits commonly used in the PCU literature; Section IV presents the complete design procedure from the high level circuit structure to the layout implementation of the voltage sensor and limiter; Section V provides the final considerations on the developed PCU, comparing the results obtained to those proposed.

II. POWER CONDITIONING

The main purpose of this chapter is to verify the power conditioning role on passive systems. In order to do it, firstly the passive systems structure and operation are defined. Then, the internal blocks that constitute state-of-the-art PCUs are generically characterized.

A. Overview

To understand the passive system operation, each of the blocks influence on the power delivering process to the load circuit has to be verified. Figure 1 presents an equivalent high level model of the passive system. The energy harvester and load circuits are replaced by ideal electrical components, whereas the PCU is defined as a circuit block that outputs $V_{Load}$ based on the supply generated by the harvester, defined as $V_{DC}$. In order to explain the model, each block is analysed.

In the model of Figure 1, the energy harvesting block is composed by a current source $I_S$ and a capacitor $C_{Out}$. The current source value correlates to the power that the harvester is able to provide to a circuit. $C_{Out}$ is the element responsible for storing the harvested energy.

The conditioning unit can be interpreted as a gate that establishes the power link between the harvester and the load. Recalling section I, to fully accomplish that role, the conditioning unit is responsible for three different functions: stored energy evaluation, load activation and power delivery. Regarding the first conditioning function, the energy stored in a capacitor is directly related to the voltage at its terminals. Therefore it is required that the PCU performs a voltage sensing of $V_{DC}$. By doing this function, the load can be activated or deactivated based on the $V_{DC}$ value. The activation occurs for $V_{DC} = V_{ON}$, which turns ON the PCU output, equivalently $V_{Load} > 0$ V. The deactivation is set by $V_{DC} = V_{OFF}$ and results in turning OFF the output signal, $V_{Load} = 0$ V. The power delivery occurs when the load is active. This last PCU function is divided in two parts: voltage regulation and limiting. Voltage regulation is used to generate a $V_{Load}$ stable and independent of $V_{DC}$. The voltage limiting consists in imposing a maximum $V_{DC}$ value, defined as $V_{Lim}$, when an overvoltage occurs.

For the PCU design point of view, the load circuit can be interpreted as resistor $R_L$ (Figure 1) with voltage and operating time requirements.

B. System Operation

The passive system, described by Figure 1, operation depends on the power harvested and the power required by the system, which corresponds to the power delivered to the PCU and load circuit. When the harvested power is below the power required, the load can only operate intermittently, once it relies on the energy stored in $C_{Out}$. The $V_{DC}$ and $V_{Load}$ voltages behave as presented in Figure 2 for an intermittent operation. The time $t_0$ corresponds to the start-up time, which is the time required for the discharged passive system to reach $V_{ON}$. At $t_1$ the load operation is interrupted, because the capacitor discharge leads to $V_{DC}=V_{OFF}$. The period between the $t_0$ and $t_1$ is defined as the load active period $\Delta t_{ON}$.

![Fig. 2. Passive system supply voltage ($V_{DC}$) for the intermittent operation.](image)

When the harvested power is higher than the required by the load, the passive system operates continuously. When $V_{DC}$ continues to rise despite the load activation, a voltage limiting mode at $V_{DC}=V_{Lim}$ is imposed, depicted in Figure 3. The time between the load activation $t_0$ and the limiter activation $t_L$ is defined as $\Delta t_L$.

![Fig. 3. Passive system supply voltage ($V_{DC}$) for the voltage limiting operation.](image)
C. PCUs Review

After describing the passive system blocks and their influence in the overall operation, the PCU internal structure and the circuit blocks required for this work (voltage sensor and limiter) are presented. As illustrated in Figure 4, the PCU follows a two-stage structure. The first is composed by the voltage sensor, which evaluates the harvested energy and activates the load by turning ON the voltage regulator circuit. The second stage is composed by a voltage limiter and a voltage regulator to fully ensure the power delivery function.

![Fig. 4. State-of-the-art PCU structure composed by a voltage sensor, a limiter and a regulator that outputs the load voltage supply V_{Load}.](image)

A voltage sensor, also referred as Power-ON Reset (POR) in the PCU literature [5], [6], [11], [12], is usually implemented by a comparator based circuit, following the structure presented in Figure 5. It compares the sensed voltage V_S to a supply independent voltage (V_{REF}). When V_S becomes higher than V_{REF}, the comparator output V_O switches from zero to V_{DC}. The V_{DC} where V_O toggles between voltage levels is known as transition voltage, defined by V_{TR}. Once V_{TR} is configured by a voltage divider and by the fixed V_{REF} value, by using three resistors R_U, R_D and R_H, as presented in Figure 5(a), a hysteresis behaviour can be imposed. Thus, for V_O = 0 V a voltage division ratio

$$\alpha_0 = \frac{V_S}{V_{DC}} = \frac{R_D}{R_U + R_D}$$  \hspace{1cm} (1)

is defined, whereas for V_O = V_{DC} the ratio is changed to

$$\alpha_1 = \frac{R_D}{R_U + R_H + R_D}.$$  \hspace{1cm} (2)

As V_S becomes dependent of the comparator output, V_O is activated at V_{DC} = V_{ON} and deactivated at V_{DC} = V_{OFF}, as illustrated in Figure 5(b).

Although a voltage limiter can be implemented simply by several diodes in series connecting V_{DC} to ground [6], [10], [13], the circuit presented in Figure 6(a) is more efficient [5], [7], [9], [13], [14]. It uses a voltage sensor without hysteresis to activate a low impedance path, based on a N-type Metal Oxide Semiconductor (NMOS) transistor. As illustrated in Figure 6(b), by setting the division ratio \( \alpha \) to activate V_O at V_{DC}=V_{Lim}, a current I_{disc} is imposed. Once V_O = V_{DC} after the V_{Lim} transition, the V_{DC} increase, causes also an I_{disc} increase. In turn, this leads to a V_{DC} reduction. Therefore, a feedback structure is formed by the I_{disc} relation to V_{DC}. This allows the passive system supply to stabilize in V_{Lim} by dissipating the excess harvested power, as shown in Figure 6(b).

![Fig. 5. (a) Schematic of a voltage sensor with hysteresis behaviour. (b) Plot of the sensed voltages V_S resultant of the division ratios \( \alpha_0 \) and \( \alpha_1 \), and the corresponding sensor output V_O characteristic.](image)

III. PCU CIRCUITS

Based on the analysis of section II, the voltage sensors and limiters rely on comparators and voltage reference circuits. Considering the power and precision specifications imposed, those circuits are analysed for both typical conditions, temperature and process corners. To do it, the operating regions and Process, Voltage and Temperature (PVT) influence on the MOS transistors is initially reviewed.

A. MOS transistors review

The current on a MOS transistor is primarily dependent on its gate-to-source voltage V_{GS}, drain-to-source voltage V_{DS} and threshold voltage V_{th}. The expression that describes its
current on the strong inversion saturation region \((V_{DS} \geq V_{GS} - V_{th})\) is
\[
I_D = \frac{1}{2} \mu C_{ox} W \frac{L}{L} (V_{GS} - V_{th})^2,
\]
where \(\mu\) is the charge-carrier effective mobility, \(C_{ox}\) is the oxide capacitance and \(W\) over \(L\) is the relation of the width and length of the transistor. In order to reduce the current in a saturated transistor, its length can be increased, or its \((V_{GS} - V_{th})\) term, known as overdrive voltage, can be decreased. If the overdrive voltage becomes lower than 0 V, the MOS operates in the subthreshold, which contains the weak inversion region [15]. Compared to strong inversion, a weak inversion biasing allows a greater current reduction, nonetheless it also imposes a slower circuit operation [16]. The current on weak inversion saturation region \((V_{DS} > 4U_T)\) is modelled by [17]
\[
I_{DS} = I_{SO} \exp \left( \frac{V_{GS}}{nU_T} \right),
\]
where specific current \(I_{SO}\), is defined as
\[
I_{SO} = \mu \frac{W}{L} U_T^2 C_{ox} \exp \left( \frac{-V_{th}}{nU_T} \right).
\]
Such current presents an exponential dependence on \(V_{GS}, V_{th}\), subthreshold swing parameter \(n\) and thermal voltage \(U_T\).

Once the MOS transistor operation regions are defined, the influence of the temperature and process corners on the transistor parameters is analysed. Besides the thermal voltage \((U_T)\) variation, the temperature influence is mainly noticed on the mobility \((\mu)\) and threshold voltage \((V_{th})\). \(U_T\) and \(V_{th}\) are known to increase with temperature, whilst \(\mu\) to decrease with it. However, the \(V_{th}\) effect for low currents is more significant than \(\mu\). Consequently, in weak inversion the current increases with temperature.

A process corner represents a fabrication condition imposed by the technology foundry that causes the worst shift on the semiconductor device properties. Considering MOS devices, the corners state how fast or slow is the produced N or P type transistor relatively to a typical case. In a fast corner, the mobilities \(\mu\) are increased and threshold voltages \(V_{th}\) decreased, whereas in a slow corner the opposite is verified.

### B. Comparator Circuits

The PCU literature usually apply simple, well-known circuits as the differential pair [5], [7], [9], [13] and the Complementary MOS CMOS inverter [12] to implement the required voltage comparison. That is verified because they present a good power to performance trade-off when power dissipation is a design specification.

The differential pair is an amplifier circuit that affects the amplitude of the differential signal applied at its inputs. Applying large amplitudes makes the circuit leave the linear region and its output saturates, providing two voltage levels, zero and the supply voltage. Commonly the topology used is the presented in Figure 7(a), also known as the pseudo differential pair. To make the output \(V_{O1}\) or \(V_{O2}\) saturate, the current on one of the branches has to be higher than the other, thus the transition occurs when the currents are equal. If the transistor pairs \(M_3, M_4\) and \(M_1, M_2\) have the same sizes, then the comparison offset \(V_{OS}\) is zero, as the input voltages \(V_{I1}\) and \(V_{I2}\) impose the same current on both branches when they have equal values.

The CMOS inverter, presented in Figure 7(b) is normally used as logic gate that operates with digital signals, presenting a fast transition between the voltage levels, as desired for a comparator. The output toggles when \(V_I\) reaches a transition voltage that is usually half of the supply voltage. This circuit presents an high resistance path from \(V_{DD}\) to ground, because there is always one transistor in the cut-off region, except during the transition, where both \(M_N\) and \(M_P\) are saturated. Such characteristic makes the circuit steady state current to be very low.

By comparing both circuits under the same conditions, the inverter has a lower power dissipation. Nonetheless the inverter presents a high sensitivity to PVT variations, once that its transition voltage depends on the transistors parameters. On the differential pair, the PVT effect is mitigated by making \(M_3, M_4\) and \(M_1, M_2\) have the equal sizes.

### C. Voltage References

The design of a voltage reference circuit has to account for the voltage value generated, the supply and temperature influences on it, and the power dissipated. The reference output \(V_{REF}\) dependence on the supply voltage is known as the line sensitivity. The temperature influence on \(V_{REF}\) is defined by the figure of merit known as the Temperature Coefficient (TC). The temperature independence can be achieved, as occurs in bandgap circuits. Nonetheless these require a power in the micro-watts range [7], [18], which is not feasible to apply in the described system.

Commonly, the circuit of Figure 8(a) is applied to provide a reference voltage \(V_{REF}\) for PCUs [5], [6], assuring the supply independence with reduced design time. The \(V_{REF}\) provided is imposed by the saturation current of the Bipolar Junction Transistor (BJT).

On Figure 8(b) another reference is presented, which is proposed by [18]. This simple design known as the 2T topology has a pico-watt power dissipation. It applies a negative \(V_{GS}\) on the upper transistor \(M_C\) to impose a subthreshold operation and significantly reduce the voltage reference circuit current. The generated \(V_{REF}\) is mainly defined by the \(M_D\) and \(M_C\)
thresholds difference \( (V_{thD} - V_{thC}) \). Thus it is required that such difference is great enough to produce a positive \( V_{REF} \).

Comparing both circuits, the proposed by Figure 8(b) presents a lower power dissipation and does not use BJT devices, which is advantageous for IC design.

IV. PROPOSED PCU

A. Structure and Design Considerations

As previously referred, the circuit blocks required to implement an intermittent operation and a voltage limiting, are the voltage sensor and voltage limiter, respectively. In order to match the specifications proposed in the research goals, the transition voltages are: \( V_{ON} = 1.2 \text{ V} \), \( V_{OFF} = 0.4 \text{ V} \) and \( V_{Lim} = 1.5 \text{ V} \). The applied PCU structure is presented in Figure 9. The PCU output is the power enable signal \( (P\_EN) \) provided by the voltage sensing circuit. This allows the control of the load activation by using a switch. Once \( V_{ON} < V_{Lim} \), the voltage sensor output is also used to activate the voltage limiter sensing part.

In order to verify the expected \( V_{DC} \) charge and discharge behaviours (section II) that characterize the intermittent and voltage limiting operations, an ideal voltage source cannot be used. Thus, the testbench presented in Figure 10 is used. In fact, this results from the passive system high level model defined in the power conditioning review (Figure 1). The current source \( I_S \), capacitor \( C_{Out} \), switch and load resistance \( R_L \) used in the testbench are ideal. The \( I_S \) and \( R_L \) values are changed in order to simulate different operating modes. \( C_{Out} \) is fixed to 50 nF, which is considered sufficient for an intermittent passive system with a \( I_S = 1 \mu\text{A} \).

B. Voltage Sensor

The applied voltage sensor follows the structure presented in Figure 11, where \( V_{DC} \) is the input, and \( P\_EN \) and \( P\_EN' \) the outputs. The comparator and reference circuits compose the voltage sensing core, due to its main role on detecting the transition voltage through the voltage sensed, defined by \( V_S \). In the case of the proposed voltage sensor, the transition voltage, generically defined by \( V_{TR} \), corresponds to the \( V_{DC} \) where \( P\_EN \) and \( P\_EN' \) toggle between voltage levels. To reduce the power dissipation, the comparator supply voltage is the sensed voltage and the down resistance of the voltage divider is eliminated. As later explained, the down resistance is provided by the load imposed by the circuit supplied by \( V_S \). The voltage level shifter is used to shift the voltage sensor output to \( V_{DC} \). The shifted \( V_S \) is \( P\_EN \), whilst \( P\_EN' \) corresponds to its logical opposite. In order to implement the hysteresis behaviour, the resistors \( R_{U0} \) and \( R_{U1} \) are accompanied with switching interfaces controlled by the level shifter outputs. The division ratio achieved with \( R_{U0} \) defines the \( V_{ON} \) transition, whilst the ratio established by \( R_{U1} \) tunes \( V_{OFF} \). The implemented voltage sensor is illustrated in Figure 12 at transistor level. Each circuit section is explained in the following paragraphs.
Recalling subsection (III-C), the mean value of the reference generated by the 2T circuit, defined by $V_{REF}$, is mainly dependent on the transistors thresholds difference, namely $V_{thD} - V_{thC}$. Once that only high speed transistors are used, that term can only be sufficiently high when transistors of different channel types are applied. Thus, a PMOS is used as MD and an NMOS as MC, because the PMOS threshold is higher than the NMOS. This reference provides a stable $V_{REF} \approx 0.1 \, \text{V}$ for a supply $V_S > 0.2 \, \text{V}$.

By connecting the reference voltage to the inverter input, the transistor $M_1$ operates in the weak inversion region. Hence, the comparator output transition depends mainly on $M_2$ switching between the cut-off and strong inversion saturation region. The transition of the complete sensor output $P_{EN}$, depends on the transition of the sensing core. Therefore, $V_{TS}$ is used to define the supply $V_S$ required to make the sensing core output $V_O$ to switch voltage levels. According to the proposed design, $V_{TS} = 0.3 \, \text{V}$ and the sensing core current is below 1 nA.

In order to perform the $V_S$ to $V_{DC}$ conversion, a voltage level shifter based on cross coupled PMOS transistors $M_7 - M_8$ is used. Besides that main block, also one low voltage inverter ($M_3 - M_4$) is required to generate $V_S$, the logical opposite of $V_O$, and an output inverter ($M_9 - M_{10}$) to buffer the signal $P_{EN}$. The transistors used in the level shifter present low aspect ratios in order to reduce the current spikes that occur at the $V_{TR}$ transitions. The sensing core output transition, defined by $V_{TS}$, occurs at $V_S = 0.3 \, \text{V}$, and the voltage sensor has to activate $P_{EN}$ at $V_{DC} = V_{ON}$. Attending at Figure 12, the cross coupled PMOS transistors operate in the strong inversion and the NMOS $M_5$ and $M_6$ operate near the subthreshold region. Therefore, the aspect ratio of the NMOS is increased comparatively to the PMOS, so that the NMOS current drive capability can be sufficiently high to pull-down the $P_{EN}$ voltage node. However it is verified that when $V_O$ transits from zero to $V_S$ at $V_{TS}$, the low voltage $V_S$ is not high enough for the $P_{EN}$ pull-down to occur. In fact, the pull-down is only verified for $V_S = 0.32 \, \text{V}$. From $V_S=V_{TS}$ to $V_S = 0.32 \, \text{V}$, the cross coupled level shifter section establishes a direct current path, which compromises the power dissipation specification. Note that this effect is only verified for the $V_{ON}$ transition, because at $V_{OFF}$, the supply $V_{DC} = 0.4 \, \text{V}$.

In order to minimize the effect of the NMOS low current drive capability, the time period between the $V_{TS}$ transition and $V_S = 0.32 \, \text{V}$, has to be reduced. Once the current on the voltage sensing core stabilizes at approximately 0.9 nA when $V_S = V_{TS}$. Furthermore, the current on the low voltage inverter of the level shifter ($M_3 - M_4$) decreases from 0.25 nA to 0.5 pA, at the referred transition. Thus, it can be verified that the current on the low voltage circuit, which is defined by $I_{LV}$ and identified in Figure 12, becomes lower and stable after $V_S = V_{TS}$. As a consequence, the load imposed by the low voltage circuit, which is defined as $R_{LV} = V_S/I_{LV}$, increases after $V_S = V_{TS}$. Once the $R_D$ resistor is not used on the voltage divider, the voltage $V_S$ presents a faster rise after the transition at $V_{TS}$. This causes the reduction of the time period between the $V_{TS}$ transition and $V_S = 0.32 \, \text{V}$.

Besides depending on the $R_{U0}, R_{U1}$ resistances, the configuration of the load activation ($V_{ON}$) and deactivation ($V_{OFF}$) is based on the $R_{LV}$ resistance at the sensing core transition. When $V_S = V_{TS}$ the $R_{LV}$ value is defined as $R_{TS} \approx 300 \, \text{M} \Omega$. Bearing that $V_{ON} = 1.2 \, \text{V}$, $V_{OFF} = 0.4 \, \text{V}$ and $V_{TS} = 0.3 \, \text{V}$, the division ratio for the load activation must be

$$
\alpha_0 = \frac{V_{TS}}{V_{ON}} = \frac{R_{TS}}{R_{TS} + R_{U0}} = 1/4 \tag{6}
$$

and for the deactivation

$$
\alpha_1 = \frac{V_{TS}}{V_{OFF}} = \frac{R_{TS}}{R_{TS} + R_{U1}} = 3/4. \tag{7}
$$

Thus the up resistance values have to be $R_{U0} \approx 1 \, \text{G} \Omega$ and $R_{U1} \approx 100 \, \text{M} \Omega$. When the circuit is simulated with ideal $R_{U0}$ and $R_{U1}$ resistances, the voltage sensor current $I_{VS}$, harvester output $V_{DC}$ and $V_S$ behave as depicted in Figure 13. The load is activated at $V_{DC} = 1.28 \, \text{V}$ and deactivated at $V_{DC} = 0.38 \, \text{V}$. To impose the intermittent operation $I_S = 1 \, \mu \text{A}$ and $R_L = 0.3 \, \text{M} \Omega$.

When using ideal resistors $R_{U0}$ and $R_{U1}$ in the voltage divider, their resistance does not change with temperature. Nonetheless the current increase with temperature, reported in subsection III-A, affects the division ratios $\alpha_0$ and $\alpha_1$ through $R_{TS}$. The load imposed by the voltage sensing core at the transition moment ($R_{TS}$), decreases with temperature, due to the current increase. Furthermore, the sensing core transition voltage, defined as $V_{TS}$, increases with temperature. In order to verify those influences on the $V_{ON}$ and $V_{OFF}$ transitions, the generic voltage sensor transition voltage, defined by $V_{TR}$ is analysed. Once $V_{TR}$ is given by

$$
V_{TR} = \left(\frac{R_U}{R_{TS}} + 1\right)V_{TS}, \tag{8}
$$

the transition voltages rise significantly with temperature, considering the $V_{TS}$ positive temperature dependence and the denominator $R_{TS}$ negative temperature dependence. Therefore, a negative temperature dependence has to be introduced in $R_U$ so that both $V_{TS}$ and $R_{TS}$ influences can be overcome.

In order to compensate the temperature effect on $V_{TR} (V_{ON}$ and $V_{OFF})$, resistors based on diode connected MOS strings are proposed, Figure 12. This approach is based on the voltage dividers of [20]. According to [21], the gate to source voltage

![Fig. 13. Passive system supply $V_{DC}$, sensed voltage $V_S$ and voltage sensor current $I_{VS}$ for an intermittent system operation with $I_S = 1 \, \mu \text{A}$ and $R_L = 0.3 \, \text{M} \Omega$.](image-url)
of a diode connected MOS varies in temperature according to its drain current. For this implementation, the current will be imposed by the sensing core, and its effect on the MOS string is influenced by three parameters: the transistors type, the number of transistors ($N_U$) and also their aspect ratio ($W/L$).

Considering the nominal temperature case, $R_{U0} = 1 \, \text{G}\Omega$ and $R_{U1} = 100 \, \text{M}\Omega$, a subthreshold biasing is required at the transition time so that the MOS strings can generate such high resistance values. Once the PMOS overdrive voltage has to be lower than zero to impose a subthreshold biasing, the minimum number of transistors, defined by $N_U$, is 5 for $R_{U0}$ and 1 for $R_{U1}$. It is verified that the transistors aspect ratio and the number of transistors used, have different influences on the $V_{TR}$ temperature dependence. By optimizing the circuit through simulation, it is verified that the best temperature compensation is achieved for $R_{U0}$ with $N_U = 6$ and $R_{U1}$ with $N_U = 1$. Attending at Figures 14 and 15, it can be perceived that the voltage sensor transitions occur inside the defined $\pm 10\%$ tolerance. In fact, the $V_{ON}$ variation is $\pm 2.75\%$ for and the $V_{OFF}$ variation is $\pm 2.86\%$. Both the average power dissipated and the peak current defined by are below the specifications imposed, $10 \, \text{nW}$ and $1 \, \mu\text{A}$, respectively. Furthermore, the voltage sensor steady state current at $1.2 \, \text{V}$ is $1 \, \text{nA}$.

C. Voltage Limiter

In this section, the second part of the developed PCU is reviewed, following a similar analysis to the previous section. The block proposed to perform the voltage limiting is based on the high level circuit presented in Figure 16. This uses the same voltage sensing method as the voltage sensor, but without hysteresis. To create the discharge current $I_{\text{disc}}$ mentioned in the voltage limiters review (section II-C), a low impedance path is established by $M_{\text{disc}}$. To successfully control $I_{\text{disc}}$, a CMOS inverter is used to amplify $V_O$. Power down switches controlled by $P_{\text{EN}}$ are included in the design to block the limiter operation and the current flow while the load is not active.

The complete voltage limiter schematic is shown in Figure 17, where the up resistor $R_{UL}$ is implemented by a MOS string to compensate the temperature effect. The voltage sensing core uses the same circuit as the voltage sensor. The discharge control part uses the $M_3 - M_4$ inverter as an amplifier to control the discharge current $I_{\text{disc}}$ through $V_{\text{disc}}$. Transistors $M_{S1} - M_{S2}$ are the power down switches. The $P_{\text{EN}}$ transition from $V_{DC}$ to zero activates the limiter voltage sensing function. When $V_{DC} = V_{\text{Lim}}$, $V_O$ transits from zero to $V_S$, which decreases $V_{\text{disc}}$. The consequent $I_{\text{disc}}$ rise forces $V_{DC}$ to reduce. Thus a feedback loop based on the voltage supply is verified. Once the voltage limiter is sensing $V_{DC}$ when the load active, it is important that the
leakage current on the limiter does not compromise the power dissipation specification. Figure 18 displays the $V_{DC}$, $V_S$, $V_{disc}$ and $I_{disc}$ plots when a voltage limiting operation is imposed ($R_L = 0.3 \, \text{M} \Omega$, $I_S = 10 \, \mu\text{A}$) and $R_{UL}$ is ideal. Attending at those results, $V_{Lim}$ is close to 1.5 V and $V_{DC}$ stabilizes in the acceptable range by making $I_{disc} = 4 \, \mu\text{A}$. However, it can be verified by $V_{disc}$, that the limiter response is started at $V_{DC} = 1.4 \, \text{V}$ and the system presents a transient response caused by the feedback loop. This factor is mainly limited by the sensing core long response time, which causes a $V_{DC}$ propagation delay through $V_O$. Furthermore, $V_{Lim}$ is different from $V_{DC} = 1.4 \, \text{V}$, because the sensing core output at $V_S = V_{TS}$ is not sufficiently high to reduce $V_{DC}$. Thus, $I_{disc}$ must be activated for the lowest $V_{DC}$ value that makes $V_{Lim}$ to be contained inside the acceptable range. When $R_{UL}$ is replaced by the MOS string to compensate the temperature effect, the maximum $V_{DC}$ achieved, which is $V_{Lim}$, and the voltage where $V_{DC}$ stabilizes, defined as final $V_{DC}$, are presented in Figure IV-C. $R_{UL}$ is made by 8 PMOS transistors and the voltage limiting is imposed for the same conditions used on Figure 18. Attending at the plots of Figure IV-C, it is confirmed that both the maximum $V_{DC}$ ($V_{Lim}$) and final $V_{DC}$ satisfy the $\pm 10\%$ tolerance imposed. In fact, the $V_{Lim}$ tolerance to the temperature is $\pm 4.5\%$.

D. Layout and Final Results

When the voltage sensor and limiter blocks are connected as displayed in Figure 9, the specifications achieved are not significantly affected when compared to those obtained for the separate blocks simulations. The most affected is the power dissipated during the intermittent operation, due to contribution of the voltage limiter current. The PCU steady state current becomes 2 nA. The layout of the proposed PCU
with pads is presented in Figure 20, which occupies an area of 32310 μm². If pads are not included, the area is only 1215 μm². Besides V_{DC}, ground and P_{EN}, also a P_EN pad is included for testing purposes.

The results obtained by simulating the extracted circuit for MOS process corners and temperature range (−25°C to 90°C) are presented in Table I. Once it is a temperature sweep, the mean (μ) and (Δ) variation are indicated for each transition voltage. For \( P_{av} \) and \( I_p \) only the maximum values are presented. As it can be verified, the specifications are not met for all the corners, therefore the research goals are not met. In fact, a variation as high as ±55% is verified for the transition voltages \( V_{ON}, V_{OFF} \) and \( V_{Llim} \), considering all the process corners. That is due to a shift in the mean value of the sensing core transition voltage \( V_{TS} \) for mixed corners.

Table II, compares the specifications achieved to the state-of-the-art PCUs literature. Analysing the presented results, the maximum current achieved by the circuit in nominal conditions is below the other results. However, the proposed PCU does not include a regulator, which would impose a higher current on the discharge phase, as happens on [7]. Compared to state-of-the-art voltage sensors [11], [12], which present a ±4.8% precision to process corners on a temperature range from −40°C to 105°C, the tolerance achieved by this work (±55%) is inferior. However, the current required in this work is 2 nA and in the state-of-the-art is 6.8 nA.

Table III compares the specifications achieved for the most probable process variation event (yielded by Monte Carlo) with those proposed in the research goals. The average power is below the target and the worst transition precision can reach ±17%, which does not meet the target. However it is verified that 88% of the circuits present a tolerance below or equal to ±10%. The remaining specifications do not satisfy the initial targets.

![Fig. 20. Layout implementation of the proposed PCU with pads.](image)

### TABLE I

Comparison of the achieved specifications and target specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target</th>
<th>Achieved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition Tolerance</td>
<td>±10%</td>
<td>±17%</td>
</tr>
<tr>
<td>Average Power</td>
<td>10 nW</td>
<td>6.2 nW</td>
</tr>
<tr>
<td>Peak Current</td>
<td>1 μA</td>
<td>1.2 μA</td>
</tr>
<tr>
<td>Temp. Range</td>
<td>[−40 100] °C</td>
<td>[−25 90] °C</td>
</tr>
</tbody>
</table>

### TABLE II

Results obtained for post-layout simulations on MOS process corners and −25 to 90°C range.

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>( V_{ON} ) (μ ± Δ) [V]</th>
<th>( V_{OFF} ) (μ ± Δ) [V]</th>
<th>( P_{av} ) [nW]</th>
<th>( I_p ) [μA]</th>
<th>( V_{Llim} ) (μ ± Δ) [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical</td>
<td>1.167 ± 0.032</td>
<td>0.396 ± 0.012</td>
<td>5.8</td>
<td>0.92</td>
<td>1.5 ± 0.05</td>
</tr>
<tr>
<td>SS</td>
<td>1.188 ± 0.104</td>
<td>0.405 ± 0.012</td>
<td>10.1</td>
<td>0.88</td>
<td>1.498 ± 0.19</td>
</tr>
<tr>
<td>SNFP</td>
<td>0.655 ± 0.061</td>
<td>–</td>
<td>0.92</td>
<td>0.2</td>
<td>0.863 ± 0.109</td>
</tr>
<tr>
<td>FF</td>
<td>1.174 ± 0.08</td>
<td>0.396 ± 0.032</td>
<td>13.76</td>
<td>1.2</td>
<td>1.546 ± 0.094</td>
</tr>
<tr>
<td>FSNP</td>
<td>1.755 ± 0.071</td>
<td>0.013 ± 0.028</td>
<td>14.1</td>
<td>2.4</td>
<td>2.18 ± 0.068</td>
</tr>
<tr>
<td>Target</td>
<td>[1.08; 1.32]</td>
<td>[0.36; 0.44]</td>
<td>&lt; 10</td>
<td>&lt; 1.3</td>
<td>[1.35; 1.66]</td>
</tr>
</tbody>
</table>
V. Conclusions

This work proposes the design of a PCU implementable on passive systems based on low power external energy sources. In order to verify the role of a PCU in a system composed by an energy harvester and a load circuit, known as a passive system, a study of its high level model is proposed. This allows the characterization of three different system operations: intermittent, continuous and voltage limiting, which is a special case of the continuous. The intermittent case proves to be more advantageous for low power operations, once it requires the lowest input power. The voltage limiting is the extreme operation mode, where the PCU must limit the power delivered to the load, so that it is not damaged.

In this work, a voltage sensor is needed to apply the intermittent operation and a voltage limiter for the limiting operation. The circuits are designed in the UMC 130 nm technology with high speed transistors only. The load is activated at 1.2 V ($V_{ON}$), deactivated at 0.4 V ($V_{OFF}$) and its supply cannot surpass the 1.5 V ($V_{Lim}$). The voltage sensor relies on a voltage sensing core circuit based on subthreshold biasing to achieve a low power dissipation, required for the passive system to be power efficient. The core combines a CMOS inverter connected to a modified 2T reference circuit. To provide the sensing core supply voltage and the hysteresis sensor behaviour, two voltage dividers are used. Those are based on the resistance implemented by a string of diode connected MOS and the sensing core equivalent resistance. By applying the correct number of MOS and aspect ratio, the $V_{ON}$, $V_{OFF}$ and $V_{Lim}$ transitions are temperature compensated, yielding a maximum tolerance of ±10%. Due to the sensing core slow response, Monte Carlo analysis prove that the circuit performance is severely dependent on the voltage supply charge and discharge rates. The final circuit is implemented at layout level and it is verified that the specifications achieved do not meet those initially imposed. That is mainly due to the sensing core circuit high sensitivity to mixed process corners, which leads to a ±55% tolerance on the transition voltages. However the PCU power dissipation (6.2 μW) is still below the power provided by state-of-the-art harvesters (1 μW). Considering the transition voltages ±10% tolerance, an 88% yield is verified for Monte Carlo process and temperature variations. Thus, the circuit only does not achieve the target specifications for process corners.

REFERENCES


