Low-Noise Resistive Sensing Interface for Integrated Eddy Current Based Non-Destructive Testing System

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Abstract

A pseudo-resistor implementation with a bootstrapping technique is proposed. The pseudo-resistor is used to implement a controllable resistor on the feedback of a high-pass amplifier, that presents a low set-up time. This high-pass amplifier is implemented on a Non-Destructive Testing system.

Magnetoresistive sensors are resistive sensors that present a variation of the electrical resistance as a function of the magnetic field. These sensors are used in many applications, from biomedical analysis to industrial applications, such as Non-Destructive Testing based on eddy currents evaluation. Generally, eddy currents Non-Destructive Testing systems use an emitter that creates an alternating current which generates an alternating magnetic field around the emitter, and a pickup receiver to detect the magnetic field.

The target Non-Destructive Testing system is used for reading an array of magnetoresistive sensors to detect flaws and defects of materials, which have their magnetic field frequency in the range [100 Hz ; 10 MHz]. The depth of penetration analysed depends on the magnetic field frequency. The pseudo-resistor resistance can be varied between $k\Omega$ and $G\Omega$ by changing the $V_{SG}$ voltage of the PMOS transistors that comprise the pseudo-resistor, which can be used to vary the cut-off frequency of the high-pass filter between Hz and MHz, accordingly to the material under test. To reduce the set-up time between each magnetoresistive sensor reading, the pseudo-resistor resistance is switched to a resistance in the order of $k\Omega$, resulting in a set-up time equal to $0.3 \mu s$. This circuit is designed in $0.35 \mu m$ AMS technology.

Keywords

pseudo-resistor, controllable resistor, high-pass amplifier, set-up time, variable bandwidth, non destructive testing
Resumo

Uma implementação de uma pseudo-resistência com uma técnica de bootstrapping é proposta. A pseudo-resistência é usada para implementar uma resistência controlável no feedback de um amplificador passa-alto com tempo de set-up baixo. O amplificador passa-alto é implementado num sistema de Ensaio Não Destrutivo.

Os sensores magnetoresistivos são sensores resitivos em que a sua resistência varia com o campo magnético. Estes sensores são usados em diversas aplicações, como análises biomédicas ou aplicações industriais, tais como ensaios não destrutivos baseados na avaliação de correntes induzidas. Geralmente, os sistemas de ensaios não destrutivos baseados nas correntes induzidas utilizam um emissor, onde uma corrente alternada gera um campo magnético à volta do mesmo, e um receptor que detecta o campo magnético.

O sistema de Ensaio Não Destrutivo em estudo é utilizado para a leitura de sensores magnetoresistivos para detectar falhas e defeitos em materiais, que apresentam frequência de campo magnético entre 100 Hz e 10 MHz. A profundidade de penetração analisada depende dessa frequência. É possível variar a resistência da pseudo-resistência entre kΩ e GΩ, alterando a tensão $V_{SG}$ dos transistores PMOS utilizados na implementação da pseudo-resistência, o que pode ser utilizado para varia a frequência de corte do filtro passa-alto entre Hz e MHz, de acordo com o material testado. De forma a reduzir o tempo de set-up entre cada leitura dos sensores magnetoresistivos, a resistência é alterada para uma resistência na ordem dos kΩ, resultando num tempo de set-up de 0.3 μs. O circuito foi projectado na tecnologia 0.35 μm AMS.

Palavras Chave

pseudo-resistência, resistência controlável, amplificador passa-alto, tempo de set-up, largura de banda variável, ensaio não destructivo
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<th>Acronym</th>
<th>Description</th>
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<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application-Specific Integrated Circuit</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EC</td>
<td>Eddy Currents</td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
</tr>
<tr>
<td>HP</td>
<td>High-Pass</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MR</td>
<td>Magnetoresistive</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>NDT</td>
<td>Non-Destructive Testing</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-type Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-type Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
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In this chapter, a general overview of Magnetoresistive (MR) sensors and Non-Destructive Testing (NDT) is presented, in order to introduce the work that will be done throughout this thesis. A system for reading MR sensors is presented and explained, which is the starting point of our work. The object of study of this thesis is disclosed. In section 1.2 the objectives are listed and, in section 1.4 an outline of this thesis is described.

1.1 Motivation

MR sensors are resistive sensors that present variation on the electrical resistance as a function of the magnetic field. They are used in a wide range of areas from biomedical analysis systems to industrial applications, such as NDT based on Eddy Currents (EC) evaluation. In NDT based on EC evaluation, an advantage of using MR sensors is their higher Signal-to-Noise Ratio (SNR) compared with common coil-based probes [1].

NDT is a set of techniques used to characterize and detect defects and flaws on certain materials, without changing their characteristics and utility. These techniques can be applied to reduce the cost of operation, increase the safety of use and ensure the reliability of industrial components. NDT found its usage on aerospace, power generation, automotive, railway and petrochemical applications, avoiding air-plane crashes, nuclear disasters, traffic accidents, derailments, oil spills. There are several NDT methods, relying on different physical principles:

- Ultra-sonic;
- EC evaluation;
- X-radiography;
- Magnetic particles inspection;
- Dye penetrant/biological application.

The choice of the NDT method depends on several factors: safety, cost and efficiency. For our purpose, the NDT method used is EC evaluation, since it is the preferred NDT method for superficial and internal flaws detection on conductive materials [2]. EC evaluation is based on Electromagnetic (EM) induction and analysis of electrical currents on conductive materials and is used for:

- Thickness measurement;
- Corrosion evaluation;
- Electrical conductivity measurement;
- Magnetic permeability measurement;
- Flaw detection.
One advantage of EC evaluation is that it requires minimal surface preparation. EC evaluation is an intuitive method. There are different EC probes, aiming different evaluation purposes.

Most of the EC NDT systems use an emitter, where an alternating current generates an alternating magnetic field on its surroundings, and a pickup receiver to sense the magnetic field, as shown in Figure 1.1. When the emitter is close to the metal surface under test an EC is induced in the metal due to EM induction. Internal differences in conductivity result in differences in the surface magnetic field, which can be used to characterize internal integrity.

![EC NDT System](image)

Figure 1.1: EC NDT System [3].

The depth of penetration to be analysed depends on the magnetic field frequency, the material electrical conductivity and the magnetic permeability. The depth of penetration is described by:

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \mu_r \sigma}}$$

(1.1)

where:

- $f$ - Frequency of the magnetic field;
- $\mu_0$ - Magnetic permeability of air;
- $\mu$ - Magnetic permeability of the material;
- $\sigma$ - Electrical conductivity of the material.

By inspecting (1.1), it is easy to conclude that the depth of penetration varies inversely with frequency. Figure 1.2 shows penetration depth of the EM field for different materials. For the materials that we are concerned, magnetic field frequency is in the range [100 Hz, 10 MHz].

In [4], a system for reading MR sensors is presented. This system has the main objective of detecting defects of conductive materials under test while not compromising it. The system architecture is divided into two main elements: the Emitter System and the Receiver System. The Emitter System comprises an Emitter Coil and a driving generator at a frequency $f_1$ (frequency of the magnetic signal). The Receiver System contains a Sensor Array, an Application-Specific Integrated Circuit (ASIC) that drives the sensors with a frequency $f_2$, and some interface circuits. The purpose of the Sensor Array is to
acquire the signals produced by the currents induced by the Emitter Coil. The interface circuits generate an analogue output and digital synchronization signals.

Although this system is already implemented, there are some aspects with room for improvement, including the way the sensors are biased and switched and the type of amplification employed. This work is focused on an Operational Transconductance Amplifier (OTA). This amplifier (Pre-amp) is implemented in the ASIC as part of the NDT system receiver. This amplifier is preceded by a first-order RC High-Pass (HP) filter. This HP filter has to present a cut-off frequency of at least 50 Hz, since the frequencies of interest are in the range [100 Hz, 10 MHz]. The set-up time has to be the minimum possible, in order to switch between sensors with minimum time overhead.

The main challenge is to have a low resistance, during the set-up time, and a very high resistance during steady-state operation to guarantee that the HP filter cut-off frequency is at the desired frequency, with the same resistor implementation. This can be achieved with a controllable resistor.

### 1.2 Objectives

The main goal is to design a HP filter with a low set-up time. A variable resistor and its required circuit sub-blocks are implemented within the HP filter, achieving two main objectives:

- HP filter cut-off frequency equal to 50 Hz;
- Set-up time on the order of 0.1-1 \( \mu \text{s} \).

A variable resistor can be implemented with one or several Metal-Oxide-Semiconductor (MOS) transistors, which is known as a pseudo-resistor. A pseudo-resistor implementation is a solution that guarantees that our objectives are achievable, since it can be controlled to present a high or low resistance.
Therefore, our work will be focused on implementing a pseudo-resistor to be used on the feedback of the amplifier Pre-amp.

1.3 Main contributions

The innovation of this work is the implementation of a resistor that changes its value according to a clock signal, using a voltage to control its resistance. The voltage used to change the resistance is provided by a Digital-to-Analog Converter (DAC) and a complementary circuit is also used, which is inspired in a bootstrapping technique. This work, combined with that presented in [5], lead to two publications on international conferences:


1.4 Outline

This thesis is organized as follows. In chapter 2 the theory concerning resistive sensors and ways of reading resistive sensors are presented. The ASIC that is part of the NDT system is described. The topics in which this work is focused are noted (HP filter cut-off frequency and set-up time). Resistor implementations based on MOS transistors are presented. Finally, some considerations about an amplifier with a Folded-Cascode topology are made. In chapter 3 a pseudo-resistor implementation that uses the bootstrapping technique and a 6-bit output voltage DAC is proposed. Its implementation on the full system ASIC is described and explained. In chapter 4 time-domain simulations with Direct Current (DC) and Alternating Current (AC) inputs are shown, in order to evaluate the pseudo-resistor performance on the ASIC. Also, the layouts of the circuit components developed in this thesis are presented. In chapter 5 conclusions regarding the developed work and the results obtained are disclosed. Finally, a section with suggestions for future work is presented.
2 Related Work

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In section 2.1, two basic structures for readout of resistive sensors are presented: a current source biasing a bare sensor and the Wheatstone Bridge. These circuits are the basis for the sensor interface design used in the target NDT system. An alternative topology for reading variations of resistive sensors is presented, in order to overcome the trade-off between resolution and power consumption in the Wheatstone Bridge architecture. In section 2.2, the ASIC that drives the sensors present in the target NDT system is presented. Also, two sections are used to present details of the main objectives of this work and which techniques and circuits can be implemented to achieve those objectives. In section 2.3, several variable resistor implementations are presented. Several implementations and techniques to reduce the set-up time are explored. Finally, in section 2.4, we present considerations about flicker noise in the OTA and give guidelines for flicker attenuation, aiming to reduce its impact on the system.

### 2.1 Resistive Sensors Interface

In the system presented in section 1.1, the way for reading MR sensors has the advantage of low noise overhead to the system. The MR sensors reading procedure in our system is based on two simple ways for reading resistive sensors: the Wheatstone Bridge and the bare sensor with a current source.

The Wheatstone Bridge is the most common architecture to read the variations of resistive sensors [6], which is shown in Figure 2.1a. However, this architecture has an issue: the trade-off between resolution and power consumption. A different way to read resistive sensors is using a bare sensor and a current source (see Figure 2.1b).

![Figure 2.1: Basic biasing of a resistive sensor.](image)

A topology to solve the trade-off between resolution and power consumption on the Wheatstone Bridge is presented in [6], which combines the principal of the Wheatstone Bridge with the principle of the bare sensor with a current source. The “Active bridge” topology is based on a common gate configuration of a transistor, which is shown in Figure 2.2. The “Active bridge” topology has the principle of using a single current for both sensors bias and signal amplification, which is an advantage in terms of power consumption.
The “Active bridge” topology acts as an amplifier \( A_v = g_{m} R_L \), hence a small variation of the voltage across the sensor translates in a larger variation of the output voltage \( [6] \). The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) \( T_1 \) is the main noise source of the circuit. However, if \( T_1 \) is sized properly, it adds less noise than the resistor \( R_{BRIDGE} \) present in the “active bridge” topology. The SNR and the power consumption of the “active bridge” topology are approximately the same of a bare sensor. However, the “active bridge” topology has an output voltage of at least two orders of magnitude higher when compared with a bare sensor. Comparing the “active bridge” topology to the Wheatstone Bridge, it is possible to achieve a better current consumption in the “active bridge” topology (about one order of magnitude lower), without SNR degradation.

Two ways of implementing the current source of the “active bridge” are presented in Figure 2.3. In Figure 2.3a, it is possible to visualize an implementation with an N-type Metal-Oxide-Semiconductor (NMOS) transistor biased in the active region. In Figure 2.3b, it is presented a different implementation, which uses an NMOS transistor and a resistor. The difference between those implementations is the impact introduced by the resistor \( R_{NI} \). In the implementation presented in Figure 2.3a the impact of the noise introduced by the transistor \( T_2 \) is lower than in the implementation presented in Figure 2.3b. The resistor \( R_{NI} \) allows that the current noise introduced by \( T_2 \) flows into it, creating a feedback loop on \( V_{GST2} \) \( [6] \).

A differential topology is presented (see Figure 2.4a), in order to combine the “active bridge principle” and robustness (good immunity to environmental disturbances). However, the differential “active bridge” topology has a high gain. Therefore, any small variation of \( R_{BRIDGE} \) can put \( T_1 \) or \( T_2 \) into triode region, harming the amplification. In order to ensure the realization of the amplification, an offset cancellation method is introduced in \( [6] \). This method is based on a digitally controlled feedback trimmer realized with a resistor ladder, which is presented in Figure 2.4b.
2.2 Application-Specific Integrated Circuit for Reading a Magnetoresistive Sensor Array for Non-Destructive Testing

In [4], the [ASIC] implemented in the NDT system receiver is presented. The [ASIC] drives the sensors and has 8 sensors per amplifier and 4 blocks for a 32-sensor array (see Figure 2.5). The number of sensors can be scaled. The [ASIC] has the following functions: drive the magnetic sensors; multiplex the signals, amplify/filter the signals and cancel the electrical sensor drive signal. The [ASIC] allows [DC, AC] current input signals. Each sensor is followed by a band-pass preamplifier (centered on $f_1$, $f_3 = f_1 - f_2$ or $f_4 = f_1 + f_2$) with bandwidth $f_b$. The [DC] and the $f_2$ components have to be filtered at the output, since they do not hold information on the sensor resistance value.
The ASIC specifications are:

- Drive the sensor with the maximum possible amplitude;
- Drive the sensor with frequencies from 100 Hz to 10 MHz;
- Amplify the magnetic signal, by at least 30 dB;
- Remove the electric signal;
- Have noise (power spectral density) lower than 100 nV/√Hz.
In Figure 2.6, the simplified circuit of each block of the ASIC is presented. As explained before, the focus of this work is the amplifier Pre-amp and the HP filter at its input. In Figure 2.7, the HP filter and the feedback circuit of the amplifier Pre-amp can be visualized, which is the part of the circuit that is the core of our work.

![Simplified circuit of HP filter and Pre-amp.](image)

2.2.1 High-Pass Filter Cut-off Frequency

The HP filter that precedes the amplifier Pre-amp is a first-order RC filter. The amplitude of the signal at the input of the HP filter is low. Therefore, an active filter or a filter with higher complexity are not necessary to implement the HP filter. The pole of the HP filter has to be located at a very low frequency (50 Hz). Two of the solutions to define the pole frequency at the desired value are: a nF capacitor or a resistor that is in the MΩ range or higher. A nF capacitor and a resistor that is in the MΩ range or higher can be implemented externally. Nevertheless, a resistor that is in the MΩ range or higher can be implemented using one or several MOS transistors. This implementation is known as a pseudo-resistor, allowing to have a resistor that meets our specifications integrated on-chip. Since we are interested in integrating our solution on-chip, the solution chosen to implement the HP filter resistor is a pseudo-resistor. By using a pseudo-resistor on the feedback of the amplifier Pre-amp is also possible to maintain a stable DC operating point of the OTA [7]. The capacitor of the HP filter has a capacitance of 10 pF.

2.2.2 Set-up Time

The set-up time is an aspect that has a particular focus in this thesis, since our main goal is to implement an amplifier with a low set-up time. The set-up time of the HP filter is pointed to be in the range 0.1-1 µs, which is a demanding specification. This difficulty is caused by the value of the resistance needed for the resistor that is part of the HP filter to fulfil the two main objectives of this work. The value of the resistance has to be around 320 MΩ or higher to have the pole of the HP filter at a frequency lower than 50 Hz, which increases the set-up time. To have a set-up time in the order of 0.1-1 µs, it is necessary a resistance between 1.5 kΩ and 15 kΩ. Therefore, it is possible to conclude that two
significantly different resistances are needed to accomplish the specifications of the pole frequency and the set-up time. Analysing the equations that give the set-up time and the cut-off frequency, it is possible to conclude that the set-up time and the cut-off frequency have a different relation with the resistance. The set-up time equation gives the amount of time required for the system to reach 99.9% of its final value.

\[ t_{\text{set-up}} = 6.9RC \quad ; \quad f_{\text{cut-off}} = \frac{1}{2\pi RC} \]  

(2.1)

Therefore, the resistor has to be carefully designed and switched to guarantee the correct pole frequency, concerning at the same time the reduction of the set-up time.

In Table 2.1, the state-of-the-art of the settling time is presented. Applying fast settling techniques, it is possible to reduce the set-up time. Despite the set-up time reductions presented are not low enough compared with our objective, these techniques can be used as a starting point to create a technique to use in our circuit. Our objective is to have a set-up time between 0.1 µs and 1 µs.

Table 2.1: State-of-the-art of settling time.

<table>
<thead>
<tr>
<th></th>
<th>Fast-Settling Disabled</th>
<th>Fast-Settling Enabled</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Muhammad Awais Bin Altaf [8]</td>
<td>Several hours</td>
<td>0.5 seconds</td>
<td>90 nV/√Hz</td>
</tr>
<tr>
<td>Jiawei Xu [9]</td>
<td>Tens of seconds</td>
<td>1 second</td>
<td>60 nV/√Hz</td>
</tr>
<tr>
<td>Yongqiang Xiao [10]</td>
<td>-</td>
<td>18 µs</td>
<td>10 Hz to 100 kHz Empty Load: 36 nV/√Hz 1mA: 39.3 nV/√Hz Full Load: 39.4 nV/√Hz</td>
</tr>
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</table>

In [8], a fast-settling technique applied in a pseudo-resistor is presented. This technique consists in applying 0 V to the gate of a pseudo-resistor. In [9], a fast-settling path with a high transconductance is included in a DC servo-loop, which is temporarily switched on during the start-up to reduce the set-up time. In [10], a low-pass filter with a fast set-up module is proposed. This technique uses a transistor with a low resistance along with a constant charging current to provide a significant current to a transistor working as a capacitor, in order to reduce the set-up time of the low-pass filter output voltage.

### 2.3 Pseudo-resistors

A pseudo-resistor implementation using one or several MOS transistors working as switches can be used to implement a resistor. Taking advantage of the transistors operating regions and controlling their gate voltage with a DC voltage, it is possible to use a pseudo-resistor implementation to have a variable resistor. A variable resistor implementation is the main topic in this work, since with transistors in the triode region a low resistance is obtained, creating a low resistance path on the feedback of the amplifier, which is very important to achieve our main goal: implement a HP amplifier with a low set-up time. With transistors operating in sub-threshold region a high resistance is obtained, allowing also to vary the cut-off frequency of the HP filter accordingly to the material under test. This means that the pseudo-resistor can be tuned according to the wanted bandwidth.

Several pseudo-resistors implementations will now be presented, which are possible solutions to
implement the resistor of the HP filter mentioned in section 2.2. In Figure 2.8 it is shown a first implementation of a pseudo-resistor. This implementation, using two devices in series, presents a very high resistance, as shown in Figure 2.9.

![Figure 2.8: Implementation of a pseudo-resistor](image)

For $|\Delta V| < 0.2$ V, this pseudo-resistor implementation presents a considerably high incremental resistance, $r_{inc}$, with values higher than $10^{11}$ Ω. With the values of resistance measured, presented in [11], it is not possible to achieve a set-up time in the order of 0.1-1 μs, considering a 10 pF capacitor in the HP filter. For example, if we choose $R = 10^8$ Ω (value extracted from the graphic presented in Figure 2.9), it will result in $\tau = RC = 1$ millisecond. Therefore, a set-up time equal to 6.9 milliseconds is obtained, which is a higher value compared to the value that we want for our amplifier. Nevertheless, despite that the large resistance of this implementation provides a long time constant, a large voltage variation in the input causes a large voltage variation through the devices in series. Therefore, their incremental resistance decreases and presents a reduction in the settling time [11].

![Figure 2.9: Measured incremental resistance (pseudo-resistor of Figure 2.8)](image)

Another pseudo-resistor implementations having variable-$V_{GS}$ are shown in Figure 2.10a. These implementations are presented in [7], for the purpose of implementing a feedback resistor on a neural amplifier. The implementation A (same implementation shown in Figure 2.8) and the implementation C can not be tuned to the bandwidth, which is a disadvantage. The ability to be tuned to the bandwidth
can be an important aspect for our variable resistor, since it allows the HP filter cut-off frequency to be defined accordingly to the material under test. The implementation B has the ability to be tuned to the bandwidth, although this implementation suffers from non-linearity at high output swings, which can drift the DC biasing point if the resistance is too high [7].

![Diagram](image)

(a) Variable-$V_{GS}$ implementations. 
(b) Simulated resistance.

Figure 2.10: Pseudo-resistors with variable-$V_{GS}$ and simulation results.

These three implementations present approximately constant resistance for small output voltage swings of less than 200 mV, as shown in Figure 2.10b. If $V_{GS}$ is set too low, a large resistance is obtained. However, setting $V_{GS}$ too low can lead to variations on the current that flows through the pseudo-resistor implementations. Those variations can have a greater influence on a large resistance, since the current is too small.

Three pseudo-resistor implementations with fixed-$V_{GS}$ are presented in Figure 2.11a. In Figure 2.12, the simulation results show reasonably constant resistance over the large voltage swing for the implementation D. However, the implementations E and F present a stronger non-linear performance. In [7], the implementation D is chosen to implement a feedback resistor. To implement the voltage source to define $V_{GS}$ of both transistors, two source followers are used, as shown in Figure 2.11b. The source followers can provide a constant $V_{GS}$ on the sub-threshold feedback devices. The resistance changes accordingly to the bias current in the source followers, which allows a variation in the HP pole frequency. Increasing the bias current in the source follower the resistance is reduced, while reducing the bias current in the source follower the resistance is increased.

In order to evaluate the behaviour of the presented implementations in the NDT system, it is necessary to simulate and obtain the resistance under a most approximate situation of the target NDT system. Therefore, one of the nodes ($V_{OUT}$) of our resistor is fixed at 1.65 V and the other node ($V_{IN}$) is swept between 0 and 3.3 V. For each implementation, it is necessary to take into account a minimum transconductance, $g_{\text{min}}$, in order to prevent the nodes from floating if a device is turned completely off. If $g_{\text{min}}$ is too large, the accuracy can be affected, while if it is too small, the convergence can be affected. When a pseudo-resistor presents a large resistance, acting as an open circuit, the minimum transconductance value provides to the simulator a reference, in order to guarantee that at least an approximate result is presented. The simulations results for the variable-$V_{GS}$ implementations (A and C) are shown in Figure
2.11 while the simulations results for the implementation B are presented in Figure 2.15 for different $V_{tune}$ values between 0 and 1.65 V.

Figure 2.11: Pseudo-resistors with fixed-$V_{GS}$.

Figure 2.12: Simulated resistance for fixed-$V_{GS}$ implementations [7].

Figure 2.13: Simulation results with variable-$V_{GS}$ implementations A and C.
For the implementation A, it is used $g_{\text{min}} = 1 \times 10^{-13}$ S, since for smaller values the simulations presented a resistance that probably not corresponded to its real value. For the implementation B, it is used $g_{\text{min}} = 1 \times 10^{-14}$ S, for the same reason as the implementation A. Finally, for the implementation C, it is used $g_{\text{min}} = 1 \times 10^{-16}$ S. To show the influence of the minimum transconductance value on the resistance behaviour, a simulation result for the implementation C with a higher $g_{\text{min}}$ value is presented in Figure 2.14.

![Figure 2.14: Simulation results with variable-V$_{\text{GS}}$ implementation C with $g_{\text{min}} = 1 \times 10^{-12}$ S.](image)

A higher $g_{\text{min}}$ value establishes a limit to the pseudo-resistor implementation resistance. Therefore, it is necessary to take into account this value. When a $g_{\text{min}}$ value is set, it is possible to obtain an inaccurate result. For these simulations, the transistors that are part of the implementation C, which are P-type Metal-Oxide-Semiconductor (PMOS) transistors, have the bulk connected to the source. The transistors of the implementations A and B (NMOS transistors) have the bulk connected to ground. With these simulation results, it is possible to conclude that with these variable-V$_{\text{GS}}$ implementations high resistances are achievable, which is one of our main goals, in order to have a pole frequency at 50 Hz.

![Figure 2.15: Simulation results with variable-V$_{\text{GS}}$ implementation B.](image)

For the fixed-V$_{\text{GS}}$ implementations, the resistance is simulated with different values for the ideal
voltage sources (0.2 V, 0.4 V and 0.6 V, for example), in order to evaluate how the resistance varies with that voltage. That voltage defines the voltage between the gate and the source of the transistors. In Figure 2.16 the simulation results for the implementation D are presented. In Figure 2.17 the simulation results for the implementation E are presented. Finally, in Figure 2.18 the simulation results for the implementation F are shown.

Figure 2.16: Simulation results with fixed-\( V_{GS} \) implementation D.

For all the simulations, it is used a minimum transconductance of \( 1 \times 10^{-16} \) S. The PMOS transistors that comprises the fixed-\( V_{GS} \) implementations have the bulk connected to the supply voltage, while the NMOS transistors have the bulk connected to ground. With these simulations results, it is possible to conclude that with the fixed-\( V_{GS} \) implementations, it is also possible to have a pseudo-resistor that presents a resistance that is in the M\( \Omega \) range to have a cut-off frequency equal to 50 Hz. With that cut-off frequency, the MR sensors readings can be performed for the materials of interest, since they have the magnetic field frequency in the range \([100 \text{ Hz}, 10 \text{ MHz}]\). For \(|\Delta V| < 0.5 \text{ V}\), it is necessary that the pseudo-resistor resistance does not change to a value lower than 320 M\( \Omega \), in order to maintain the cut-off frequency at least below 50 Hz and not compromise the MR sensors readings.

An increase in \( V_{GS} \) (\( V_{SG} \) for the PMOS transistors) causes a decrease on the resistance, which can be an improvement to our objective of having a resistance of 320 M\( \Omega \) or higher. This improvement allows to adjust the bandwidth with resistances smaller than 320 M\( \Omega \) accordingly to the material under test, obtaining a variable bandwidth.

Concerning the set-up time, it is necessary that the pseudo-resistor implementation that presents high resistances can be changed to present a resistance between 1.5 k\( \Omega \) and 15 k\( \Omega \). This change allows to achieve the objective of having a set-up time between 0.1 \( \mu \)s and 1 \( \mu \)s with a unique pseudo-resistor implementation. In [8], a fast settling technique is proposed. This technique allows the control of a pseudo-resistor implemented with PMOS transistors to achieve a low set-up time. This technique connects the gate of transistors to ground, in order to enable the fast settling technique. In Figure 2.19 the pseudo-resistor implementation with a fast settling technique having measurement results is presented. However, a settling time of 1 second is obtained, which is still a high value compared with our objective. The objective is to design a proper pseudo-resistor implementation, in order to apply this fast settling technique and achieve a reduction of the set-up time to values in the order of 0.1-1 \( \mu \)s.
2.4 Operational Transconductance Amplifier Pre-amp

The main goal of this thesis is to design an amplifier with a low set-up time. This amplifier has a Folded-Cascode topology and has a HP filter at its input. An important specification for the ASIC is to have low-noise, in order not to impair the measurements taken with the probe. The source of the noise is mostly from the amplifier Pre-amp. Therefore, it has to be ensured that the noise from the amplifier Pre-
amp is the lowest possible, taking into account all the specifications that it has to accomplish, especially the bandwidth.

There are two types of noise in Complementary Metal-Oxide Semiconductor (CMOS) operational amplifiers: the flicker noise and the thermal noise. Usually, for frequencies lower than 1-10 kHz, the flicker noise component, that is proportional to 1/f, has a greater influence than the thermal noise component for typical bias conditions and device geometries [12].

The total current noise of a MOSFET is given by (equation valid for long channel devices):

\[
\frac{i_t^2}{\Delta f} = K_F g_m^2 \frac{C_{ox} W L f}{3} + 8K T g_m
\]

with:

\[
g_m^2 = 2\mu C_{ox} \frac{W}{L} I_D
\]

where:

- \(K_F\) - flicker noise coefficient;
- \(g_m\) - transconductance parameter of the MOSFET device;
- \(C_{ox}\) - gate oxide capacitance per unit area;
- \(W\) - channel width;
- \(L\) - channel length;
- \(f\) - frequency;
- \(\mu\) - effective mobility;
- \(I_D\) - drain current;
- \(\Delta f\) - bandwidth.

In (2.2), the first parcel of the sum corresponds to the flicker noise contribution and the second parcel corresponds to the thermal noise component. Always taking into account fabrication technology, generally, the PMOS transistors are used to reduce the flicker noise component, while the NMOS transistors are used to reduce the thermal noise component. Therefore, large size p-channel input transistors with high transconductance and long-channel transistors with small transconductance as active load normally are used to achieve a low-noise design. However, devices with large areas demand a careful design, taking into consideration the large parasitic capacitances. Higher parasitic capacitances imply higher power consumption, in order to maintain speed specifications.

As mentioned before, the amplifier Pre-amp has a Folded-Cascode topology, as represented in Figure 2.20. This amplifier topology could be a Telescopic topology or a Mirrored topology. The Mirrored OTA has the worst noise performance and the higher current consumption, while the Telescopic topology presents the best noise performance and the lower current consumption. The Folded-Cascode topology has a worst noise performance and a higher current consumption when compared with the Telescopic topology. However, the Folded-Cascode topology has only four transistors in the output rail. In [1], an analysis of the noise of the Folded-Cascode OTA is presented.
The input referred noise power of the Folded-Cascode [OTA] is given by:

\[
\frac{dV_{n^2}^2}{df} = 16K_BT \left( 1 + \frac{g_{m4,5}}{g_{m1,2}} + \frac{g_{m10,11}}{g_{m1,2}} \right)
\]

where:

- \(K_B\) - Boltzmann constant;
- \(T\) - Temperature in Kelvin;
- \(g_{m_i}\) - transconductance parameter of the MOSFET device.

By inspecting equation 2.4, it is possible to conclude that the transistors that have a greater influence to the input referred noise power of the Folded-Cascode OTA are: \(M_1\) and \(M_2\) (differential pair); \(M_4\) and \(M_5\) (current mirror); \(M_{10}\) and \(M_{11}\) (current mirror). The amplifier Pre-amp is already designed [3], with a particular focus on the output current, the bandwidth and the noise specifications.

![Folded-Cascode OTA](image)

**Figure 2.20: Folded-Cascode OTA**

### 2.5 Summary

This chapter described our work [HP] filter in the input of the amplifier Pre-amp) and the objectives that we pretend to accomplish: define the HP filter cut-off frequency at the desired value (50 Hz) and reduce the set-up time to a value between 0.1 \(\mu s\) and 1 \(\mu s\). A pseudo-resistor implementation is the solution chosen for the resistor that is part of the first-order RC [HP] filter. Several implementations of
pseudo-resistors were explored, in order to evaluate how the behaviour of the pseudo-resistor implementations can be used to achieve our objectives. Some circuits for reading variations of resistive sensors and a Folded-Cascode (amplifier Pre-amp) were presented.
Non-Destructive Testing System with Pseudo-resistor Implementation

Contents

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3.3 Summary .................................................................................... 39
In this chapter, the implementation of the block of the full system ASIC is presented. The pseudo-resistor to be used on the feedback of the amplifier Pre-amp and how it is implemented the control of the pseudo-resistor to switch its resistance are disclosed.

In section 3.1, a fixed-$V_{GS}$ pseudo-resistor with only PMOS transistors to implement the variable resistor of the HP filter is presented. Some simulations results are presented to show the advantages of this pseudo-resistor implementation. In 3.1.1, a circuit with a bootstrapping technique is proposed. This circuit is used to define the voltage between the source and the gate of the PMOS transistors of the pseudo-resistor. A 6-bit voltage divider DAC is used, in order to provide a voltage to the circuit with a bootstrapping technique. The DAC has a range between 0 V and 1.65 V, which means that the pole frequency can be varied accordingly to the material under test. In section 3.2, a single block diagram that is part of the full system ASIC is presented. The amplifier Pre-amp is implemented in this block, which is the HP amplifier that we are focused on this work. A description of the implementation of the pseudo-resistor on the amplifier feedback is presented. The pseudo-resistor is controlled to guarantee that the resistance is in the range of values that we need during steady-state operation and also during set-up time.

### 3.1 Pseudo-resistor Implementation

In order to choose a pseudo-resistor implementation, it is necessary to take into account some specifications that are necessary to accomplish our objectives for the HP filter cut-off frequency and the set-up time. In section 2.2, the pseudo-resistor resistance that has to be ensured is determined: $320 \, \text{M}\Omega$ to have a cut-off frequency of at least 50 Hz and a value between $1.5 \, \text{k}\Omega$ and $15 \, \text{k}\Omega$ to accomplish a set-up time of 0.1-1 $\mu$s. The behaviour of the pseudo-resistor around $|\Delta V| < 0.5$ V is critical, since voltage variations through the pseudo-resistor can occur. Therefore, it is necessary to guarantee that when the readings of the MR sensors take place the resistance does not change to a value lower than $320 \, \text{M}\Omega$, in order to not compromise the MR sensors readings.

Here, the behaviour of a fixed-$V_{GS}$ implementation with only PMOS transistors is evaluated. By using only PMOS transistors, the bulk terminal is available to connect to the source or to the supply voltage, which can be an advantage to minimize leakage currents. The leakage currents can have a significant influence in high resistances, since variations in the current can have a significant influence on the resistance. A fixed-$V_{GS}$ pseudo-resistor implementation, that is inspired in the fixed-$V_{GS}$ implementations presented in section 2.3 is proposed, which is shown in Figure 3.1.

![Figure 3.1: Fixed-$V_{SG}$ implementation with PMOS transistors.](image)
As with the other implementations, a simulation is performed to evaluate the behaviour of this pseudo-resistor under similar conditions of the target NDT system. One of the nodes \( V_{\text{OUT}} \) of our pseudo-resistor is fixed at 1.65 V and the other node \( V_{\text{IN}} \) is swept between 0 and 3.3 V. In this case, the bulk terminal of both PMOS transistors is connected to the supply voltage. A minimum transconductance of \( 1 \times 10^{-16} \) S is settled. In order to evaluate how the resistance behaves with the variation of the \( V_{SG} \) voltage, a simulation where the \( V_{SG} \) voltage is defined by a voltage source is performed. The simulation results with different \( V_{SG} \) values (0.5 V, 0.7 V and 0.9 V) for the PMOS transistors are presented in Figure 3.2.

![Figure 3.2: Simulation results with pseudo-resistor implemented with PMOS transistors (see Figure 3.1).](image)

The behaviour of the resistor is not exactly symmetric. However, a better resistance symmetry around \( \Delta V = 0 \) V by using devices in series can be achieved, as shown in Figure 3.3. By using devices in series, it is easier to guarantee that the pseudo-resistor resistance does not change to a value lower than 320 M\( \Omega \) for \( |\Delta V| < 0.5 \) V. By inspecting the resistance characteristic presented, it is possible to conclude that an increase of \( V_{SG} \) causes a decrease in the resistance. This feature represents an improvement to our main objective. By using this variation, the HP filter cut-off frequency can be changed accordingly to the material under test and its magnetic field frequency. Since the resistance decreases with the increase of \( V_{SG} \), it is possible to predict that a low resistance is achievable, if \( V_{SG} \) is equal to 1.65 V. In order to have \( V_{SG} = 1.65 \) V, it is easier to connect the gate of the PMOS transistors to ground, removing the ideal voltage source. The simulation results corresponding to a simulation performed with 0 V applied to the gate of PMOS transistors are shown in Figure 3.4.

With 0 V applied to the gate of the PMOS transistors, the resistance obtained is low, achieving values in the order of k\( \Omega \), which reduces the set-up time. However, the implementation with four PMOS transistors presents a resistance higher than what is desirable to theoretically reduce the set-up time to a value between 0.1 \( \mu \)s and 1 \( \mu \)s. Nevertheless, the difference is not significant. Therefore, the performance of the pseudo-resistor implementation under the conditions of the NDT system can accomplish the target specifications.

The implementation with four PMOS transistors can guarantee that the achieved equivalent resistance is, approximately, in the order of values that are needed. Therefore, this implementation is simulated in the target NDT system for evaluating its performance. In order to implement the pseudo-resistor
Resistance [Ω]

V\textsubscript{SG} = 0.5V
V\textsubscript{SG} = 0.7V
V\textsubscript{SG} = 0.9V

Figure 3.3: Simulation results with implementations (see Figure 3.1) in series.

Figure 3.4: Simulation results with 0 V applied to the gate of PMOS transistors.

in the NDT system, it is necessary to modify its topology. The ideal voltage sources have to be replaced for a circuit that is capable of generating a voltage variation between the source and the gate of the PMOS transistors that comprise the pseudo-resistor implementation. In section 2.3, it is presented a circuit to define the voltage between the source and the gate of transistors. This circuit is a source follower, which can vary the resistance accordingly to the bias current in the source follower. Therefore, it is necessary to analyze if a pseudo-resistor implementation with source followers can guarantee resistances in the orders that are needed. A simulation result for two different bias currents is presented in Figure 3.5.

As explained before, the resistance is reduced, increasing the bias current in the source follower. Reducing the bias current in the source follower, the resistance is increased. With the simulation result shown in Figure 3.5, it is possible to confirm that the resistance varies accordingly to the bias current, as supposed. However, the resistance variation does not fulfill our requirements, since with a bias current equal to 1 \( \mu \)A, which is a low value, a maximum resistance of 1.5 MΩ is obtained. This resistance value is not high enough to achieve a cut-off frequency of 50 Hz, which is an important specification for the
target NDT system. Therefore, it is necessary to explore a different solution to provide a variation in the voltage between the source and the gate of the PMOS transistors that guarantees resistances in the order of values that are needed.

### 3.1.1 Bootstrapping Technique

A boosted switch is presented in Figure 3.6, which uses a technique similar to the one presented in [13]. This circuit has 2 phases: in phase 1 (clk1 set to a logic level '1'), the capacitor C is charged to \( V_{DD} \) and the boosted switch is open (gate connected to ground); in phase 2 (clk1 set to a logic level '0'), the capacitor C is disconnected from the voltage supply and the bottom plate is referenced to \( v_i \), resulting in a switch gate voltage of \( V_{DD} + v_i \).

![Figure 3.6: Switch with bootstrapping technique.](image)

In more detail, the circuit works as follows: initially, the capacitor C is discharged and the clk1 signal is set to logic '1', turning on \( N_1 \) and connecting the node B to ground, while \( P_1 \) turns off (high impedance path between nodes A and B) and \( P_2 \) turns on and the capacitor C and the node A are charged to \( V_{DD} \); when the clk1 signal commutes to a logic '0', \( N_1 \) turns off and the inverter ties the bottom plate of the...
capacitor to \( v_i \), turning off \( P_2 \) and raising the node A to \( V_{DD} + v_i \), while \( P_1 \) is turned on and connects the node B to the node A.

In our pseudo-resistor implementation, we have an identical situation, since the PMOS transistors work as switches and it is necessary to define a voltage between the source and the gate of the transistors. Therefore, a circuit (see Figure 3.7) inspired in the circuit presented in [13] is proposed, changing the voltage that charges the capacitor to a voltage \( V_{TUNE} \). The bottom plate of the capacitor has to be referred to \( v_{cm} \), while the capacitor is charging, in order to have an equal \( V_{SG} \) for all the PMOS transistors. When the MR sensors readings take place, it is necessary that the bottom plate of the capacitor has to be connected to the source of the PMOS transistors that comprise the pseudo-resistor.

The proposed circuit works as follows: in phase 1, \( N_1 \) and \( N_2 \) turn on, the capacitor C is charged with \( V_{TUNE} - v_{cm} \), while the transmission gate creates a high impedance path between the nodes A and B (node B connected to ground); in phase 2, \( N_1 \) and \( N_2 \) turn off, while the transmission gate connects the node A to the node B, which allows that the voltage at the gate of the PMOS transistors of the pseudo-resistor is equal to the voltage \( V_{TUNE} \). In order to confirm that the circuit proposed works as described, a simulation result with different \( V_{TUNE} \) values is shown in Figure 3.8. The capacitor C has a capacitance of 10 pF, in order to guarantee that it is dominant in relation to the transistors capacitances and that the voltage charged remains constant for a longer period of time to allow the measurements to be taken.

The simulations results show that the proposed circuit with a bootstrapping technique works as de-
sired. Therefore, it is possible to use this circuit to replace the voltage sources between the source and the gate of the PMOS transistors that are part of the pseudo-resistor. With this circuit, it is possible to vary the resistance by changing $V_{TUNE}$ and, consequently, vary the pole frequency. Taking advantage of the node B being grounded in phase 1, this circuit can be used to connect the gate of the PMOS transistors to ground, in order to obtain a low resistance. As explained before, a low resistance allows to reduce the set-up time. By using only this circuit with a bootstrapping technique, resistances in the order of values that are needed can be obtained. Therefore, this circuit is essential to achieve our main goal of implementing a HP amplifier with a low set-up time.

### 3.1.2 Digital-to-Analog Converter

In order for the proposed circuit with a bootstrapping technique works as supposed, it is necessary to generate the voltage $V_{TUNE}$. Since the circuit to provide the voltage $V_{TUNE}$ is not an important topic in our work, our objective is to implement a simple circuit for this purpose. Therefore, our choice is to implement a DAC with a voltage divider architecture, as shown in Figure 3.9. This DAC architecture consists of $2^N$ equal value resistors followed by a matrix of switches and a voltage buffer. In this case, a 6-bit DAC with 1 kΩ resistors is used. This architecture uses a buffer, in order to have a low output impedance.

Our 6-bit voltage divider DAC has $2^6 = 64$ possible voltage outputs comprised between $V_{ref} = 1.65$ V and 0 V. This range allows having different orders of resistance, which means that the cut-off frequency can be adjusted according to the requirements of the material under test and its applications. Connecting the 6-bit DAC with the circuit with a bootstrapping technique, the node B voltage of the circuit with a bootstrapping technique is established by the codification of the DAC, as shown in Figure 3.10.

Finally, the pseudo-resistor can be implemented with the proposed circuit with a bootstrapping technique and the 6-bit output voltage DAC which are the circuits that replace the ideal voltage sources. The voltage provided by the DAC can be used to change the output voltage of the circuit with a bootstrapping technique, in order to vary the pseudo-resistor resistance. This variation represents an improvement to our first objective. By using this implementation, we can present a variable bandwidth, which is an ad-
vantage. The pole frequency can be defined accordingly to the magnetic field frequency of the material under test.

3.1.3 High-Pass Filter Resistor

With the circuit represented in Figure 3.7 and the 6-bit voltage divider DAC it is possible to have the final implementation of the pseudo-resistor, as represented in Figure 3.11.

The proposed pseudo-
resistor implementation has a circuit with a bootstrapping technique that defines $V_{SG}$ of the PMOS transistors. That voltage can be varied with the voltage provided by the 6-bit DAC between 0 V and 1.65 V, which is the $V_{TUNE}$ voltage (input of the circuit with a bootstrapping technique). When the capacitor $C$ of the circuit with a bootstrapping technique is charging, the node B voltage is grounded, allowing to have a resistance in the order of $k\Omega$, which allows to reduce the set-up time. The HP filter resistor is implemented with two equal devices in series. Therefore, in total are used four PMOS transistors and four equal circuits with a bootstrapping technique with a shared 6-bit DAC to generate the voltage $V_{TUNE}$.

![Figure 3.11: Pseudo-resistor implementation with a bootstrapping technique.](image)

### 3.2 Single Block Diagram

The full system ASIC addresses 32 sensors, divided by 4 equal blocks. The block circuit at a schematic level is shown in Figure 3.12 which is the circuit that is used to test the pseudo-resistor. The block has three main components: a current source (CURRENT SOURCE), a block to select which sensor is read (MR_MUX) and an amplifier (Pre-amp) with a HP filter at its input, which is the main focus of our work. The MR sensors are fabricated separately (1 k$\Omega$ with $\pm10\%$ variation) and wire bonded to the ASIC while RCOM is an external 1 k$\Omega$ resistor. One MR sensor (MR1 to MR8) is selected by the MR_MUX accordingly to the signals $S < 1 : 8 >$ and $NS < 1 : 8 >$, which are generated by an auxiliary circuit that is controlled by a clock signal ($nSync$). The selected sensor is driven with a precision low noise current source.

Our main focus is the HP filter at the input of the amplifier Pre-amp that is part of a two stage output amplifier, since the output amplifier is comprised by other Folded-Cascode amplifier in the full system ASIC which is implemented in front of the amplifier Pre-amp. The output amplifier drives a capacitance around 1 pF. With an output voltage of 2 V and a maximum frequency of 10 MHz, it leads to a slew-rate of 125 V/$\mu$s, and an output current of 1 mA. The amplifier Pre-amp was already designed in a previous work, with a particular focus on the output current, the bandwidth and the noise specifications. The HP filter is comprised by a capacitance of 10 pF and a pseudo-resistor, which is the implementation
proposed in section 3.1. As mentioned before, one of the nodes of the pseudo-resistor is fixed at 1.65 V (negative input of amplifier Pre-amp) and the other node should tend to 1.65 V (amplifier Pre-amp output), yet voltage variations may occur. Therefore, the pseudo-resistor is placed to match the simulation conditions established before, as shown in Figure 3.13.

The MR sensors are selected sequentially by the signals $S < 1 : 8 >$ and $NS < 1 : 8 >$, which are generated by a complementary circuit that is controlled by a clock signal ($nSync$). When the clock signal $nSync$ is set to a logic level ‘1’, a MR sensor is read. Therefore, the pseudo-resistor has to present a resistance that defines a cut-off frequency accordingly to the material under test and its magnetic field frequency. The circuit with a bootstrapping technique is controlled by the clock signal $nSync$, in order to create a path between the source and the gate of the PMOS transistors to define their $V_{SG}$ voltages.
When the clock signal $n\text{Sync}$ commutes to logic '0', a set-up of a different MR sensor is performed, in order to allow a new MR sensor reading. In this stage, the capacitors that comprise the circuit with a bootstrapping technique are referenced to $v_{cm}$ and charged. The pseudo-resistor resistance is set to a low value to reduce the set-up time, taking advantage that in this stage the nodes B are grounded. In Figure 3.14 it is shown the behaviour of the MR sensors signals over two clock signal $n\text{Sync}$ periods, with a description of how the pseudo-resistor implementation is controlled at the two $n\text{Sync}$ logic levels.

![Figure 3.14: Clock signal $n\text{Sync}$ and MR sensors signals.](image)

In order to visualize how the pseudo-resistor implementation change with the clock signal $n\text{Sync}$, the different configurations accordingly to the clock signal $n\text{Sync}$ logic levels are shown in Figure 3.15 ($n\text{Sync} = '0'$) and in Figure 3.16 ($n\text{Sync} = '1'$). As explained before, when the clock signal $n\text{Sync}$ is set to a logic level '0', the node B is grounded and connected to the gate of the PMOS transistors, which results in a resistance in the order of $k\Omega$. The capacitors C are charged in this stage, periodically.

![Figure 3.15: Configuration of the pseudo-resistor implementation for $n\text{Sync} = '0'$](image)

When the clock signal $n\text{Sync}$ commutes to a logic level '1', it is created a path between the source
and the gate of the **PMOS** transistors of the pseudo-resistor. This path allows defining the $V_{SG}$ voltage in all **PMOS** transistors accordingly to the 6-bit code. A resistance with a certain value is established (a $V_{SG}$ voltage around 1.65 V results in a lower resistance, while a $V_{SG}$ voltage close to 0 V results in a higher resistance), in order to define the **HP** filter cut-off frequency.

![Diagram of pseudo-resistor configuration](image)

Figure 3.16: Configuration of the pseudo-resistor implementation for $n_{Sync} = '1'$. 

### 3.2.1 New Pseudo-resistor Configuration

With the pseudo-resistor included in the block of the full system **ASIC** it is possible to start to simulate its behaviour. However, with a preliminary simulation with a **DC** signal at the input of the current source (see Figure 3.12), it is possible to conclude that a modification on the pseudo-resistor implementation, that is presented in Figure 3.11, has to be made. When the clock signal $n_{Sync}$ (red) commutation $'0' \rightarrow '1'$ occurs, the amplifier **Pre-amp** output voltage (blue) shows a variation due to charges stored on the nodes of the pseudo-resistor implementation. Those charges cause a variation on the current that flows through the pseudo-resistor, resulting in the amplifier output voltage variation shown. This variation take approximately 10 milliseconds (this value increases as the resistance increases) to the amplifier output voltage settles to 1.65 V as supposed, which can be visualized in Figure 3.17.

In order to minimize the time that the amplifier **Pre-amp** output voltage needs to tend to 1.65 V, four switches are connected in parallel with the **PMOS** transistors of the pseudo-resistor. When the clock signal $n_{Sync}$ commutation occurs, the switches are closed for a period around 300 nanoseconds to create a low resistance path between the amplifier **Pre-amp** negative input and its output. The new configuration of the amplifier **Pre-amp** with the pseudo-resistor implementation with the switches in parallel with the **PMOS** transistors is shown in Figure 3.18. Performing the same simulation with the new configuration of the pseudo-resistor, it is possible to visualize that the amplifier **Pre-amp** output voltage does not present the variation and tends to 1.65 V almost instantaneously, as shown in Figure 3.19.

The switches implemented in parallel with the **PMOS** transistors of the pseudo-resistor are controlled by a clock signal $n_{Sync2}$. The clock signal $n_{Sync2}$ is generated from the clock signal $n_{Sync}$. The clock
Figure 3.17: Amplifier Pre-amp output voltage (blue) with an input DC signal.

Figure 3.18: Amplifier Pre-amp with HP filter (new configuration).

Figure 3.19: Amplifier Pre-amp (new configuration) output voltage (blue) with an input DC signal.

signal nSync2 is obtained by inverting the clock signal nSync with a delay of approximately 300 nanoseconds. Since this variation in the amplifier Pre-amp output voltage only occurs with large resistances, this delay is only generated for codes with the Most Significant Bit (MSB) = ‘1’. The clock signals nSync
and \(n\text{Sync}2\) are shown in Figure 3.20. Observing the amplifier \(\text{Pre-amp}\) output voltage, it is possible to visualize that the amplifier \(\text{Pre-amp}\) output voltage tends to 1.65 V within the delay between the clock signals \(n\text{Sync}\) and \(n\text{Sync}2\).

![Figure 3.20: Clock signals \(n\text{Sync}\) and \(n\text{Sync}2\) with amplifier \(\text{Pre-amp}\) output voltage.](image)

As referred above, the delay between the clock signals \(n\text{Sync}\) and \(n\text{Sync}2\) is around 300 nanoseconds, which is difficult to implement in microelectronics. However, since area is not a limitation for this work, CMOS inverters with considerable dimensions are used, which are slow inverters, in series with smaller inverters, to implement this delay. A logic NAND gate can be used for the switches to stay open when the MSB = '0'. Dimensions of the inverters used to implement the clock signal \(n\text{Sync}2\) are presented in Table 3.1.

<table>
<thead>
<tr>
<th></th>
<th>Small Inverter</th>
<th>Big Inverter</th>
</tr>
</thead>
<tbody>
<tr>
<td>(W[\mu m])</td>
<td>0.4 1.2</td>
<td>10 30</td>
</tr>
<tr>
<td>(L[\mu m])</td>
<td>0.35 0.35</td>
<td>10 10</td>
</tr>
</tbody>
</table>

The diagram of the inverters that generate the clock signal \(n\text{Sync}2\) is shown in Figure 3.21.

![Figure 3.21: Inverters for generating clock signal \(n\text{Sync}2\) diagram.](image)

With the simulations presented, it is possible to conclude that connecting the bulk of the PMOS transistors of the pseudo-resistor to the supply voltage results in bulk leakage currents. In order to that effect can be minimized, the bulk terminal is connected to the source. However, the symmetry that the implementation with the bulk connected to the supply voltage presented is lost. Nevertheless, the priority
is to guarantee that the resistance is not lower than the resistance needed to have a cut-off frequency coherent to the magnetic field frequency of the material under test.

The simulation results presented in section 3.1 are updated, in order to evaluate the behaviour of the pseudo-resistor resistance with the bulk of the PMOS transistors connected to the source. Therefore, new simulations results with different values for \( V_{SG} \) are shown in Figure 3.22.

![Figure 3.22: Simulation results with pseudo-resistor implemented with PMOS transistors (bulk connected to the source).](image)

Comparing these simulation results to the simulation results presented in Figure section 3.1, it is possible to conclude that with the bulk connected to the source the resistance is not symmetrical as the implementation with the bulk connected to the supply voltage. However, that is not critical, since the resistance maintains the same behaviour as function of the \( V_{SG} \) voltage, allowing to adjust the pseudo-resistor resistance. Adjusting the resistance, the cut-off frequency can be varied accordingly to the magnetic field frequency of the material under test. A simulation result is shown in Figure 3.23, which results from applying ground to the gate of the PMOS transistors of the pseudo-resistor implementation.

In this case, the resistance maintains the same behaviour comparing to the pseudo-resistor implementation with the bulk of the PMOS transistors connected to the supply voltage. As mentioned in section 3.1, the resistance is higher than the values needed to reduce the set-up time to a value between 0.1 \( \mu \)s and 1 \( \mu \)s. Although, the difference is not significant. Therefore, as explained before, a evaluation of the behaviour of the pseudo-resistor implementation under the conditions of the NDT system is performed, which is presented in the next section.
3.2.2 Amplifier Pre-amp Set-up Time

Our main goal is to implement a HP amplifier with the set-up time in the range $[0.1 \, \mu s; 1 \, \mu s]$. By reducing the set-up time, it is possible to reduce the time needed to switch between the MR sensors, since the purpose of the ASIC during set-up time is to quickly address the 32 sensors of the array. Therefore, by reducing the set-up time at each commutation, a reduction in the set-up time of the whole NDT system is ensured. A simulation is made to evaluate how the pseudo-resistor implementation with the new configuration (bulk of PMOS transistors connected to the source; switches in parallel with PMOS transistors) on the feedback of the amplifier Pre-amp performs. The objective is to analyse which is the achievable reduction in the set-up time, when the commutation between the MR sensors occurs. The simulation result concerning the amplifier Pre-amp output voltage (blue) set-up time is shown in Figure 3.24.
A variation in the amplifier Pre-amp output voltage occurs when the clock signal nSync commutes
to a logic level ‘0’. The amplifier output voltage has to settle to 1.65 V as fast as possible. For that
purpose, a fast settling technique is used, applying 0 V to the gate of the PMOS transistors that are part
of the pseudo-resistor (see Figure 2.19). With the marked points in the simulation result, the set-up time
of the amplifier Pre-amp output voltage is obtained, resulting in a set-up time equal to 0.291 µs, which
represents a value that is within our objectives. With the pseudo-resistor implementation without the
switches in parallel, the set-up time is affected, since a slow variation on the amplifier Pre-amp output
voltage occurs. The same effect occurs if a high resistor is used, without the feature of switching the
pseudo-resistor to present a low resistance. Although, with the pseudo-resistor implementation with the
switches in parallel with the four PMOS transistors, the switching between the MR sensors occurs with
a minimum time overhead, as shown in Figure 3.24.

The simulation of the pseudo-resistor resistance presented in Figure 3.23 resulted in a 25 kΩ resis-
tance, approximately, for |ΔV| = 0 V. Nevertheless, in the NDT system during set-up time, four switches
are in parallel with the pseudo-resistor implementation, which decreases the pseudo-resistor resistance.
Furthermore, the current that flows into the pseudo-resistor in the block of the full system ASIC is 10
times higher than the current that flows through the pseudo-resistor in the simulations performed to
evaluate the resistance behaviour before its implementation on the feedback of the amplifier Pre-amp. A
higher current also reduces the pseudo-resistor resistance. Despite that the exact resistance in the set-
up is difficult to obtain, since it presents significant variations, it is possible to predict that the equivalent
resistance is lower than 25 kΩ (as obtained in the simulation with only the pseudo-resistor implement-
tion), accordingly to the set-up time obtained. Therefore, it is possible to conclude that, in the NDT
system, equivalent resistances in the order of kΩ (lower than 25 kΩ) are achieved, as presented in the
next chapter.

3.3 Summary

This chapter presented the pseudo-resistor implementation with the PMOS transistors that is used
on the feedback of the amplifier Pre-amp (see Figure 3.18). This implementation guarantees a variable
resistance as shown in simulation results (see Figure 3.22 and Figure 3.23). A variable resistor allows
to achieve our objectives, since it is possible to have a 320 MΩ resistance and a resistance in the order
of kΩ, approximately, allowing to present a 50 Hz cut-off frequency and a reduction in the set-up time.

In order to implement this pseudo-resistor, two complementary circuits were proposed. A circuit
with a bootstrapping technique (see Figure 3.7) and a 6-bit output voltage DAC are used to define the
voltage between the source and the gate of the PMOS transistors of the pseudo-resistor implementation.
The pseudo-resistor resistance varies accordingly to VSG of the PMOS transistors that are part of the
pseudo-resistor. The proposed circuit with a bootstrapping technique allows to define the VSG voltage,
charging a capacitor referenced to vcm with a VTune voltage and then applying that voltage to the gate
of the PMOS transistors, creating a path between the source and the gate of the PMOS transistors. This
circuit with a bootstrapping technique has an input VTune, which is a voltage provided by the 6-bit output
voltage DAC. With these two circuits, it is possible to present a complete pseudo-resistor implementation without the ideal voltage sources.

Our [NDT] system has an [ASIC] that is comprised by 4 blocks for a 32-sensor array. A schematic of one of that blocks is presented in section 3.2. This block is comprised by a current source, a resistor array to work as MR sensors, a multiplexer to select a sensor to be read and an amplifier. This amplifier (Pre-amp) is the circuit that we are focused on this thesis. The amplifier Pre-amp has a HP filter at its input, which is a first-order RC filter. The capacitor has a capacitance of 10 pF, while the resistor is implemented with the pseudo-resistor presented in section 3.11. With the simulation results presented, it is possible to conclude that with that pseudo-resistor implementation, the HP filter cut-off frequency can be varied, adjusting it accordingly to the magnetic field frequency of the material under test. This is an improvement to our objective of defining a 50 Hz cut-off frequency for all the materials. The pseudo-resistor has also to present a low resistance, in order to reduce the time needed to switch between the MR sensors. The pseudo-resistor is controlled by a clock signal nSync, which also controls the switching between the MR sensors. Therefore, the pseudo-resistor resistance varies its value accordingly to that signal, allowing to have the full system synchronized. Finally, a simulation result regarding the set-up time is presented (see Figure 3.24), showing that with the technique used to have a low resistance, applying 0 V to the gate of PMOS transistors as presented in section 2.3 is possible to have a set-up time around 0.3 µs. This value is within our objectives, showing that, with this pseudo-resistor, an implementation of the HP amplifier with a low set-up time is achievable, which is our main goal.
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System Results and Layout

Contents

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In this chapter, the simulations results of the transient analysis regarding the pseudo-resistor resistance and the amplifier Pre-amp bandwidth are shown and evaluated. The layout design of the circuit components are presented.

With some transient analyses, it is possible to take better conclusions about the behaviour of the circuit, concerning the pseudo-resistor resistance and the high-pass filter cut-off frequency, allowing to take some conclusions about their relation. The simulation results concerning the pseudo-resistor implementation resistance are presented in section 4.1. Firstly, the time-domain simulation results with a DC input are shown, in order to evaluate how the resistance varies with the 6-bit DAC output voltage. The simulation results with an AC input, for analysing if at least one resistance guarantees a cut-off frequency equal to 50 Hz. Considerations regarding Monte Carlo simulations are presented in section 4.2. Those simulations are used to predict process variations. The Monte Carlo testing is used to evaluate if even with that variations, it is possible to guarantee that at least one resistance results into a cut-off frequency equal to 50 Hz. Finally, the circuit components layouts are presented in 4.3.

### 4.1 System Results

The simulation setup and the simulation results concerning the set-up time are shown in the previous chapter. Finally, it is essential to present the simulation results regarding the resistance when the MR sensors are read. The magnetic field frequency is in the range \([100 \text{ Hz, } 10 \text{ MHz}]\), depending on the material under test. Therefore, our main objective is to have a 50 Hz cut-off frequency. Nevertheless, the simulation results concerning the behaviour of the pseudo-resistor implementation show that we can vary its resistance and, consequently, vary the pole frequency.

#### 4.1.1 Transient Analysis with DC Input

In order to evaluate the achievable cut-off frequency range with our pseudo-resistor implementation, a simulation with all the codes of the 6-bit output voltage DAC to obtain the resistance for each code is performed. The simulation results for fourteen codes for a clock signal \(n_{\text{Sync}}\) period with a DC input are shown in Figure 4.1, which are the resistances that presented the better results.

For these codes, a resistance almost constant for all the clock signal \(n_{\text{Sync}}\) period is obtained, despite that for few milliseconds after the clock signal \(n_{\text{Sync}}\) commutation \(‘0’ \rightarrow ‘1’\) the resistance presents a variation caused by the variation in the output voltage amplifier Pre-amp, which can prejudice the settling time. With the marked points referring minimum and maximum resistance obtained, a maximum and minimum cut-off frequency is determined, respectively. The equation \(2.1\) is used to determine the cut-off frequency, \(f_{\text{cut-off}}\). With a \(R_{\text{min}} = 352.6 \text{ k}\Omega\) results in a maximum cut-off frequency equal to 45 kHz, while with a \(R_{\text{max}} = 1.231 \text{ G}\Omega\) a minimum cut-off frequency equal to 13 Hz is obtained.

The simulation results shown in Figure 4.1 are presented only with fourteen codes, because the resistances greater than 1.231 GΩ are not used for our application. The resistances smaller than 352.6 kΩ present significant variations after the clock signal \(n_{\text{Sync}}\) commutation, as shown in Figure 4.2.
Those smaller resistances can be used, because they are used for small clock signal $nSync$ periods (periods of $\mu$s) and for those kind of periods, the resistance settles to a constant value faster as shown in Figure 4.3. Despite the resistances greater than 1 GΩ are not used in our application and the initial variations in smaller resistances, it is still advantageous to have 64 codes available, to account for process variations, adjusting the bits externally to present a resistance that matches our specifications.
4.1.2 Amplifier Pre-amp Bandwidth

A simulation result presenting the AC frequency response of the HP amplifier is shown in Figure 4.4. In order to evaluate how the AC response varies with the \( V_{SG} \) voltage, different \( V_{SG} \) voltages are imposed. Theoretically, the cut-off frequency is lower with small \( V_{SG} \) voltages, since the pseudo-resistor presents a very high resistance. Increasing the \( V_{SG} \) voltage of the PMOS transistors that are part of the pseudo-resistor and consequently, decreasing the resistance, the cut-off frequency increases.

![Figure 4.4: Amplifier Pre-amp bandwidth.](image)

Analysing the AC frequency response for each \( V_{SG} \) voltage, it is possible to conclude that the cut-off frequency has nine orders of magnitude, between mHz and MHz, which corresponds to resistances between T\( \Omega \) and k\( \Omega \), respectively. Nevertheless, in our application, a minimum cut-off frequency equal to 50 Hz is enough. Comparing these cut-off frequencies with the resistances presented before, the cut-off frequency does not match exactly with the resistance. However, in the AC analysis losses are
not taken into account, which can result in simulation results variations, between the simulation result with the pseudo-resistor and the simulation result presented in Figure 4.4. Nevertheless, it is possible to conclude that the amplifier *Pre-amp* presents a variable bandwidth with cut-off frequencies between 0.045 Hz and 1.765 MHz, which means that the cut-off frequency can be varied accordingly to the materials of interest, which have their magnetic field frequency between 100 Hz and 10 MHz.

### 4.1.3 Transient Analysis with AC Input

Finally, a simulation with an AC input signal is performed, in order to conclude if the resistance works as supposed. With an AC input signal with a certain frequency, especially with a frequency equal to 50 Hz, the pseudo-resistor has to present at least one resistance that allows the MR sensors readings. Therefore, a simulation result with an AC input with a frequency equal to 50 Hz is presented in Figure 4.5 for two different codes, resulting in two different resistances. By using an AC input, it is possible to confirm that the pseudo-resistor continues to guarantee that the amplifier *Pre-amp* set-up time is between 0.1 µs and 1 µs, as shown in Figure 4.6.

![Figure 4.5: Transient analysis with AC input for two different resistances.](image)

In Figure 4.5 it is possible to visualize that for '001101' the amplifier *Pre-amp* output voltage is only a DC signal. For '110011', the amplifier *Pre-amp* output voltage has an AC component. This means that for the first code the cut-off frequency is above 50 Hz and for the second code the cut-off frequency is below 50 Hz, as represented in Figure 4.7.

These results prove that the pseudo-resistor can vary its resistance and, consequently, the pole frequency, allowing to have a variable bandwidth. The input signal frequency can be changed, in order to confirm that a variable bandwidth is achieved, adjusting the cut-off frequency accordingly to the material under test. The simulation results for two other frequencies, 1 kHz and 100 kHz, are presented in Figure 4.8 and in Figure 4.9 respectively. Since it is pretended to read 10 signal periods of MR sensors, the clock signal *nSync* period also changes with the AC input signal frequency.

Despite the good results presented, the amplifier *Pre-amp* output voltage suffers a shift on its DC
Figure 4.6: Settling time with AC input.

Figure 4.7: Pre-amp amplifier AC response.

Figure 4.8: Transient analysis with an AC input signal (1 kHz).
voltage when clock signal \textit{nSync} commutes to a logic level ‘1’. This can be explained by a charge redistribution when the commutation occurs, since it is necessary to take into account the capacitances associated with the devices, which are represented in Figure 4.10 to predict the devices AC behaviour \cite{14}. However, that DC shift does not compromise the MR sensors readings. Although, this issue will be analysed more carefully in a future work, improving our solution of implementing four switches in parallel with the PMOS transistors that are the main part of the pseudo-resistor implementation.

![Figure 4.9: Transient analysis with an AC input signal (100 kHz).](image)

\textbf{4.2 Monte Carlo Simulations}

The Monte Carlo simulations are used to predict the fabrication process parameter and the device mismatch, in order to evaluate the design performance with that effects. For each Monte Carlo iteration, new pseudo-random values are generated for the specified netlist parameters \cite{15} and, then, a particular analysis are performed (for example, transient analysis), presenting variations accordingly to the values.
generated for the netlists.

Our main objective with the Monte Carlo analysis is to examine and validate our circuit, focusing on the pseudo-resistor implementation. Therefore, it is essential to confirm that the pseudo-resistor implementation allows having a cut-off frequency that matches with the magnetic field frequency of the material under test. Since the Monte Carlo simulations are computationally heavy, our focus is on the 50 Hz cut-off frequency, which is a reference value in our objectives in this work. In order to validate the proposed pseudo-resistor implementation, it is necessary that at least one code of the 6-bit DAC provides a voltage that guarantees a 320 MΩ (or higher) resistance to achieve a cut-off frequency equal to 50 Hz.

A Monte Carlo simulation with 500 iterations is executed, using an AC input signal with 50 Hz, analysing at each iteration the amplifier Pre-amp output voltage, in order to evaluate the effects of the Monte Carlo simulation variations. The simulations results allowed to conclude that 90% of the iterations are similar with the simulation results shown in the section 4.1, while for 10% of the iterations the DC shift referred before is more problematic. The DC shift can result in a signal that is not stabilized, presenting variations through the clock signal period, or result in a DC shift high enough to saturate the amplifier Pre-amp, which is prejudicial to the MR sensors readings. In Figure 4.11, it is shown one of that cases (amplifier Pre-amp output voltage - blue) for the DAC codes between ‘110000’ and ‘111111’. The set-up time does not suffer significant variations in Monte Carlo simulations. In all the iterations, when nSync = ‘0’, the resistance maintains a value that allows to achieve the objective of having a set-up time between 0.1 µs and 1 µs between the MR sensors readings. These results confirm that the proposed pseudo-resistor implementation is a solution to achieve our objectives in most cases (90% of the 500 Monte Carlo simulations). However, in 10% of the Monte Carlo simulations, the pseudo-resistor caused significant DC variations on the amplifier Pre-amp output voltage during the steady-state operation. This will be an issue to analyse and solve in a future work.

![Monte Carlo simulation (worst case).](image)

In Figure 4.12, a simulation result with a typical case for the codes between ‘110000’ and ‘111111’ is presented. Each clock signal nSync period results in a different code.
This simulation result represents a typical case for the amplifier Pre-amp output voltage behaviour, since it can be visualized that for lower resistances the amplifier Pre-amp output voltage has only a DC signal. For higher resistances, it presents an AC component, showing that the cut-off frequency varies with the resistance. For four codes, at least, the MR sensors readings are not prejudiced, only presenting the DC shift, which is not harmful.

4.3 Layout

4.3.1 Fingering

The main goal of a layout design with fingering is to attenuate the influence of the fabrication process variations. By using this technique, the variations that affect a certain transistor are attenuated, with a greater probability, by a symmetrical variation in another finger of the same transistor or by the average variations in all fingers be null. Fingering is used to reduce both the S/D junction area and the gate resistance [14]. This technique is used to minimize the sensibility to the voltage noise, due to the temperature variations, since the poly and the diffusions have a non-constant characteristic with temperature variations. However, while the gate resistance can be reduced by decomposing the transistors in fingers, the capacitance associated with the perimeter of the source/drain area increases [14].
4.3.2 Dummy Transistors

Dummy transistors are used in circuits layout design, without having active influence on the circuit behaviour. The dummy transistors protect the surrounding transistors of the circuit layout in the fabrication process, since the excessive metal is removed to have metal tracks well defined, by using a process known as etching. The transistors poly is also affected in the fabrication process. The dummy transistors are used to protect the transistors poly, in order to maintain the design after the fabrication as closest as possible to the projected.

The dummy transistors provide an environment to the surrounding transistors close to the environment of the central transistors of the layout design. The dummy transistors have their sources and drains shorted circuit, in order to not interfere with the circuit performance.

![Figure 4.14: Dummy transistors to improve symmetry](image)

4.3.3 Common centroid

Asymmetrical dispositions in circuits are sensible to process variations and thus, introduce voltage offsets, common-mode noise and non-linearities. Therefore, it is necessary to have a symmetrical layout, in order to reduce those effects. With a common centroid layout is guaranteed a homogeneous distribution of voltage and current through the circuit, increasing its linearity. A common centroid configuration is used to cancel the effect of first-order gradients. For exemplification, a common centroid layout design of a differential pair, represented in Figure 4.15a, is shown in Figure 4.15b.

![Figure 4.15: Differential pair and its layout](image)
4.4 Circuit Components Layout

In this section, the proposed circuit components layout are presented. In this work, our main component is the pseudo-resistor implementation, which is comprised by four PMOS transistors along with a circuit with a bootstrapping technique and a shared 6-bit output voltage DAC.

Firstly, the proposed circuit with a bootstrapping technique is presented. This component is grouped with the pseudo-resistor implementation layout. The DAC layout is then introduced, which can be separated into three main parts: the resistor array, the matrix of switches and the buffer amplifier. Finally, the interface circuits for generating the clock signal nSync2 are presented.

4.4.1 Circuit with a Bootstrapping technique

The circuit with a bootstrapping technique is shown in Figure 4.16. Only metal one and metal two are used, which are oriented vertically and horizontally, respectively, while metal three is not used. The capacitor C has a capacitance of 10 pF, which occupies a significant area, in order to guarantee that this capacitor is dominant in relation to the pseudo-resistor transistors capacitances. That value of capacitance is also explained by the need of maintaining the voltage that charges the capacitor constant for a longer period of time to allow the measurements to be taken.

Figure 4.16: Circuit with a bootstrapping technique (Layout).

This component layout occupies, approximately, 116.5 \times 141.6 \mu m^2, due to the large area occupied by the capacitor, which has a capacitance of 10 pF.
4.4.2 Pseudo-resistor

The pseudo-resistor layout has four circuits with a bootstrapping technique (each one for a PMOS transistor), as shown in Figure 4.17. As explained in the previous component, metal one and metal two are oriented vertically and horizontally, respectively. Despite we try to not use metal three, in this layout is necessary to do some connections, in order to not overlap metals, which is a design rule.

![Figure 4.17: Pseudo-resistor (Layout).](image)

This layout occupies, approximately, $242 \times 335.5 \ \mu m^2$, due to this circuit comprises four circuits with a bootstrapping technique.

4.4.3 Digital-to-Analog Converter

The 6-bit output voltage DAC is comprised by three main components: the resistor array, the matrix of switches and the buffer. The resistor array is comprised by sixty-four 1 kΩ resistors that match with the number of bits ($2^6 = 64$), while the matrix of switches has 150 transmission gates working as switches. Finally, the buffer has a Folded-Cascode topology. As explained before, we wanted a simple circuit to provide the voltage at the input of the circuit with a bootstrapping technique ($V_{TUNE}$). Since the components that are part of this 6-bit DAC are circuits that we already implemented in the pseudo-resistor implementation (transmission gates), while others we studied it before (buffer with a Folded-Cascode topology [18]), we decided to use them.

4.4.3.1 Resistor Array

As mentioned before, a resistor array comprised by sixty-four 1 kΩ resistors is used to create each voltage that is used as an input of the circuit with a bootstrapping technique. The resistor array layout designed is shown in Figure 4.18.
Each 1 kΩ resistor occupies an area of $10 \times 8.15 \, \mu m^2$. Totally, this layout occupies, approximately, $151 \times 155.5 \, \mu m^2$.

### 4.4.3.2 Matrix of switches

A matrix of switches with 150 transmission gates is implemented to create a path between the resistor, selected accordingly to the 6-bit code, and the buffer amplifier. Therefore, this layout is mainly comprised by each transmission gate layout and their corresponding connections. Metal one and metal two are used, vertically and horizontally, respectively, while metal three is used only once to respect the design rules. The matrix of switches layout is shown in Figure 4.19.

This layout has an area equal to $403 \times 239 \, \mu m^2$, approximately, which is explained by the number of transmission gates used to work as switches.
4.4.3.3 Buffer

A buffer amplifier with a Folded-Cascode topology is used, since it is a topology that we already implemented in Analog Integrated Systems course [16]. For that reason, since the 6-bit output voltage DAC implementation is not a main topic in this work, the amplifier already implemented on that course is used. The voltage buffer layout is shown in Figure 4.20.

![Figure 4.20: Voltage Buffer (Layout).](image)

This layout occupies, approximately, 108.8 × 71.3 μm². Metal one (vertically) and metal two (horizontally) are used, while metal three is not used.

4.4.4 Clock generator

In section 3.2, a circuit to generate a clock signal (nSync2) from the clock signal nSync is presented, which uses inverters, mainly. The clock signal nSync2 is used to control four switches that are in parallel with the four PMOS transistors that are part of the pseudo-resistor implementation (see Figure 3.19). This circuit uses inverters with considerable dimensions (see Table 3.1), in order to have a delay around 300 nanoseconds between the clock signal nSync and the clock signal nSync2 (see Figure 3.20). A logic circuit to generate non-overlapping clocks is also used. The clock generator layout is shown in Figure 4.21. Metal one and metal two are used, vertically and horizontally oriented, respectively, while metal three is used only once, in order to not overlap the same metal type, respecting the design rules.

This layout occupies, approximately, 185 × 200 μm², due to large area occupied by the big inverters used to implement the clock signal nSync2 (NMOS transistors - W = 10 μm, L = 10 μm; PMOS transistors - W = 30 μm, L = 10 μm).
4.4.5 ASIC Block Layout

In this section, it is presented the layout design of the circuit presented in section 3.2 (see Figure 3.12), which corresponds to one of the four blocks that are part of the full system ASIC. In this layout design, the components layout previously designed are included (the current source, the multiplexer MR_MUX and the amplifier Pre-amp). The ASIC block layout design is shown in Figure 4.22, which is divided into five main components: the current source (red box); the multiplexer to select a MR sensor (white box); the amplifier Pre-amp (green box); the capacitors of 1 pF and 10 pF (blue box) and the pseudo-resistor implementation (yellow box). This layout design occupies an area of $890 \times 1060 \mu m^2$, approximately.
4.5 Summary

In section 4.1, the simulations results of transient analysis are presented. Firstly, a transient analysis results with a DC input is shown, in order to evaluate the pseudo-resistor resistance when the clock signal \( n\text{Sync} \) is set to a logic level ‘1’. A constant resistance with a range between 352.6 k\( \Omega \) and 1.231 G\( \Omega \) is obtained, which results in a cut-off frequency between 45 kHz and 13 Hz, respectively. Therefore, the pseudo-resistor proposed is an implementation of a variable resistor that allows to vary its resistance and, consequently, vary the pole frequency, which results in a variable bandwidth. Since different materials have different magnetic field frequencies, this pseudo-resistor can be used to have...
a cut-off frequency that matches with the magnetic field frequency of the material under test. In order to confirm that a variable bandwidth is achieved, a transient analysis with an AC input for different frequencies is presented. Our priority is to have a pseudo-resistor that presents a 320 MΩ, which results in a cut-off frequency equal to 50 Hz. With this pseudo-resistor implementation that objective is achieved, as shown in Figure 4.5. Since that objective is accomplished, an improvement of that objective is evaluated, adjusting the cut-off frequency accordingly to the material under test and, consequently, a variable bandwidth, as confirmed with a simulation presenting the amplifier Pre-amp bandwidth. A simulation to analyse the set-up time with an AC input is also performed, resulting a value within our objectives. In section 4.2 the Monte Carlo simulations validated our pseudo-resistor implementation for 90% of the 500 iterations by using an AC input signal with a 50 Hz frequency, analysing all the available resistances, confirming that at least one results in a cut-off frequency that allows to the MR sensors readings.

In section 4.4 the layout design of circuit components developed in this thesis are presented. Firstly, the circuit with a bootstrapping technique layout is presented. This circuit is included in the pseudo-resistor implementation along with the four PMOS transistors, since each PMOS transistor has one circuit with a bootstrapping technique, in order to define the \( V_{SG} \) voltage of each PMOS transistor. Then, the 6-bit output voltage DAC layout is presented. This layout can be divided into three parts: the resistor array, the matrix of switches and the buffer amplifier. The layout design of an interface circuit, that is used to generate the clock signal \( n\text{Sync}2 \), is shown. Finally, the ASIC block layout design is presented.
5

Conclusions
Our NDT system uses a method based on EC evaluation, since it is the most used method to detect superficial and internal flaws on conductive materials. The MR sensors, which are resistive sensors that vary its electrical resistance accordingly to the magnetic field, are used in our NDT system. The depth of penetration that can be analysed depends on the magnetic field frequency. For the materials of interest, that frequency is in the range [100 Hz, 10 MHz]. Our NDT system has integrated an ASIC that drives the MR sensors and it has 8 sensors per amplifier and 4 blocks for a 32-sensor array (see Figure 2.5). Each block has a Folded-Cascode topology amplifier (Pre-amp), which was the main focus of our work. These amplifiers are preceded each one by a first-order RC HP filter. Although this is a system already implemented, the way the MR sensors are biased and switched was our focus on this work, since it is necessary that the HP filter can present a cut-off frequency equal to 50 Hz, which can be achieved with a 320 MΩ resistor (HP filter resistor). However, the same resistor has to present a significantly lower resistance when the MR sensors are switched, in order to reduce the amplifier set-up time to a value between 0.1 µs and 1 µs. This reduction has to be achieved to accomplish our main goal of implementing a HP amplifier with a low set-up time. Therefore, our goal was to implement a variable resistor that can present a value between 1.5 kΩ and 15 kΩ, when the commutation between the MR sensors occurs, and a 320 MΩ resistance, when the MR sensors are read.

The HP filter resistor was implemented with a pseudo-resistor, which uses four PMOS transistors, since it can be integrated on-chip, presenting resistances in the orders desired. A pseudo-resistor implementation that allows varying its resistance by changing the $V_{SG}$ voltage of the PMOS transistors was proposed. A circuit with a bootstrapping technique to define the $V_{SG}$ voltage of the transistors is used, which allows to vary that voltage along with a 6-bit DAC and, consequently, vary the pseudo-resistor resistance. With that variation, our objective of having a cut-off frequency equal to 50 Hz was improved, resulting in a variable bandwidth, which means that we can change the pseudo-resistor resistance and vary the cut-off frequency, accordingly to the material under test. A variable resistor, that presented the better results with a variation between 352.6 kΩ and 1.231 GΩ, is presented, which results in a variation in the HP cut-off frequency between 13 Hz and 45 kHz, approximately, as confirmed by the simulation results. A 6-bit output voltage DAC was implemented using a very simple topology, in order to provide a voltage at the input of the circuits with a bootstrapping technique.

The circuit with a bootstrapping technique is also used to connect the gate of the PMOS transistors that are part of the pseudo-resistor implementation to ground. Therefore, a path on the feedback of the amplifier Pre-amp with a low resistance is created, which reduces the set-up time. With this pseudo-resistor implementation, a set-up time equal to 0.3 µs is achieved, which is a value within our objectives, improving the set-up time presented in the state-of-the-art. Therefore, our main goal of implementing a HP amplifier with a low set-up time was achieved. This goal was achieved with a novel pseudo-resistor implementation with a bootstrapping technique, presenting also a variable bandwidth, since it is possible to vary the pseudo-resistor resistance and, consequently, vary the cut-off frequency.

The layout design (AMS 0.35 μm technology) of the circuit components developed in this thesis was presented, using layout design techniques, such as fingering, dummy transistors and common centroid.
Future work

Future work suggestions are based in three main parts. Firstly, it is possible to improve the performance of the pseudo-resistor implementation, with a particular focus on the amplifier Pre-amp output DC voltage shift discussed in section 4.1. This DC shift can harm the MR sensors readings or present readings with significant variations. Nevertheless, the circuit can be sent to fabrication (AMS 0.35 μm technology), in order to evaluate its behaviour, with measurement results, focusing on measuring the pseudo-resistor resistance.

Secondly, with Chopper Stabilization implemented on the amplifier Pre-amp, the pseudo-resistor proposed in this thesis can be used to implement a Miller integrator, in order to sense the DC components from the MR sensors biasing signals. That DC components are modulated to the chopper frequency and, consequently, are not blocked by the input capacitors [5]. The integrator has to present a low pole frequency near to DC, which can be achieved with the pseudo-resistor proposed in this work.

Finally, the pseudo-resistor linearity is an aspect that can be improved. In [17], a method to improve the linearity of a tunable pseudo-resistor is proposed, which is shown in Figure 5.1. This circuit allows for a first-order cancellation of the process dependency of the pseudo-resistor, which can be implemented in our circuit to correct process variations.

![Figure 5.1: A: Tunable Pseudo-resistor; B: Proposed adaptive bias circuit: the pseudo current mirror [17].](image)
References


