TÉCNICO LISBOA

Integrated Eddy Current based Non-destructive Testing System for High-end Applications

A Capacitively Coupled Chopper Instrumentation Amplifier

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Abstract

This work addresses an Eddy-Current (EC) Non-Destructive Testing (NDT) system that makes use of Magneto-Resistive (MR) sensors to characterize metallic samples under test. A system with MR sensors can work with low-frequency magnetic signals to allow higher penetration depths. The resultant signals are processed by an Application Specific Integrated Circuit (ASIC), that includes a pre-amplifier, which is the focus of this work.

The pre-amplifier presents a very significant flicker noise contribution that impairs measurements. To reduce flicker noise, Chopper Stabilization is implemented. The pre-amplifier has a Folded Cascode topology and implements a capacitive feedback, which allows superior gain precision, when compared with resistive feedback configurations.

The action of chopper modulators results in the modulation of input DC components that are not blocked by the input capacitors. When amplified, these DC components can cause the saturation of the pre-amplifier. For this reason, a DC Servo Loop (DSL) is added, as it extracts the output DC component and, by means of negative feedback, subtracts it from the amplifier input, achieving its cancellation.

The pre-amplifier was designed in AMS 0.35 µm CMOS technology and has a simulated gain of 20 dB, while presenting an Input-Referred Noise (IRN) of 6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz and noise floor of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The pre-amplifier also presents an attenuation of 60 dB for the DC signals, allowing the attenuation of DC components up to 200 mV.

Keywords

Non-destructive Testing, Folded Cascode Pre-Amplifier, Capacitive Feedback, Flicker Noise, Chopper Stabilization, DC Suppression

Resumo

O presente trabalho foca um sistema de Testes Não Destrutivos baseado em Correntes de Foucault, que utiliza sensores Magneto-resistivos (MR) para caracterizar amostras metálicas sob teste. Um sistema com sensores MR pode funcionar com sinais magnéticos de baixa frequência para permitir maiores profundidades de penetração. Os sinais resultantes são processados por um *Application Specific Integrated Circuit* (ASIC), que inclui um pré-amplificador, que constitui o foco deste trabalho.

O pré-amplificador apresenta uma contribuição de ruído de *flicker* bastante significativa que corrompe as medições. Para reduzir o ruído de *flicker*, *Chopper Stabilization* é implementado. O pré-amplificador tem uma topologia *Folded Cascode* e implementa um *feedback* capacitivo que permite uma precisão de ganho superior, aquando comparado com uma configuração de *feedback* resistivo.

A acção dos moduladores de *chopper* resulta na modulação das componentes DC de entrada que não são bloqueadas pelos respectivos condensadores. Quando amplificadas, estas componentes podem causar a saturação do pré-amplificador. Por esta razão, o *DC Servo Loop* (DSL) é adicionado, já que este extrai a componente DC de saída e, através de um *feedback* negativo, subtrai-a da entrada do pré-amplificador, atingindo assim o seu cancelamento.

O pré-amplificador foi projectado numa tecnologia AMS 0.35 µm CMOS e possui um ganho simulado de 20 dB, enquanto demonstra um IRN de 6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ a 100 Hz e um patamar de ruído de 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. O pré-amplificador apresenta ainda uma atenuação de 60 dB para sinais DC, permitindo a atenuação destas componentes DC até 200 mV.

Palavras Chave

Testes Não Destrutivos, Pré-Amplificador *Folded Cascode*, *Feedback* Capacitivo, Ruído de *Flicker*, *Chopper Stabilization*, Supressão de DC

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List of Acronyms

AC Alternating Current

ADC Analog to Digital Converter

ASIC Application Specific Integrated Circuit

CCCIA Capacitively Couple Chopper Instrumentation Amplifier

CMFB Common-Mode Feedback

CM Common-Mode

CS Common-Source

DAC Digital to Analog Converter

DC Direct Current

DM Differential-Mode

DSL DC Servo Loop

EC Eddy-Current

IRN Input-Referred Noise

MOS Metal–Oxide–Semiconductor

MR Magneto-Resistive

NDT Non-Destructive Testing

NMOS N-type MOS

OTA Operational Transconductance Amplifier

PAC Periodically AC

PMOS P-type MOS

PNOISE Periodically Noise

PSD Power Spectral Density

PSS Periodically Steady-State

SC Switched Capacitor

S&H Sample & Hold

SNR Signal-to-Noise Ratio

TG Transmission Gate

VLTC-SC Very Large Time Constant Switched Capacitor

1

Introduction

Contents

1.1 Motivation

Nowadays, worldwide industry has been more and more dependent on electronics that provide cheaper, faster and safer ways for production of goods. From designing, to production and testing, society is aided, in the process of creating new products and services, by all kind of electronic devices. The increasing autonomy and processing power of these devices has allowed the development of testing techniques that rely on measuring physical attributes of the manufactured goods without compromising their integrity, that is Non-Destructive Testing (NDT). NDT provides a way to diagnose defects and imperfections on the test subject without compromising its characteristics. This evaluation of the condition of an object can be done via X-ray, ultrasounds, Eddy-Currents (ECs) and other means [1], [2], [3]. EC NDT, specifically, is used to assess the condition of conductive materials, by inducing electric currents on them, generated by magnetic fields. The presence of defects will, consequently, modify the magnetic field that is picked up and used to characterize the test subject. This kind of testing is extremely important in areas such aeronautics, aerospace, electric energy production, automotive and many others where human inspection is not practical and/or is dangerous [2]. The conventional EC NDT probes usually implement one or more sensing coils [3]. Other probes rely on sensors, which can be integrated in a chip, but their reduced number usually result in low resolutions.

This work is inserted in the project described in [4] and focus an EC NDT system, in which an array of Magneto-Resistive (MR) sensors is used. The number of sensors in the array can be scaled to allow increased resolution and inspection speed. The sensors present variations in resistance with the applied magnetic field, which are picked up and processed by an Application Specific Integrated Circuit (ASIC), that amplifies signals and filters out the unwanted components.

The EC NDT system, for higher penetration depths, requires lower frequencies. At such frequencies, the transistors of the pre-amplifier included in the ASIC add a high flicker (or low-frequency) noise contribution, which is a type of noise inversely proportional to the frequency. Also, the sensors are biased by a DC signal that, when amplified, is capable of saturating the output pre-amplifier. In this work, solutions to these two problems are addressed by exploring flicker noise reduction and DC cancellation techniques to produce an improved pre-amplifier for the NDT system.

1.2 Objectives

The focus of this work is the output pre-amplifier of the ASIC and the main goal is to reduce its flicker noise, while blocking input DC signals. For this reason, noise reduction and DC cancellation techniques are studied and applied to this amplifier. The following objectives were established:

- study the performance of Autozero and Chopper Stabilization as flicker noise cancellation techniques;

- apply the most suitable technique for this kind of application to the amplifier;
- achieve DC sensor biasing signal cancellation;
- produce the final layout of the amplifier.

Following the presented qualitative objectives, a set of circuit specifications is determined. Notice that since the developing circuit is integrated in a large industrial equipment, the power consumption is not a tight restrain to this project.

Table 1.1: Circuit Specifications

Technology	AMS 0.35 µm CMOS
Power Supply [V]	3.3
Open Loop Gain [dB]	70
Close Loop Gain [dB]	20
Bandwidth [MHz]	10
Phase Margin [º]	60
IRN @ 100Hz [$nV/\sqrt{Hz}$]	$<$20
DC Attenuation [dB]	40

1.3 Main contributions

This thesis aims the production of an amplifier with reduced flicker noise and DC attenuation to be included in an EC NDT system being developed by the working team at INESC-ID, Lisboa. A Chopper Stabilization technique is implemented to reduce flicker noise and a DC Servo Loop (DSL) is used to cancel DC components. These techniques are explored in this thesis to provide useful information for future implementations. A two page abstract ([5]) and a poster for the conference ENDE 2016 on NDT systems were produced. A full paper for inclusion in "Electromagnetic Nondestructive Evaluation" series, to be published by IOS Press, has been delivered.

1.4 Dissertation outline

This thesis is organized in 5 chapters. In this chapter, an introduction to the context of the work and proposed objectives are presented. Chapter 2 introduces and describes in more detail the EC NDT system. It also makes a theoretical review on flicker noise reduction techniques and DC cancellation. Chapter 3 makes a technical overview of this system, describing the sensor biasing and reading, as well as the considerations regarding the amplifier in focus. It also describes the designing process of the circuits proposed. Chapter 4 presents the circuit simulation results obtained and a comment on them. In Chapter 5, conclusions are drawn and future work is proposed.

2

State-of-the-art

Contents

2.1 Introduction

In this chapter, the theoretical background of this work is presented and possible solutions for the problems of the pre-amplifier of the ASIC are explored. First, the EC NDT system conceptual way of working is described, followed by a noise analysis of the devices that compose the elementary blocks of the system. Then, the techniques for flicker noise reduction are presented and an introduction to fully-differential amplifiers is made. Finally, a state-of-the-art DC suppression technique is discussed.

2.2 Eddy-current Non-destructive Testing System

An Eddy-Current (EC) Non-Destructive Testing (NDT) is an efficient metallic body inspection method used in a variety of industries to assure the quality of aircraft fuselage, welds and molds, as an example. This inspection method uses a coil conducting a current, which induces a magnetic field according to Ampère's Law [6]. For a coil, like the one used in EC NDTs, the magnitude of the magnetic field B is given by

$$B = \mu n I \tag{2.1}$$

where n is the number of turns of the coil, μ is the magnetic permeability and I the current that travels through the coil. If the current I is time-variant, the magnetic field, from now on named primary magnetic field, will also vary in time. As a consequence, a voltage is induced in the conductor material, as stated by Faraday's Law [6]. If there are any closed paths on the material, electric currents appear [7]. These currents will induce a secondary magnetic field, again according to Ampère's Law. In the presence of defects on the conductive material, the magnetic permeability μ is changed, altering the characteristics of the secondary magnetic field. If picked up by a device, using a sensing coil, these changes on the secondary magnetic field may indicate flaws on the material.

In the case of the EC NDT system of this work, the changes in the secondary magnetic field are used to detect buried or superficial defects. Figure 2.1 illustrates the process described.

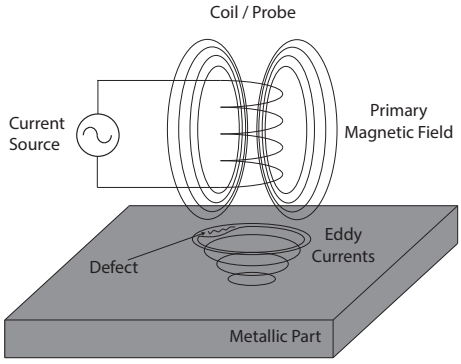


Figure 2.1: Eddy current NDT illustration.

The system of this work generates a primary magnetic field with frequency f_1, using an emitter coil. Instead of using a sensing coil, the system comprises an array of Magneto-Resistive (MR) sensors, used for defect detection, which are biased by a current of frequency f_2. These sensors present a variation in their characteristic resistance with the magnetic field applied, producing an electric signal $y(t)$ that carries the information regarding that variation. When operating in their linear region, the total sensor resistance, which is a function of the sensed magnetic field, is given by

$$R_H(t) = R_0 + \Delta R(H(f_1)) \tag{2.2}$$

where R_0 is the nominal resistance and $\Delta R(H(f_1))$ is the resistance variation as a function of the sensed magnetic field created by the ECs. Given the sensors biasing current as

$$i(t) = I_0 + I_m sin(2\pi f_2 t), \tag{2.3}$$

the signal $y(t)$ can be written as

$$\begin{aligned} y(t) = i(t).R_H(t) = R_0 I_0 + R_0 I_m \sin(2\pi f_2 t) + R_m(f_b) I_0 \sin(2\pi f_1 t) + \\ + \frac{R_m(f_b) I_m}{2} \sin(2\pi(f_1 - f_2)t) + \frac{R_m(f_b) I_m}{2} \sin(2\pi(f_1 + f_2)t) \end{aligned} \tag{2.4}$$

where f_b is the signal bandwidth required for a given inspection speed, R_m and I_m are the resistance and current variation produced by the MR sensors, respectively. This signal is the processed by an Application Specific Integrated Circuit (ASIC), which is also responsible for the biasing and multiplexing of the sensors [4]. From (2.4), the terms containing the current and resistance variation, R_m and I_m, respectively, are the ones that hold useful information regarding the presence of defects and are present at frequencies $f_1 - f_2$ and $f_1 + f_2$.

The frequencies f_1, f_2 are set by the user and they depend on the type of material under test and the speed of inspection v. The frequency of the primary magnetic field f_1 is set to achieve a desired depth of penetration δ, which is given by

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \tag{2.5}$$

where $\omega = 2\pi f_1$, μ and σ are the magnetic permeability and electric conductivity of the material under test, respectively. From (2.5), to achieve the same depth across multiple materials, ω must change accordingly. Figure 2.2(a) shows the required primary magnetic field frequency to achieve multiple depths of penetration in some metals [4]. The sensor biasing signal can be a DC, a sine or square wave signal of frequency f_2, which is also set by the user. It is chosen in such a way that $f_1 - f_2$ must be within the pre-amplifier bandwidth, so that the information regarding defects can be preserved and the signal amplified. For this work, the sensor biasing signal will be a DC signal. The signal bandwidth f_b is related to the speed of scanning v and the flaw depth, as shown in Figure 2.2(b). As an example, for a scanning speed v of 10 cm/s, to be able to detect a defect of 800 µm, a signal bandwidth f_b of about 150 kHz is required.

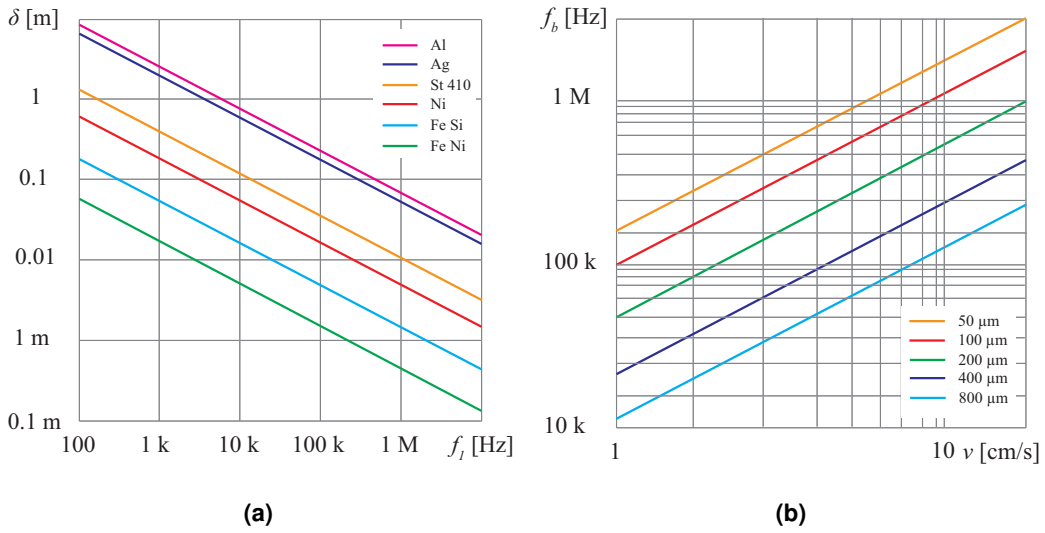


Figure 2.2: System characteristics: (a) excitation frequency for several materials and depths; (b) signal bandwidth for several scanning speeds and depths.

Figure 2.3 shows a top-level diagram of the system. It is composed by a sensor array with up to 32 MR sensors, each one producing a signal that is selected by the ASIC and then read. This selection is accomplished by a multiplexer controlled by the testing device, such as a computer. The multiplexer outputs the signal $y(t)$, described in (2.4), being amplified by the pre-amplifier included in the ASIC and fed to an Analog to Digital Converter (ADC) for digital signal processing.

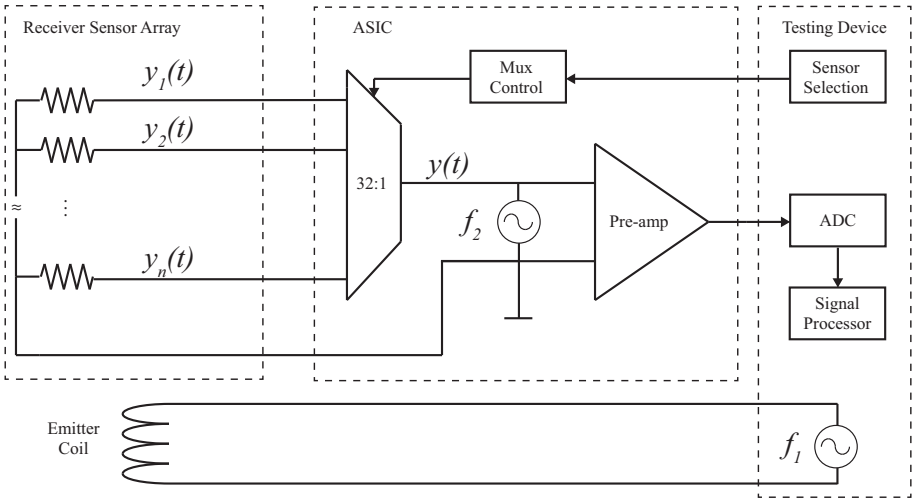


Figure 2.3: Top-level diagram of the system.

As shown in Figure 2.5, for deeper penetration on the testing material, it is required a low-frequency magnetic field, resulting in low-frequency output signals, where flicker noise is also present and can impair readings. The pre-amplifier will be addressed to tackle this problem and to block the DC biasing signal coming from the sensors that can easily saturate it.

2.3 Noise Analysis

To understand how noise can corrupt readings, there is the need to know how noise behaves and how it can be modeled, so that it can be predicted and dealt with in the design phase. First, a noise model of the Metal–Oxide–Semiconductor (MOS) transistor is defined, followed by the characterization of the noise of a Common-Source (CS) stage. The CS stage will be used as a basic block to define the noise of more complex circuits, such as the cascode stage and the differential pair. To finish, three typical Operational Transconductance Amplifier (OTA) topologies are analyzed and compared.

2.3.1 Noise in MOSFET Transistors and Single Stage Amplifiers

As the MOS transistor is the main building block of circuits in integrated electronics, it is important to define its noise model, concerning the two main noise types: thermal (white) noise and flicker (pink) noise, also called low-frequency or $1/f$ noise.

Thermal noise is caused by voltage fluctuations, originated by the random motion of electrons in a conductor. This type of noise is proportional to the absolute temperature [8], since temperature elevations cause an increase in kinetic energy of electrons, leading to an even more erratic motion, increasing the voltage fluctuations, thus increasing thermal noise. In MOS transistors, the most significant source of thermal noise is the channel. The thermal noise can be modeled as a current source connected between drain and source or as a voltage source connected to the gate, as shown if Figure 2.4.

Figure 2.4: MOS noise models: (a) as a current source; (b) as a voltage source.

According to [8] the thermal noise current $\overline{I_n^2}$ and the thermal noise voltage $\overline{V_n^2}$ are, respectively, given by

$$\overline{I_{n,thermal}^2} = \frac{2}{3} g_m (4 k_B T) \tag{2.6}$$

and

$$\overline{V_{n,thermal}^2} = \frac{2}{3} g_m (4 k_B T) r_o^2 \tag{2.7}$$

where k_B is the Boltzmann constant, T is the temperature in Kelvin, g_m and r_o are the transconductance and output impedance of the transistor, respectively.

Flicker noise is another important type of noise and occurs due to trapping of charges in the interface between the silicon substrate and the gate oxide. When these charges are released, they add a contribution to the drain current in the form of noise. This phenomenon happens more often at low frequencies, therefore being also called $1/f$ noise [8]. The flicker noise current $\overline{I_{n,flicker}{}^2}$ and flicker noise voltage $\overline{V_{n,flicker}{}^2}$ are respectively given by

$$\overline{I_{n,flicker}{}^2} = \frac{K}{C_{OX}WL}\frac{1}{f}g_m^2 \tag{2.8}$$

and

$$\overline{V_{n,flicker}{}^2} = \frac{K}{C_{OX}WL}\frac{1}{f} \tag{2.9}$$

where K is the flicker noise parameter, that depends on the process and the type of transistor (p-type or n-type), C_{OX} is the capacitance per unit area of the gate oxide, W and L are the width and length of the channel, respectively.

Noise of a Common-source Stage

Given the noise model for a MOS transistor, it is important to analyze a basic and common circuit used in amplifiers. It is the case of the CS stage of Figure 2.5(a).

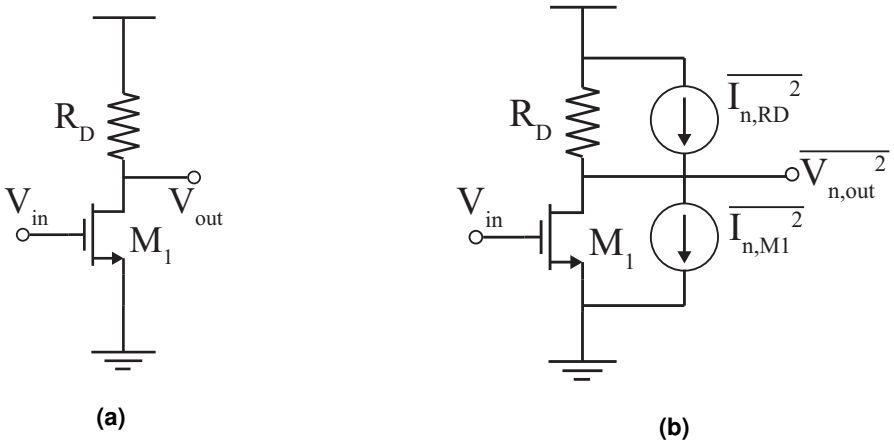


Figure 2.5: Common-source stage noise: (a) without noise sources; (b) with noise sources.

From Figure 2.5(b) the total output noise current can be written as the sum of the individual noise contributions of the components:

$$\overline{I_{n,out}{}^2} = \frac{2}{3}g_m(4k_BT) + \frac{K}{C_{OX}WL}\frac{1}{f}g_m^2 + \frac{4k_BT}{R_D}, \tag{2.10}$$

where R_D is the drain resistor. Consequently, the total output noise voltage $\overline{V_{n,out}{}^2}$ is found by multiplying the output noise current $\overline{I_{n,out}{}^2}$ by R_D^2. As the output noise depends on the gain of the circuit, a normalization to noise is appropriate for better comparison between different circuits. For this reason the concept of Input-Referred Noise (IRN) is introduced. The IRN allows the effects of all noise sources of a circuit to be represented as a single noise voltage source at the input of the

circuit. In order to be independent of the gain of the circuit, the IRN is found by taking the output noise voltage and divide it by the gain, which in this case is given by

$$\begin{aligned}\overline{V_{n,in}^2} &= \frac{\overline{V_{n,out}}^2}{A_v^2} \\ &= \left(\frac{2}{3}g_m(4k_BT) + \frac{K}{C_{OX}WL}\frac{1}{f}g_m^2 + \frac{4k_BT}{R_D}\right)R_D^2\frac{1}{g_m^2R_D^2} \\ &= \frac{2}{3g_m}(4k_BT) + \frac{K}{C_{OX}WL}\frac{1}{f} + \frac{4k_BT}{g_m^2R_D}\end{aligned} \tag{2.11}$$

From (2.11) it is noticeable that to reduce the overall IRN, the dimensions of the transistor should be increased, as well as its transconductance. As can be noticed, the last term of the sum is the noise contribution of the resistor R_D.

Noise of a Cascode Stage

As for the cascode stage, in Figure 2.6(a), the noise contribution of M_2 can be modeled as a voltage source (Figure 2.6(b)). In this view, the circuit can be seen as a CS with a source resistor r_{o1}, which is the output resistance of M_1. Thus, the gain of M_2 is given by $g_{m2}R_D/(1 + g_{m2}r_{o1})$ [9]. If the output resistance of M_1 is large, then the gain of M_2 is reduced and is much smaller than the gain seen from the gate of M_1. Since the noise voltage $\overline{V_n^2}$ is much less amplified than the actual input signal V_{in}, noise contributions of cascode transistors are neglected.

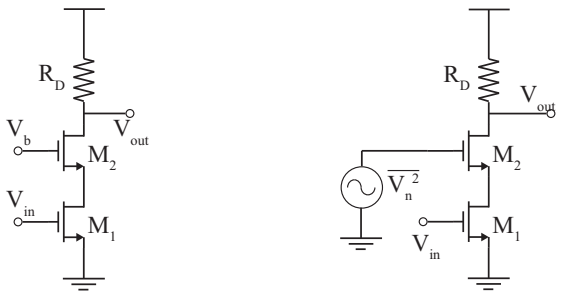
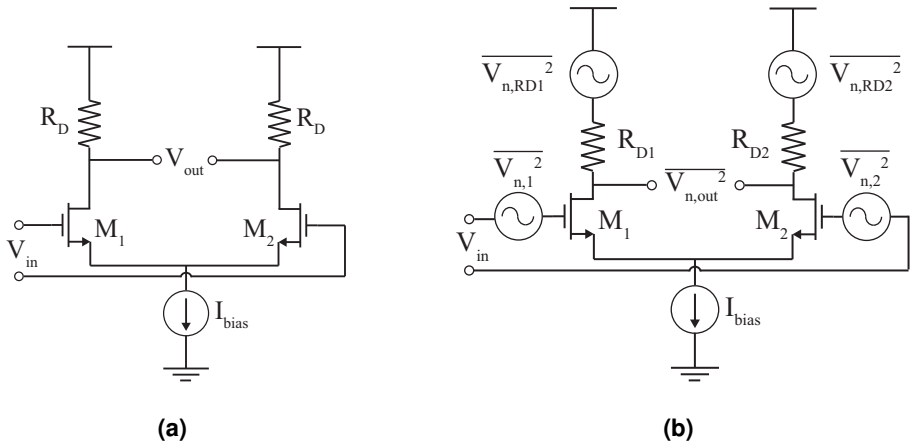


Figure 2.6: Cascode stage noise: (a) Cascode stage; (b) Noise modeled by voltage source.

Noise of a Differential Pair

Another important circuit in this study is the differential pair with resistive load (Figure 2.7). In Figure 2.7(b) the noises of M_1 and M_2 are modeled by two voltage sources placed at the gate of each transistor. The resistors are also modeled by two voltage sources. Notice that each branch of the differential pair can be seen as a CS stage with a total IRN given by (2.11). Therefore, for matched transistors, the total IRN of the differential pair is twice the IRN of a CM stage:

$$\overline{V_{n,in,total}^2} = 2\left(4k_BT\left(\frac{2}{3g_m} + \frac{1}{g_m^2R_D}\right) + \frac{K}{C_{OX}WL}\frac{1}{f}\right). \tag{2.12}$$



(a) **(b)**

Figure 2.7: A differential pair: (a) without noise sources; (b) with noise sources.

As seen in CS stages, to reduce thermal noise in a differential pair, the transconductance g_m of the transistors should be increased. Since

$$g_m = \frac{2I_D}{V_{OD}} = \sqrt{2K_{N,P}\frac{W}{L}I_D}, \tag{2.13}$$

where $K_{N,P}$ is the gain factor and V_{OD} is the overdrive voltage of the transistor, for the same transistor area and current, the choice of an NMOS transistor over a PMOS transistor leads to smaller thermal noise. As K_N has a value of 170 µA/V^2 and K_P has a value of 58 µA/V^2 in the AMS 0.35 µm CMOS process, the relation between the thermal noise contribution of an NMOS and the thermal noise contribution of a PMOS is given by

$$\frac{\overline{V_{n,NMOS}^2}}{\overline{V_{n,PMOS}^2}} = \sqrt{\frac{K_P}{K_N}} \approx \frac{1}{\sqrt{3}}. \tag{2.14}$$

In spite of having a smaller thermal noise contribution, NMOS transistors have a higher flicker noise corner frequency f_k, which is defined as the frequency where the flicker Power Spectral Density (PSD) equals the thermal noise PSD. This is a problem, since for the same frequency, the flicker noise contribution of an NMOS is higher. As the goal of this work is to mitigate flicker noise, a PMOS differential pair for the amplifier will be implemented, because the flicker noise contribution is smaller, despite having an higher thermal noise contribution, which can be managed by careful design, as described in the following subsection.

2.3.2 Noise in Operational Transconductance Amplifiers

Operational Transconductance Amplifiers (OTAs) are widely used amplifiers as they provide very high gains, large bandwidths and can achieve good noise performances. For these reasons, an OTA will be implemented as the pre-amplifier of the ASIC. Here the three main topologies are analyzed, namely telescopic, mirrored and folded cascode, regarding their noise. In this analysis, only thermal noise is taken into account, as flicker noise mitigation will be covered ahead.

Telescopic OTA

The IRN of the telescopic OTA (Figure 2.8) can be found by summing the thermal noise current contributions of each transistor to the output [10]. The total thermal noise current contribution to the output is given by

$$\overline{I_{n,out}^2} = 4k_BT\left[2\left(\frac{2}{3}g_{m1,2}\right) + 2\left(\frac{2}{3}g_{m9,10}\right)\right] \tag{2.15}$$

where k_B is the Boltzmann constant, T is the temperature in Kelvin and g_m is the transconductance of the transistor. Notice that transistors M_{5-8} have a negligible contribution to the thermal noise, since they are cascode stages (subsection 2.3.1). As for transistors $M_{3,4}$, the noise current generated by them is seen by the differential pair as a Common-Mode (CM) signal, hence is greatly attenuated, giving the differential nature of the amplifier. The IRN voltage of the amplifier is

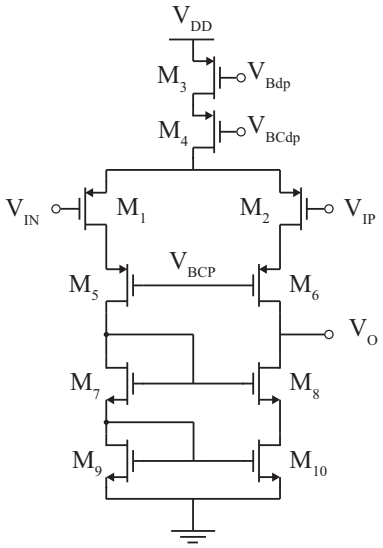


Figure 2.8: Telescopic OTA.

obtained by dividing the total noise current contribution, (2.15), by the squared transconductance of $M_{1,2}$:

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{g_{m1,2}^2} = 16\frac{k_BT}{3g_{m1,2}}\left(1 + \frac{g_{m9,10}}{g_{m1,2}}\right). \tag{2.16}$$

Since the transconductance of a transistor is given by

$$g_m = \frac{2I_D}{V_{OD}}, \tag{2.17}$$

where I_D is its drain current and V_{OD} is its overdrive voltage, (2.16) is rewritten as

$$\overline{V_{n,in}^2} = 16\frac{k_BT\,V_{OD1,2}}{3I_{D3}}\left(1 + \frac{1}{A_1}\right), \tag{2.18}$$

where A_1 is given by

$$A_1 = \frac{V_{OD9,10}}{V_{OD1,2}}. \tag{2.19}$$

From (2.18) and (2.19), to reduce the IRN, the overdrive voltage of transistors $M_{1,2}$, $V_{OD1,2}$, should be lower than the overdrive voltage of $M_{9,10}$, $V_{OD9,10}$.

Mirrored OTA

By applying the same principles to the mirrored OTA (Figure 2.9), its total noise current contribution to the output of is given by

$$\overline{I_{n,out}^2} = 4k_BT\left[2\left(\frac{2}{3}g_{m1,2}n^2\right) + 2\left(\frac{2}{3}g_{m5,6}n^2\right) + 2\left(\frac{2}{3}g_{m7,8}\right) + \left(\frac{2}{3}g_{m13,14}\right)\right] \tag{2.20}$$

where n is the current gain of the current mirrors formed by M_{5-8}. Once again, cascode transistors (M_{9-12}) have a negligible noise contribution. Transistors $M_{3,4}$ also do not contribute to the noise because the noise current they generate is seen as a CM signal by the differential pair.

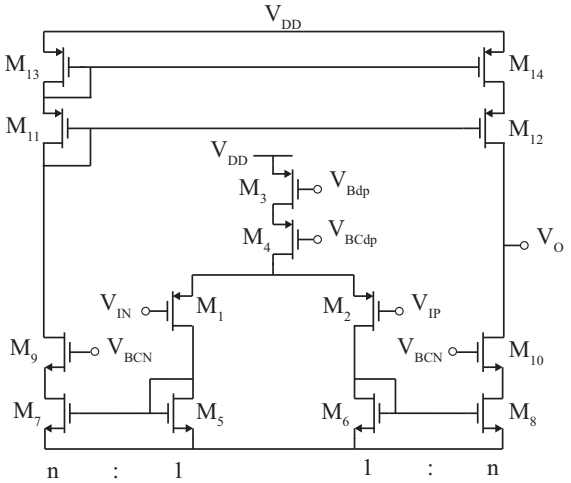


Figure 2.9: Mirrored OTA.

The total IRN is then given by

$$\begin{aligned}\overline{V_{n,i}^2} = \frac{\overline{I_{n,out}^2}}{g_{m1,2}^2n^2} &= \frac{16k_BT}{3g_{m1,2}}\left(1 + \frac{g_{m5,6}}{g_{m1,2}} + \frac{g_{m7,8}}{g_{m1,2}^2n^2} + \frac{g_{m13,14}}{g_{m1,2}^2n^2}\right) \\ &= \frac{16k_BT\,V_{OD1,2}}{3I_{D3}}\left(1 + \frac{1}{A_2} + \frac{1}{B_2n} + \frac{1}{C_2n}\right)\end{aligned} \tag{2.21}$$

where A_2, B_2 and C_2 are, respectively, given by

$$A_2 = \frac{V_{OD5,6}}{V_{OD1,2}} \qquad B_2 = \frac{V_{OD7,8}}{V_{OD1,2}} \qquad C_2 = \frac{V_{OD13,14}}{V_{OD1,2}} \tag{2.22}$$

To reduce the total IRN, parameters A_2, B_2 and C_2 should be increased, that is the overdrive voltage of the transistors $M_{1,2}$, $V_{OD1,2}$, should be lower than $V_{OD5,6}$, $V_{OD7,8}$ and $V_{OD13,14}$, respectively. Also the current gain n can be increased to reduce the noise, implicating a higher power consumption.

Folded Cascode OTA

Figure 2.10 shows the schematic of a folded cascode OTA, the last of the three topologies to be analyzed. In a similar manner, its total noise current contribution to the output is found by summing the individual noise current contributions of each transistor, therefore

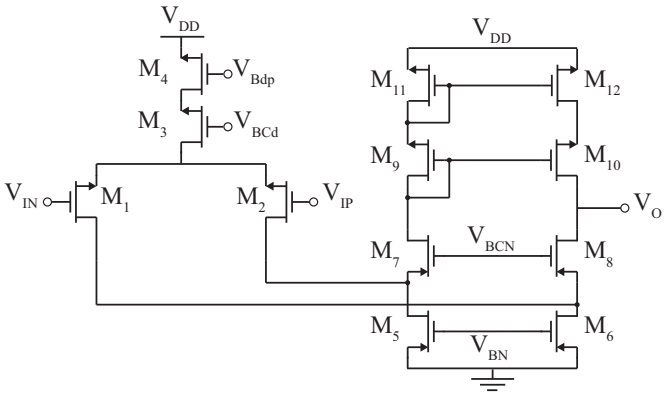


Figure 2.10: Folded Cascode OTA.

$$\overline{I_{n,out}^2} = 4k_BT\left[2\left(\frac{2}{3}g_{m1,2}\right) + 2\left(\frac{2}{3}g_{m5,6}\right) + \left(2\frac{2}{3}g_{m11,12}\right)\right]. \tag{2.23}$$

Noise, the IRN is given by

$$\begin{aligned}\overline{V_{n,i}^2} = \frac{\overline{I_{n,out}^2}}{g_{m1,2}^2} &= \frac{16k_BT}{3g_{m1,2}}\left(1 + \frac{g_{m5,6}}{g_{m1,2}} + \frac{g_{m11,12}}{g_{m1,2}}\right) \\ &= \frac{16k_BT\,V_{OD1,2}}{3I_{D3}}\left(1 + \frac{C_3 - 1}{A_3} + \frac{C_3}{B_3}\right)\end{aligned} \tag{2.24}$$

where A_3, B_3 and C_3 are, respectively, given by

$$A_3 = \frac{V_{OD5,6}}{V_{OD1,2}} \qquad B_3 = \frac{V_{OD11,12}}{V_{OD1,2}} \qquad C_3 = \frac{2I_{D11}}{I_{D3}}. \tag{2.25}$$

From (2.24) and (2.25) it is clear that to minimize the noise A_3 and B_3 must be maximized. The current flowing through the cascode transistors should be lower than the current flowing through the differential pair, making C_3 slightly higher than unity.

OTA Comparison

In [10] the same analysis is made and values are added to the parameters $A_{1,2,3}$, $B_{2,3}$ and $C_{2,3}$, in order to quantify the IRN and total current of the three topologies. The same supply voltages and amplifier tail current I_{D3} are used.

As seen, in the telescopic amplifier, $V_{OD1,2}$ must be lower than $V_{OD9,10}$, making A_1 larger than unity. In [10] is set to five. For the mirrored amplifier, A_2, B_2 and C_2 follow the same principle as for A_1, and they also set to five. In order not to penalize the total current relatively to the other topologies, the current gain n is set to one. As for the folded cascode, A_3 is set to three, B_3 is set to five and C_3 is set to 5/4, making the tail current four times larger than the one of the cascode transistors, that is $I_{D3} = 4I_{D9}$.

As seen, the differential pairs of the amplifiers reviewed have a thermal noise contribution of

$$\overline{V_{n,dpair}^2} = \frac{16k_BT\,V_{OD1,2}}{3I_{D3}} \tag{2.26}$$

and, in order to compare the three topologies, the normalized thermal noise in respect to $\overline{V_{n,dpair}^2}$ is introduced as

$$\overline{V_{n,normalised}^2} = \frac{\overline{V_{n,OTA}^2}}{\overline{V_{n,dpair}^2}} \tag{2.27}$$

where $\overline{V_{n,OTA}^2}$ is the total thermal noise of each OTA topology. Table 2.1 presents the comparison of the three topologies, made in [10], in terms of normalized noise and total current, for the same technology and power supply.

Table 2.1: OTA comparison.

	Normalized Noise	Total Current
Telescopic	1.2	I_{D3}
Mirrored	1.6	$2I_{D3}$
Folded Cascode	1.3(3)	$1.25I_{D3}$

The telescopic OTA achieves the best performance, having the lowest noise and total current, while the mirrored OTA has the worst noise performance and the highest power consumption. Although the folded cascode achieves worse noise performance and has a higher power consumption than the telescopic OTA, it will be the chosen amplifier to implement in the NDT system, since its noise performance is just slightly worse and, in order to polarize the transistors in the output rail into saturation region, a higher voltage is needed in the telescopic, leaving a smaller headroom voltage. Also, the power consumption for this work is not a major concern.

2.4 Flicker Noise Suppression

In the previous section, it was shown that the thermal noise of three main OTA topologies can be mitigated by increasing the overdrive voltages of the differential pairs and by increasing the tail currents. However, this approach does not reduce flicker noise. As seen, flicker noise is inversely proportional to the frequency f, meaning that when there is the need to process weak and low-frequency signals, these are greatly affected by flicker. To suppress flicker noise two widely used techniques may be employed: Autozero and Chopper Stabilization. Both of them will be described in the following subsections.

2.4.1 Autozero

The basic principle behind the Autozero is to sample the noise and/or offset at the output of the amplifier and subtract it from the signal [11]. As seen in Figure 2.11, this method contemplates two phases. In the first phase, ϕ_1, switch S short-circuits the input of the amplifier and by doing so, the only quantities appearing at its output are the noise and offset, $V_{N,OS}(t)$. Then, this offset and noise are sampled by the Sample & Hold (S&H) block. In phase ϕ_2, S switches back to the signal and the voltage stored in the S&H is applied to the amplifier (N), thus subtracting it to the signal.

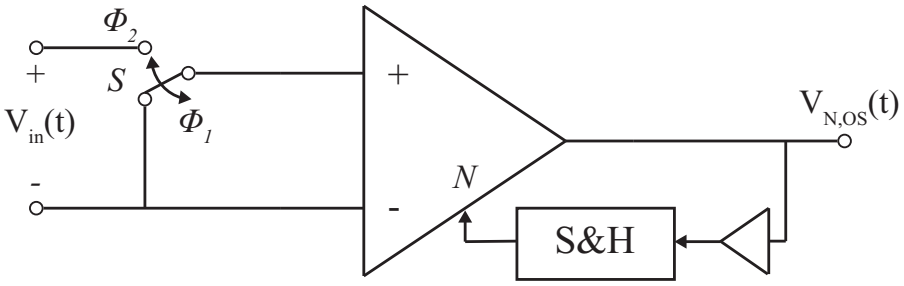


Figure 2.11: Basic Autozero implementation.

Following the principle described, during phase ϕ_1, the output of the circuit in Figure 2.11 only contains a near DC signal component, $V_{N,OS}(t)$, that describes the output flicker noise and offset. At the sampling instant, t_1, $V_{N,OS}(t_1)$ is stored in the S&H and applied to the amplifier in the instant t_2, to subtract it from $V_{N,OS}(t_2)$. As the component $V_{N,OS}(t)$ is near DC, during an infinitesimal time interval $\Delta t = t_2 - t_1$, the voltage $V_{N,OS}$ will approximately keep a constant value ($V_{N,OS}(t_1) \approx V_{N,OS}(t_2)$), which means that when the sampled voltage is applied to the amplifier, a near perfect noise and offset cancellation is achieved, theoretically.

However, real amplifiers have a larger bandwidth flicker noise component $V_{N,OS}(t)$, thus the quantity sampled by the S&H block ($V_{N,OS}(t_1)$) and the quantity to be subtracted ($V_{N,OS}(t_2)$) can be different. This results in an imperfect noise cancellation. In addition, real amplifiers also have a thermal noise (or white noise) component that is constant across the spectrum and a low-pass characteristic with a cut-off frequency f_{-3dB}. Since the sampling frequency f_S is lower than the amplifier cut-off frequency f_{-3dB}, the system suffers from undersampling leading to aliasing that increases the overall noise of the amplifier [11].

The efficiency of this process is as high as the correlation between the quantity sampled by the S&H, $V_{N,OS}(t_1)$, and the instantaneous noise value to be subtracted, $V_{N,OS}(t_2)$. As this correlation between two samples of flicker noise/offset, separated by a time interval Δt, decreases slower for an increasing Δt than it does for thermal noise [11], for time-varying random noise, Autozero has an high-passing effect over the noise, resulting in a flicker noise attenuation. However, since Autozero is a sampling-based technique, it introduces aliasing which increases the noise floor of the signal. Also, the voltage stored in the S&H block may suffer from errors, namely quantization errors (when the sampling block is implemented using ADCs and/or Digital to Analog Converters (DACs)) or leakage currents (when using capacitors for sampling).

2.4.2 Chopper Stabilization

Chopper Stabilization is a flicker noise reduction technique that uses modulation to shift the spectrum of the signal to high frequencies, where the flicker noise contribution is negligible, and then, after amplification, the signal is demodulated back to its baseband, while flicker is up-modulated. Figure 2.12 shows a diagram describing the general Chopper Stabilization process.

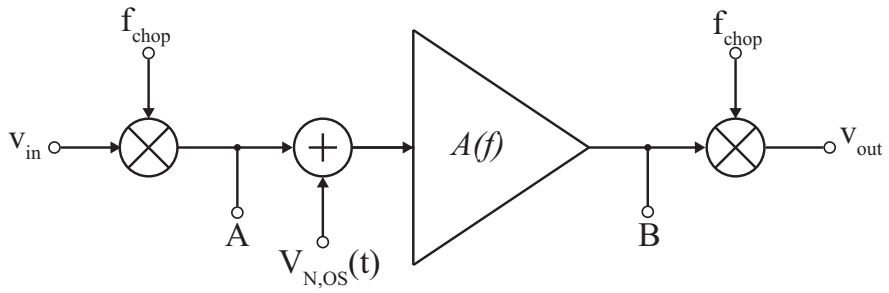


Figure 2.12: Diagram of chopper stabilization.

Let the input signal be a DC voltage, V_{in} (Figure 2.13(a)). This signal is modulated by a square wave carrier of frequency f_{chop} and unitary amplitude, that results in a square wave of the same frequency and amplitude V_{in} (Figure 2.13(a)). After modulation, the IRN and offset of the amplifier (represented by $V_{N,OS}(t)$) are added. After being amplified, the output of the amplifier (Figure 2.13(b)) is, a square wave with amplitude $A_0.V_{in}$ (if the amplifier is ideal, i.e. with infinite bandwidth and DC gain A_0).

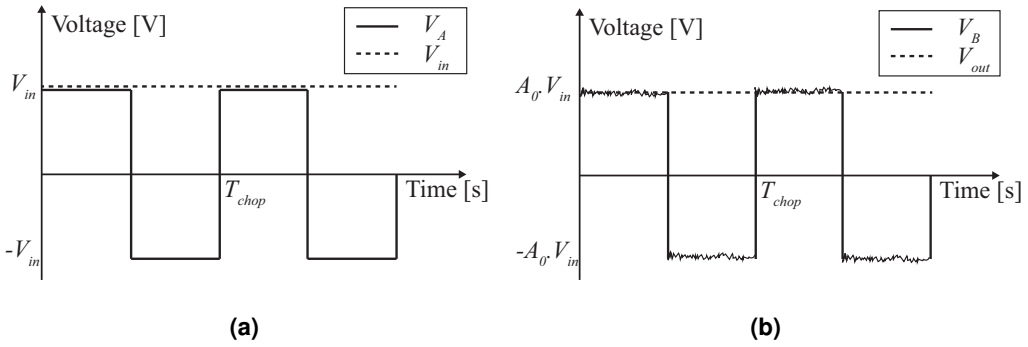


Figure 2.13: Signals along the Chopper Stabilization circuit diagram (Figure 2.12): (a) V_{in} and V_A; (b) V_B and V_{out}

Figure 2.14 shows the spectra of the signals along the signal path of the chopper circuit (Figure 2.12). Suppose the signal V_{in}, which has a spectrum represented on Figure 2.14(a), is modulated by the referred carrier. The resulting signal, V_A, (Figure 2.13(a)) has a spectrum that is composed by replicas of the spectrum of the input signal V_{in}, centered on odd multiples of the carrier frequency f_{chop} (Figure 2.14(b)), since the carrier is a square wave, with only odd harmonics. The modulated signal is then exposed to noise and amplified, before it is demodulated, resulting in signal V_B (Figure 2.13(b)), with a spectrum represented in Figure (2.14(c)). Demodulation is accomplished by using the same carrier wave, as before. This time, the flicker noise component is shifted to the odd harmonics of the carrier and the spectrum of the signal returns to its baseband (Figure 2.14(d)). The resulting signal can be, afterwards, low-pass filtered in order to eliminate the unwanted quantities present at the odd multiples of the chopper frequency f_{chop}, if necessary.

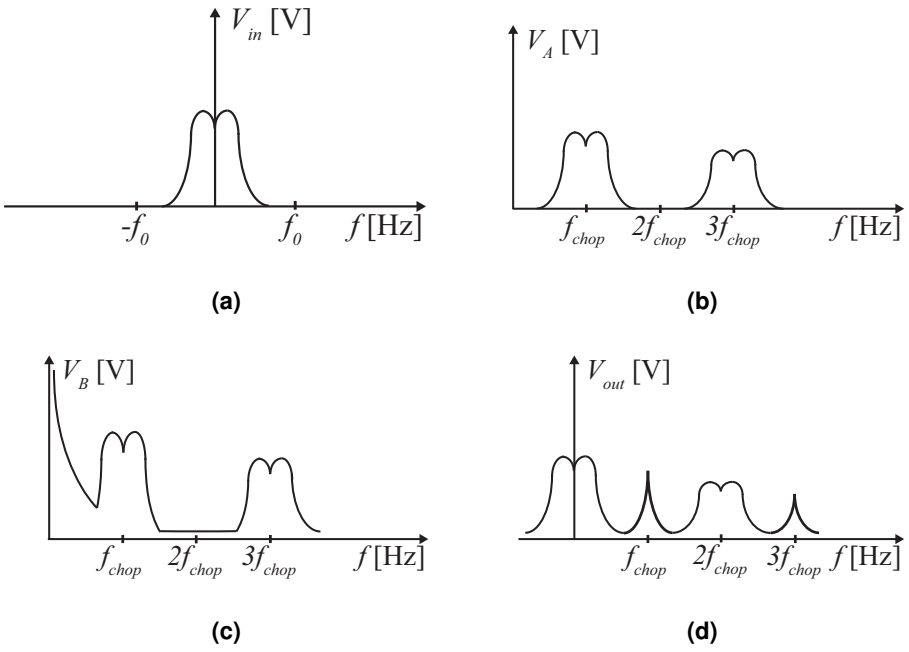


Figure 2.14: Spectra of signals at several stages of chopper stabilization process: (a) input signal; (b) signal after the first modulation; (c) signal after amplification; (d) output signal.

As seen, Chopper Stabilization is a fully-analog technique that uses modulation to shift flicker noise to an high frequency, where it does not overlap with signal spectral components, thus it can be filtered out afterwards. Unlike Autozero, that is a sampling-based technique, Chopper Stabilization does not introduce aliasing that increases the noise floor [11] and does not need complex sampling circuits. For these reasons, Chopper Stabilization is the technique chosen to implement on the folded cascode amplifier, that will compose the pre-amplifier block of the ASIC. Therefore, a further analysis on this technique is made, regarding its effects on baseband noise and how the modulations are performed.

Effect of Chopper in Baseband Noise

Chopper Stabilization does not introduce aliasing, however, it has important effects on the noise Power Spectral Density (PSD), in baseband. The PSD of the chopped output signal V_{out} can be written as

$$S_{out}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n\ odd}}^{+\infty} \frac{1}{n^2} S_N\left(f - \frac{n}{T_{chop}}\right) \tag{2.28}$$

where n is the number of the signal harmonic, S_N is the PSD of a stationary random noise and T_{chop} is the period of the chopper carrier, according to [11]. For the sum of the replicas of the spectrum shifted to the harmonics $n = -3, -1, 1, 3$ and for an amplifier with cut-off frequency f_{-3dB} equal to five times the chopper frequency $f_{chop} = 1/T_{chop}$, (2.28) can be approximated in

the baseband ($|f| \leq 0.5 f_{chop}$) by a white noise PSD

$$\begin{aligned} S_{out-white}(f) &\cong S_{out-white}(f=0) \\ &= S_0 \left[1 - \frac{\tanh\left(\frac{\pi}{2} f_{-3dB} T_{chop}\right)}{\frac{\pi}{2} f_{-3dB} T_{chop}} \right], \end{aligned} \tag{2.29}$$

which simplifies in

$$S_{out-white} \cong S_0 \quad \text{for } |f| \leq 0.5 f_{chop} \text{ and } f_{-3dB} \gg f_{chop}, \tag{2.30}$$

where S_0 is the input thermal noise PSD [11]. The effect of Chopper Stabilization on flicker noise can be derived from (2.28), considering $f_{-3dB} \gg f_{chop}$ and an input PSD given by

$$S_{N-flicker}(f) = S_0 \frac{f_k}{|f|}, \tag{2.31}$$

where f_k is the flicker noise corner frequency defined as the frequency where the flicker PSD equals the white noise PSD. Again, the output flicker noise contribution PSD can be approximated by a white noise component:

$$S_{out-flicker}(f) \cong 0.8525 S_0 f_k T. \tag{2.32}$$

Hence, the total noise contribution is found by summing (2.30) and (2.32):

$$S_{out}(f) \cong S_0(1 + 0.8525 f_k T_{chop}) \quad \text{for } |f| \leq 0.5 f_{chop} \text{ and } f_{-3dB} \gg f_{chop}. \tag{2.33}$$

Chopper Stabilization is used to shift most of the flicker noise PSD out of baseband. However, it slightly increases the noise PSD in baseband. From (2.33), it can be noticed that the output noise PSD, in baseband, is approximated by a constant white noise, proportional to the input PSD S_0. It also has a contribution proportional to the flicker corner frequency f_k and inversely proportional to the chopper frequency f_{chop}, which means that if f_{chop} is made, for example, equal to the flicker noise corner frequency f_k, the output noise PSD, in baseband, is approximately equal to twice the input PSD S_0. For this reason, f_k should be reduced and f_{chop} increased, which will result in an almost constant output PSD, with a value approximately equal to the input PSD S_0.

Chopper Modulation

After analyzing how Chopper Stabilization works and its effects on noise in baseband, the way modulation is performed in practice is explained and important concerns regarding this process are presented.

As referred, for Chopper Stabilization to work, the input and output signals of the amplifier must be modulated in amplitude. This is accomplished by chopper modulators that use a square wave, of frequency f_{chop} and unitary amplitude, as a carrier, which is shaped by the input signal. The modulator output signal is then the multiplication of the input signal by the carrier, which,

from Figure 2.13, can be seen as a periodical inversion of the input signal, with frequency f_{chop}. Internally, chopper modulators are simple circuits composed by two pairs of switches, triggered by opposite clock phases (Figure 2.15(a)). They also have two input and two output terminals that allow differential signals to be switched, creating the referred periodical inversion of the input signal, to achieve its modulation.

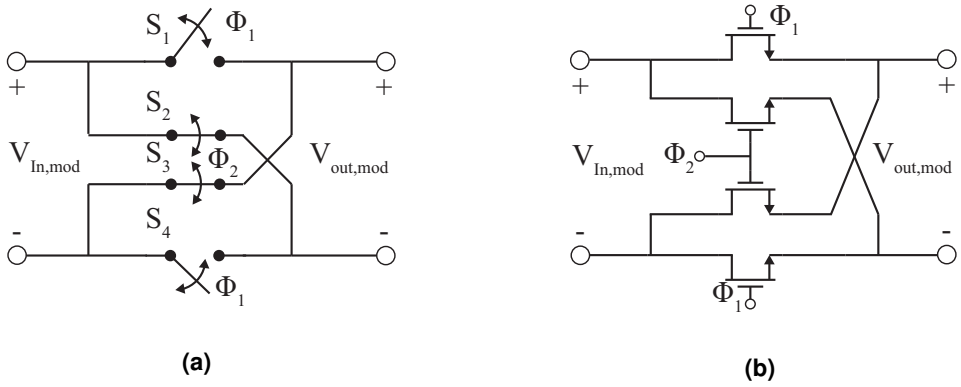


Figure 2.15: Representation of a chopper modulator:
(a) ideal switches; (b) switches implemented as NMOS transistors.

Consider the input, $V_{in,mod}$, and the output, $V_{out,mod}$ signals to be differential ones, that is $V_{in,mod} = V_{in,mod+} - V_{in,mod-}$ and $V_{out,mod} = V_{out,mod+} - V_{out,mod-}$. During phase ϕ_1, switches S_1 and S_4 are closed and the remaining are opened, making $V_{in,mod+} = V_{out,mod+}$ and $V_{in,mod-} = V_{out,mod-}$, therefore, $V_{out,mod} = V_{in,mod}$. On the next phase, ϕ_2, switches S_2 and S_3 are now closed, while S_1 and S_4 are opened, making $V_{in,mod+} = V_{out,mod-}$ and $V_{in,mod-} = V_{out,mod+}$, leading to $V_{out,mod} = -V_{in,mod}$, and, consequently, to the desired signal V_A, shown in Figure 2.13(a). The switches used to modulate the signals are usually simple MOS transistors, as seen in Figure 2.15(b).

The usage of single transistors often lead to some problems, like charge injection [11], which is a phenomenon that occurs at the interruption of the channel of the MOS transistor as it enters cut-off region. As the channel is constituted by moving charges, upon entering cut-off region, the channel is interrupted and these charges are split, flowing to the drain and source terminals. The charge splitting is not uniform, as it depends on the impedance at each one of these terminals. Furthermore, the amount of charge injected is proportional to the parasitic capacitances of the transistor, that depend on its area, meaning that larger transistors will have more charges injected [11]. In this particular application, charge injection may lead to residual offsets and increased IRN, if the charges are injected into high impedance nodes, such as the inputs of an amplifier.

The usage of single MOS transistors as switches also lead to reduced signal input swing as both NMOS and PMOS transistors are not capable of being ”ON” during all the voltage range, resulting in signal distortion. To understand how the use of a single MOS transistor can have limited voltage swing, consider an NMOS operating as a switch with a load capacitor (Figure

Figure 2.16: Circuits for determining the dynamic range of switches: (a) NMOS switch; (b) PMOS switch.

2.16(a)). If at a given moment, t_0, V_{out} is low (defined as 0 V) and the input, V_{in}, transits from low to high (V_{DD} V), the transistor is "ON" while the gate to source voltage is higher than the threshold voltage, that is $V_{GS} > V_{THn}$. Since $V_{GS} = V_{DD} - V_{out}$, the transistor will remain "ON" until the output reaches $V_{DD} - V_{THn}$, thus not being able to pass a true "1" digital value to the output. In a similar way, a PMOS transistor is not able to pass a true "0" digital value to the output. Consider now the circuit of Figure 2.16(b), where, at t_0, the output is high and the input is transitioning from high to low. Given this, the transistor will be "ON" while $V_{SG} > V_{THp}$. As $V_{SG} = V_{out} - 0$, the transistor will remain "ON" until the output reaches V_{THp}. To overcome the problem of charge injection and increase the input swing of switches, modifications to the modulator of Figure 2.15(b) are proposed.

Switches for Chopper Modulators

To reduce the effects of charge injection, shorted half-sized dummy transistors are added to the drain and source of the main transistor (Figure 2.17(a)) and triggered with a clock phase opposite to the one of the main switch (Figure 2.17(b)). When the main switch turns off and interrupts its channel, the charges that compose it leave the transistor through the drain and source. At the same time, the dummy switches are switching on, thus they are attracting the charges injected by the main transistor to compose their channel. This way, the amount of charges injected into the high impedance nodes is reduced.

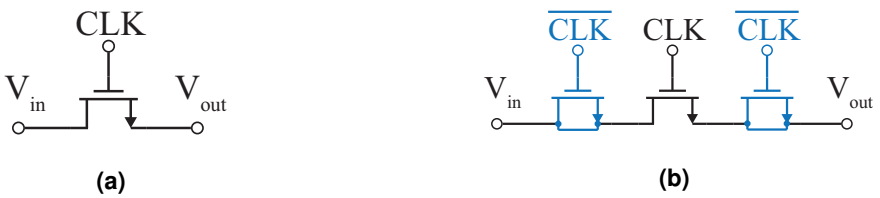
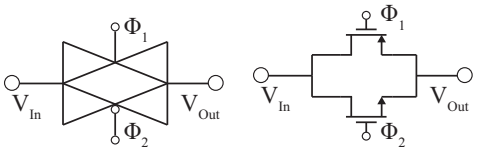


Figure 2.17: Modulator switch implemented as a: (a) NMOS transistor; (b) NMOS transistor with half-sized dummies.

To increase signal input swing Transmission Gates (TGs) can be used. The TG is a form of switch composed by a PMOS transistor and a NMOS transistor in parallel, triggered by opposite

clock phases, as shown in Figure 2.18(a). This configuration achieves good pull-up and pull-down performances, just like in the inverter circuit [9], increasing the input signal swing.



(a) **(b)**

Figure 2.18: Transmission Gate: (a) circuit; (b) symbol.

The ”ON” resistance is defined as the source-to-drain resistance of the transistor, when it works as a turned on switch. It is an important parameter as high ”ON” resistances cause significant voltage drops that may lead to significant signal losses, if the switch is place on the signal path. By combining NMOS and PMOS in parallel, an almost constant ”ON” resistance of the switch is achieved, as seen in Figure 2.19, leading to smaller voltage drops across terminals and smaller power losses.

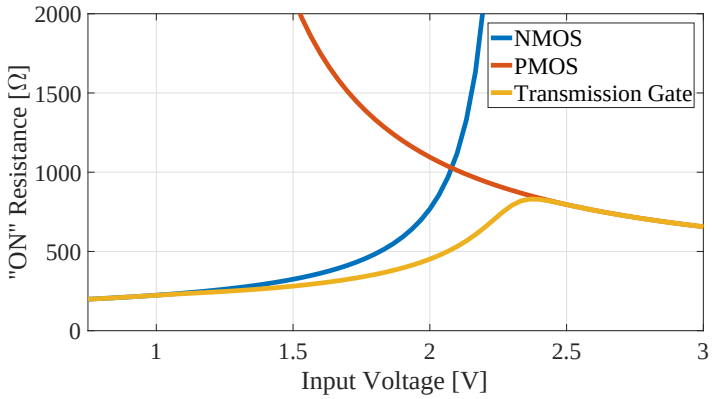


Figure 2.19: ”ON” resistance of a NMOS, PMOS and a TG. Both NMOS and PMOS results were simulated for $W/L = 10/0.35$. The TG results were calculated using data of the other two curves.

Half-sized shorted dummy switches are added to the drain and source terminals of the transistors of the TGs, to place an equal parasitic capacitance in those terminals, to achieve an equal charge splitting at the ”ON” and ”OFF” transitions, reducing the effects of charge injection introduced by the TGs [10], which may be larger than with single transistor configurations. For these reasons, switches composed by dummy compensated TGs are chosen to implement the modulators used in Chopper Stabilization.

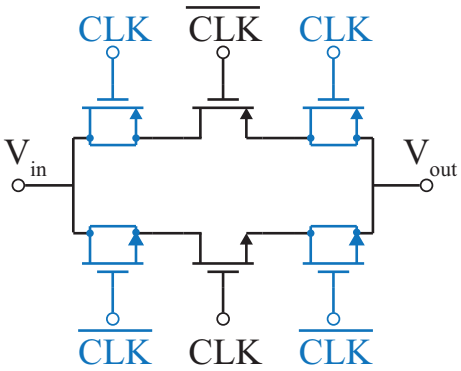


Figure 2.20: TG with half-sized dummy transistors.

2.5 Fully-differential Amplifiers and Common-mode Feedback

As referred in Section 2.4 the usage of Chopper Stabilization to reduce flicker noise, requires the addition of modulators to the circuit. Since the modulators are differential circuits, the pre-amplifier of the ASIC will be implemented as a fully-differential folded cascode amplifier. For this reason, fully-differential amplifiers are here covered.

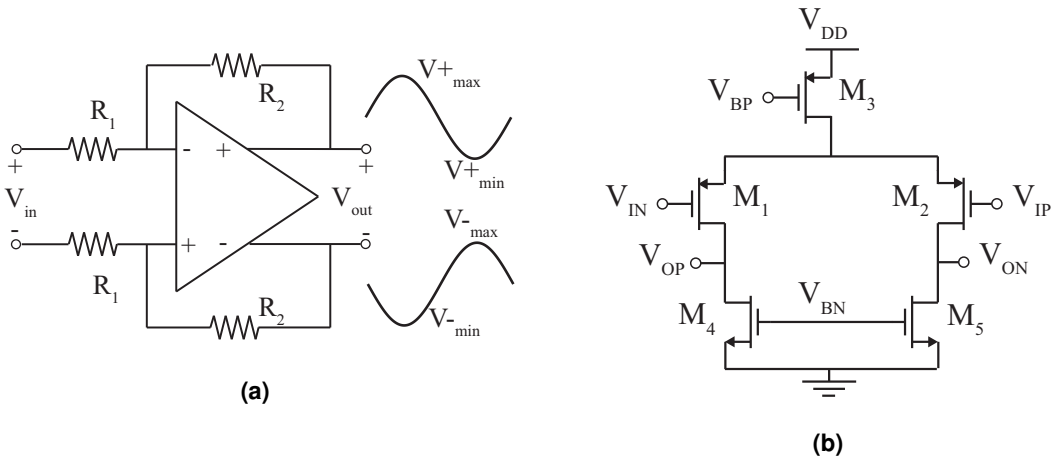


Figure 2.21: Example of: a) an inverting fully-differential amplifier with resistive feedback; b) transistor level implementation of the amplifier.

The major difference of fully-differential amplifiers relies on the fact that a differential signal is seen as the difference of two individual signal components, (non-inverting, $V_{signal+}$, and inverting, $V_{signal-}$, components), that is $V_{signal} = V_{signal+} - V_{signal-}$. Therefore, fully-differential amplifiers have two inputs and two outputs, thus requiring two feedback networks, as seen in Figure 2.21. Also, fully-differential amplifiers have twice the output swing of its single-ended counterpart [12].

Let the amplifier input be a sine wave. Its non-inverting and inverting outputs are also sine waves, but with opposite phases (Figure 2.21(a)). If the output of a singled-ended amplifier swings up to V_{max} and down to V_{min}, its output peak-to-peak maximum value is given by $V_{max} - V_{min}$.

In a differential amplifier, a single output (inverting or non-inverting) also swings up to $V+_{max}$ and down to $V-_{min}$, leading to the same peak-to-peak voltage $V_{max} - V_{min}$. However, since the output is differential ($V_{out} = V_{out+} - V_{out-}$) and V_{out+} and V_{out-} are in phase opposition, the maximum differential output voltage is $2(V_{max} - V_{min})$. This also leads to a higher Signal-to-Noise Ratio (SNR), when compared to single-ended amplifiers. Since the signal is twice larger, so is its power, leading to a SNR twice larger or 3 dB above the SNR of single-ended amplifier.

Fully-differential amplifiers are less susceptible to Common-Mode (CM) noise and power supply noise, as well. Consider the amplifier of Figure 2.21(b), where a small variation on the power supply occurs, that is $V'_{DD} = V_{DD} + \Delta V$. In that case, the source to gate voltage of M_3, $V_{SG3} = V'_{DD} - V_{BP}$ suffers the same variation ΔV, that is

$$V_{SG3} = V_{DD} + \Delta V - V_{BP}, \tag{2.34}$$

which results in drain current given by

$$I_{D3} = \frac{1}{2} K_P \frac{W}{L} \left(V_{DD} + \Delta V - V_{BN} - V_{THp}\right)^2. \tag{2.35}$$

If the circuit is balanced, this current is equally split between M_1 and M_2, which will produce a null output differential voltage, thus rejecting the variations of the power supply.

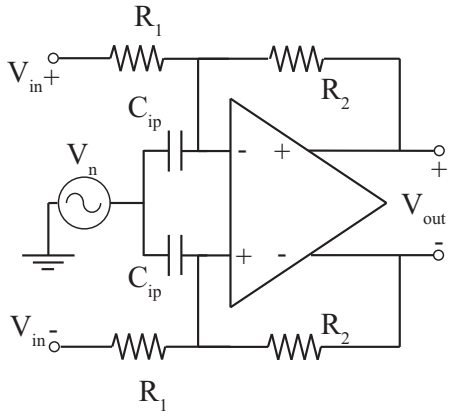


Figure 2.22: Fully-differential amplifier with CM noise.

Now, consider also the circuit of Figure 2.22, where V_n is a noise voltage that is coupled to each of the amplifier inputs by the parasitic capacitances C_{ip}. With this configuration, each input has an equal signal applied, therefore the CM input voltage suffers from disturbances. Since both input noise signals are equal, they cause an equal drain current variation in M_1 and M_2, leading to equal variations in V_{OP} and V_{ON}, respectively, which results in a zero differential output signal, if the amplifier is perfectly balanced. This means that the amplifier has zero CM gain and that this disturbance does not affect the CM output voltage [12]. In the case of the CM gain is nonzero but small, the CM voltage is affected, but the differential voltage is not, as long as the circuit is balanced. If that is not the case (for example, the parasitic capacitances are not matched), the

output differential voltage is affected. For this reason, it can be noticed that a fully-differential amplifier has a CM gain a_{cm} and a differential gain a_{dm}, which are independent, if the circuit is balanced, that is the Differential-Mode (DM) output is only proportional to the DM input and the CM output is only proportional to the CM input. Hence, a simple small-signal model for this amplifier can be derived, as shown in Figure 2.23(a).

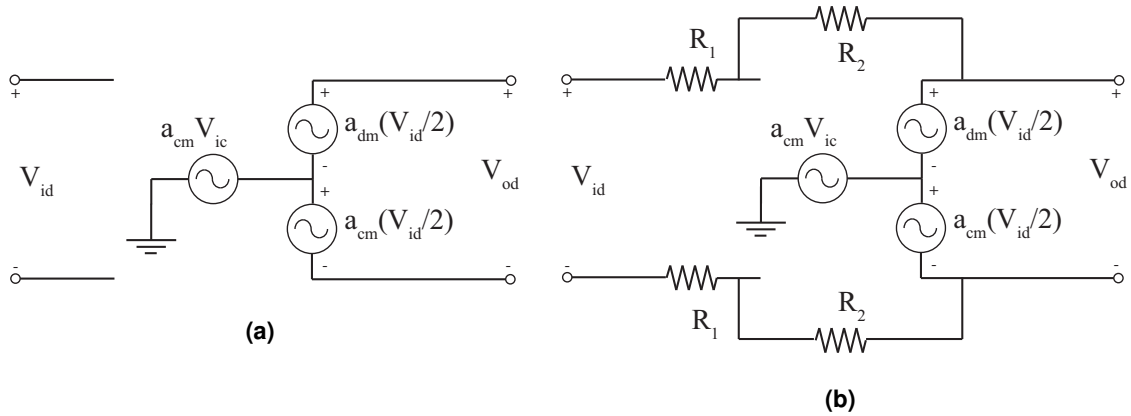


Figure 2.23: Small-signal model of a fully-differential amplifier: (a) open-loop configuration; (b) close-loop configuration.

Common-mode Feedback

As previously discussed, a fully-differential amplifier possesses a CM gain and a DM gain, which are independent, as seen in Figure 2.23. If the amplifier is ideal, $a_{cm} = 0$, $a_{dm} = -\infty$, which means that the CM output is zero for a finite input CM signal and the closed-loop DM gain is given by $-R_2/R_1$, as expected. This means that, while the DM output signal is well determined by the input DM signal, the CM input signal exerts little or no control in the CM output voltage V_{OCM}, since amplifiers have a very small CM gain, a_{cm} [12]. For all transistors to operate in saturation and maximize the output swing, a constant CM output voltage V_{OCM} must be applied. As the CM input voltage is not capable to control the output, an addition feedback path must be used in order to control the CM output voltage V_{OCM}, the Common-Mode Feedback (CMFB).

As seen from Figure 2.24(a), the CMFB is composed by a CM sensing block and a CMFB amplifier and employs a negative feedback to set V_{OCM} to a desired value, V_{CM}, by adjusting V_{BP} or V_{BN} of the amplifier of Figure 2.24(b). In this case, V_{BP} will be adjusted to make $I_{D3} = |I_{D4}| + |I_{D5}|$ when $V_{OCM} = V_{CM}$.

The CM sensing block calculates the CM output voltage V_{OCM} as $(V_{OP}+V_{ON})/2$. This voltage is then compared with the desired CM voltage and the difference is amplified. Then, a biasing voltage is added (the voltage needed to correctly bias M_3, that is V_{BP}) and the control signal V_{CMC}, which is given by

$$V_{CMC} = a_{cm}(V_{OCM} - VCM) + V_{bias}, \tag{2.36}$$

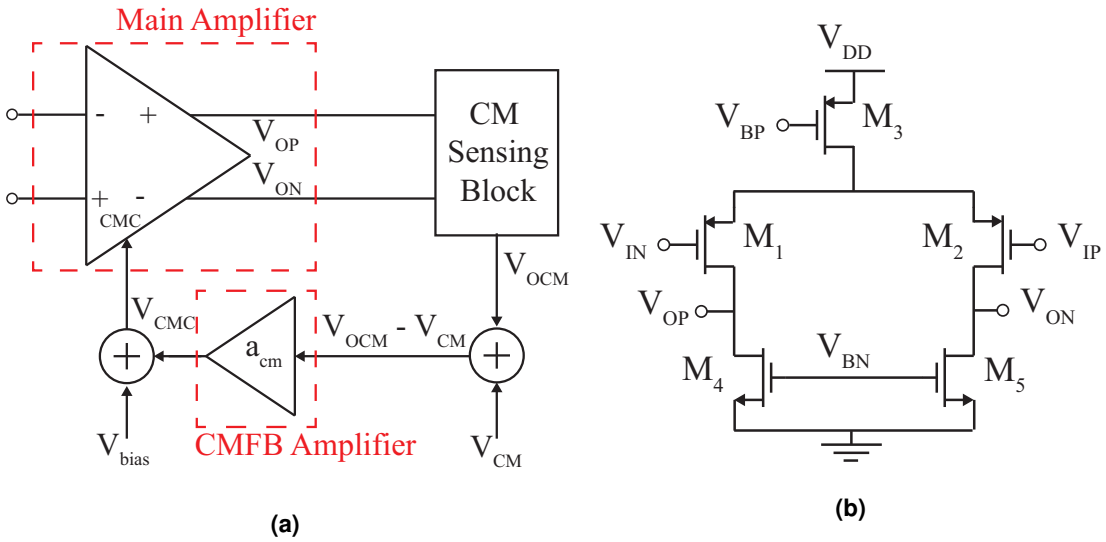


Figure 2.24: CMFB: (a) the top-level diagram; (b) the main amplifier circuit.

is fed into the amplifier, specifically the gate of M_3. If the CMFB gain is high enough, the negative feedback will force $V_{OCM} \approx V_{CM}$ and $V_{CMC} \approx V_{bias}$. Usually the gain from the CM control port, CMC, is much greater than unity, since it can be seen as the gain of a common-source, formed by M_3, with a large output resistance, and it is enough to provide all the gain needed in the CMFB loop, which allows a_{cm} to be small, thus having a larger bandwidth [12]. Two ways of implementing the CMFB are explained, whose main differences are in the way of sensing the output CM of the main amplifier.

CM Sensing with Resistive Voltage Divider

One of the most simple ways to implement a CMFB circuit is by using a single-ended CMFB amplifier and a resistive voltage divider as a CM detector, as shown in Figure 2.25(a). The output CM voltage V_{OCM}, which is given by $(V_{OP} - V_{ON})\frac{R_{CMS}}{R_{CMS}+R_{CMS}} = \frac{V_{OP}-V_{ON}}{2}$, is compared with the desired voltage V_{CM}, generating a control voltage that will bias M_3 (Figure 2.24(b)) and adjusting the output CM. The CMFB amplifier circuit is shown in Figure 2.25(b) and it is composed by a differential pair and two diode-connected PMOS transistors as load. The difference between V_{OCM} and V_{CM} will unbalance the differential pair in such a way that if $V_{CM} > V_{OCM}$, the drain current of M_9 will increase, as well as its source to gate voltage V_{SG9}. This voltage, when applied to the gate of M_3 (Figure 2.24(b)) will cause an increase of the tail current of the amplifier, increasing V_{OCM}. If $V_{CM} < V_{OCM}$, the drain current of M_9 decreases (Figure 2.25(b)) and, consequently, V_{SG9}, decreasing the amplifier tail current, which will bring V_{OCM} down.

By using CM sensing resistors, R_{CMS}, the DM output of the amplifier is loaded [12], as the node between resistors is an AC ground. This loading reduces the open-loop DM gain except if R_{CMS} is much larger than output DM resistance of the amplifier. The usage of resistors also

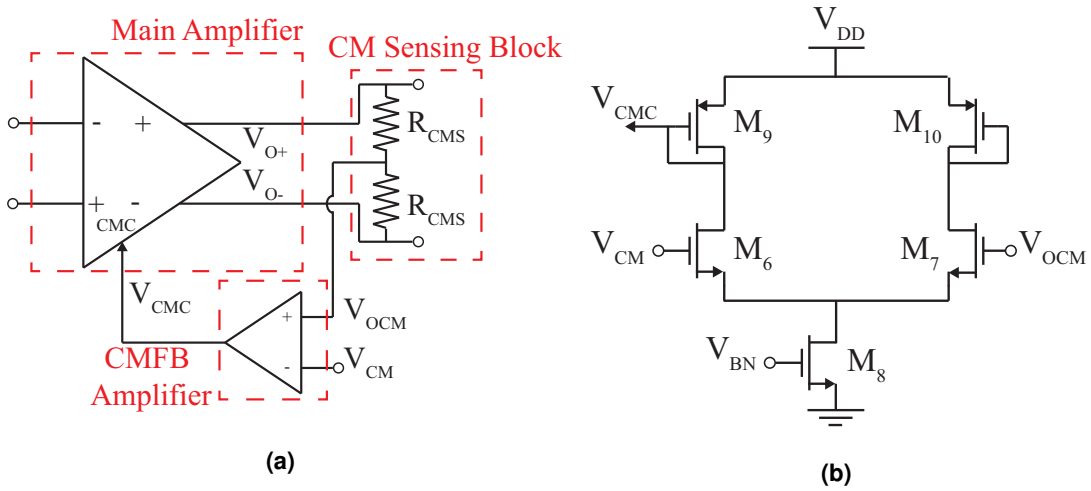


Figure 2.25: A CMFB scheme: (a) complete circuit; (b) the amplifier.

requires that they have large resistance values to ensure that the output current flows to the next stage and not to those resistors. To avoid the resistive loading, modifications to the circuit of Figure 2.25(a) can be made, for example adding buffers between the outputs and the resistors or controlling V_{OCM} by injecting currents into the amplifier, which will adjust the both CM outputs [12].

CM Sensing with Differential Pairs

A CMFB circuit that uses two differential pairs for CM sensing and amplification is shown in Figure 2.26.

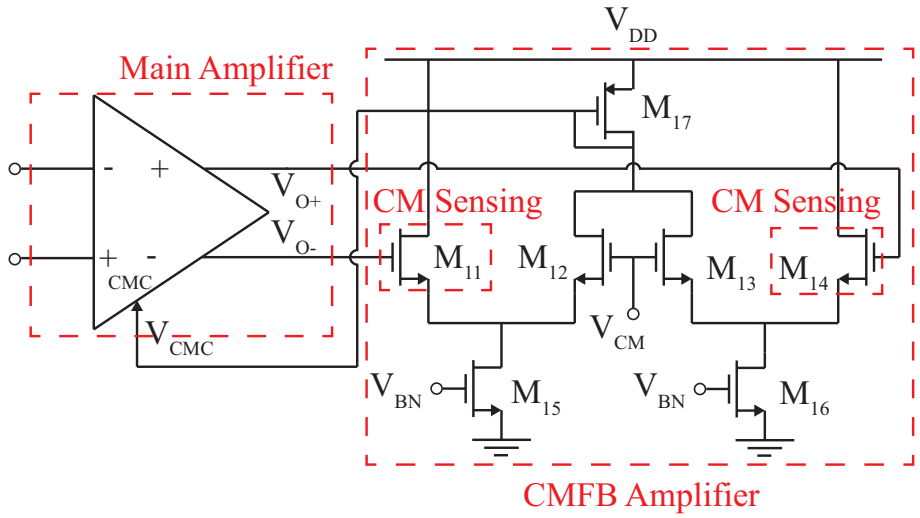


Figure 2.26: A top-level CMFB diagram.

In this circuit, transistors M_{11-14} are matched and they form two differential pairs, that sense the CM output V_{OCM} and generate a control voltage V_{CMC}, which is proportional to $V_{OCM} -$

V_{CMC}. Using a small-signal analysis and assuming that the CM gain of these pairs is zero, the drain currents of M_{12} and M_{13} are respectively given by

$$I_{D12} = \frac{I_{D15}}{2} + g_{m12}\frac{(V_{O-} - V_{CM})}{2} \tag{2.37}$$

and

$$I_{D13} = \frac{I_{D16}}{2} + g_{m13}\frac{(V_{O+} - V_{CM})}{2}. \tag{2.38}$$

These currents are summed in the diode-connected transistor M_{17}. Assuming that M_{15} and M_{16} are matched, the CM control current I_{CMC} is given by

$$\begin{aligned} I_{CMC} = I_{D17} &= I_{D15,16} + g_{m12,13}\left(\frac{V_{O+} - V_{O-}}{2} - V_{CM}\right) \\ &= I_{D15,16} + g_{m12,13}\left(V_{OCM} - V_{CM}\right). \end{aligned} \tag{2.39}$$

From (2.39), it can be noticed that I_{CMC} is composed by a DC component and a term proportional to $V_{O+} + V_{O-}$. This current is mirrored to M_3 (Figure 2.24(b)), which will produce the amplifier tail current. If $V_{OCM} = V_{CM}$, the tail current is simply equal to $I_{D15,16}$, which should be the nominal tail current set upon design.

This circuit does not resistively loads the amplifier but transistors $M_{11,14}$ have parasitic capacitances that increase the total output capacitance of the amplifier. Also, as this analysis was made assuming only small signals, this CMFB circuit will not properly function if the outputs are large enough to turn off any of M_{11-14} transistors. For this reason, their overdrive voltages must be increased.

To implement the fully-differential pre-amplifier, the CMFB that uses two differential pairs will be used to correctly set the amplifier output CM voltage.

2.6 DC Suppression

An important feature of circuits used for sensor reading is the capability to block the sensors biasing signals, which are usually DC signals, up to a few hundred of mV in amplitude. Furthermore, the sensors used present offsets which, adding to the biasing signals, can easily saturate the amplifiers. Therefore, there is the need of achieving a high-pass characteristic in order to eliminate the unwanted quantities [10] [13] [14].

In this work, MR sensors are used and they are biased by a DC current, so that variations in its resistance can be measured. This means that the signal coming from the sensors has a significant DC component. Several solutions to achieve DC suppression are possible, like the one implemented in [13], where a Capacitively Couple Chopper Instrumentation Amplifier (CCCIA) is implemented, which is composed by a folded cascode amplifier with a capacitive feedback path and chopper modulators (Figure 2.27). Its band-pass gain is given by C_{in}/C_{fb}, where C_{fb} and C_{in} are the feedback and input capacitance values, respectively.

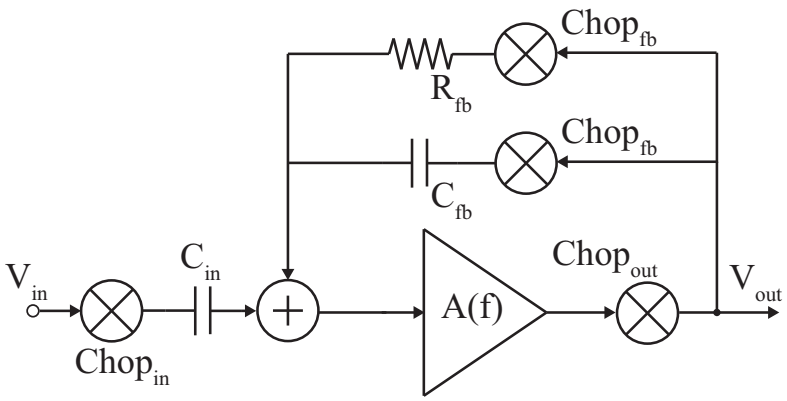


Figure 2.27: Block diagram of a CCCIA.

As Chopper Stabilization is implemented, due to the action of the input modulator $Chop_{in}$, the DC component is modulated to the chopper frequency f_{chop}, therefore is not blocked by the input capacitor C_{in} (Figure 2.27). To block the up-modulated DC, a new feedback path is added (Figure 2.28(a)), consisting of an inverting integrator (Figure 2.28(b)) that has a low-pass characteristic, amplifying only the DC at the output of the system. Then, the DC component is up-modulated to the chopper frequency f_{chop}, so that it can be subtracted from the signal at the virtual ground nodes of the amplifier. This implementation is called DC Servo Loop (DSL). Since the goal is to eliminate only the DC component, the high-pass pole of the system must be placed at a frequency f_{hp} lower than the input signal lowest frequency, in order to not affect it.

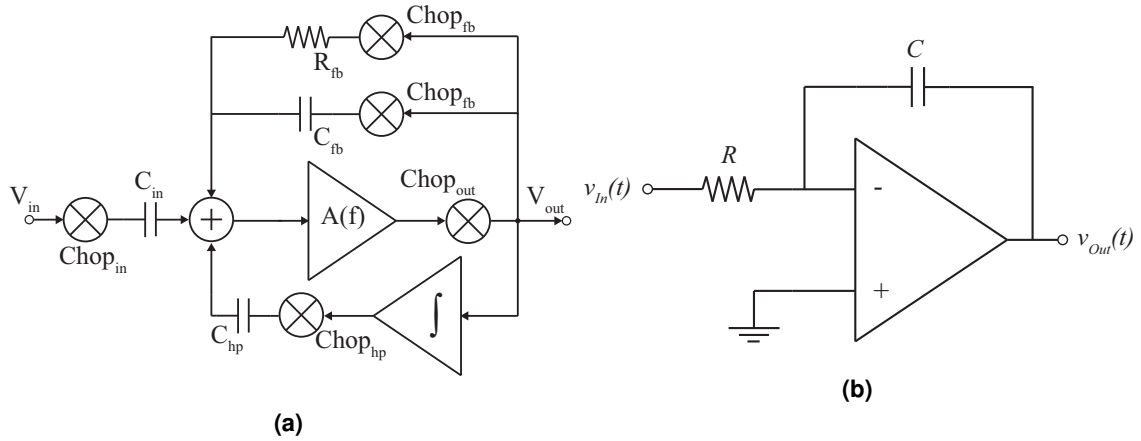


Figure 2.28: The DSL: (a) in the CCCIA; (b) integrator implementation.

For low-frequency applications, where input signal frequencies can be as low as 1 Hz, the pole of the integrator must be placed at a frequency f_{int} close to DC to force the frequency of the high-pass pole of the system f_{hp} to be lower than the minimal signal frequency. The frequency of the pole of the integrator, f_{int}, can be adjusted by changing its unity-gain frequency, $f_{0,int}$, which is given by

$$f_{0,int} = \frac{1}{2\pi}\frac{1}{CR} \tag{2.40}$$

where R and C are the values of the resistor and capacitor of the integrator of Figure 2.28(b). The unity-gain frequency of the integrator $f_{0,int}$ relates to the frequency of the high-pass pole f_{hp} of the circuit as follows:

$$f_{hp} = \frac{C_{hp}}{C_{fb}} f_{0,int}, \tag{2.41}$$

where the C_{hp} and C_{fb} are the values of the respective capacitors of Figure 2.28(a). To achieve such low pole frequencies, a solution would be to reduce the term C_{hp}/C_{fb}, however, as integrated capacitors have typical values from hundreds of fF up to few tens of pF and C_{fb} has a fixed value to establish the band-pass gain of the circuit, C_{hp}/C_{fb} can not be as low as desired to allow a larger integrator unity-gain frequency $f_{0,int}$, in order to have the same high-pass pole frequency f_{hp}. For this reason, either the resistor or capacitor of the integrator must be very large.

DSL with Switched Capacitor Integrators

To achieve low unity-gain frequencies, the integrator can be implemented as a Very Large Time Constant Switched Capacitor (VLTC-SC) integrator, as proposed in [13]. The VLTC-SC replaces the input resistors by equivalent SC ones, that have the advantages of being implemented with capacitors, which have a superior precision in production than resistors, have a controllable value by means of the switching frequency and occupy much less area.

For a typical fully differential SC integrator, the unity-gain frequency is given by

$$f_{0,SC} = \frac{f_{SW,SC} C_{A,SC}}{2\pi C_{B,SC}} \tag{2.42}$$

where $f_{SW,SC}$ is the switching frequency, $C_{A,SC}$ is the input sampling capacitor and $C_{B,SC}$ is the feedback capacitor. The Very Large Time Constant Switched Capacitor (VLTC-SC) integrator presented in [13] (Figure 2.29) has some differences when compared to the typical SC integrator. In the VLTC-SC integrator, the unity-gain frequency is given by

$$f_{0,VLTC-SC} = \frac{f_{SW,VLTC-SC} C_{A,VLTC-SC}^2}{2\pi C_{B,VLTC-SC}^2} \tag{2.43}$$

where $f_{SW,VLTC-SC}$ is the switching frequency, $C_{A,VLTC-SC}$ is the input sampling capacitor and $C_{B,VLTC-SC}$ is the feedback capacitor. As seen $C_{A,VLTC-SC}$ and $C_{B,VLTC-SC}$ appear squared, which greatly relaxes the capacitor area, while still being able to achieve very low pole frequencies. As an example, to achieve a 0.1 Hz unity-gain frequency, with a switching frequency of 2.5 kHz, the VLTC-SC uses $C_{A,VLTC-SC} = C_{C,VLTC-SC} = 240pF$ and $C_{B,VLTC-SC} = 15pF$, while, to achieve the same frequency with the same sampling capacitor, the typical integrator needs a capacitor $C_{B,SC} = 937.5pF$ [13].

Integrator with Pseudo-resistors

Another way to achieve such low unity-gain frequencies is to replace the resistors of the integrator by pseudo-resistors [14] [15]. A pseudo-resistor is composed by one or more diode-connected MOS transistors in series in near cut-off or sub-threshold region, as shown in Figure

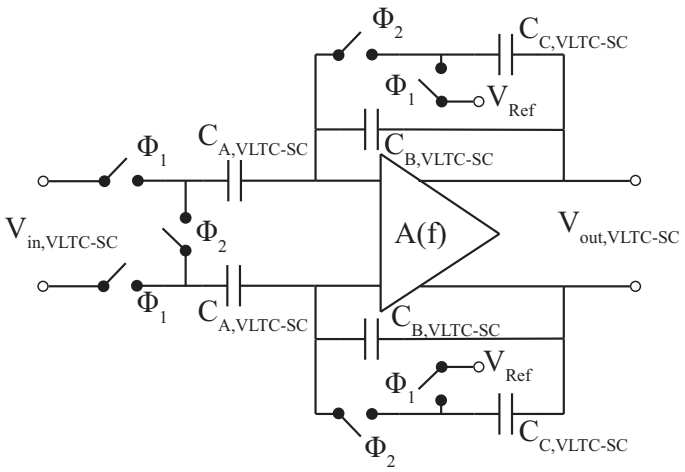


Figure 2.29: A VLTC-SC integrator.

2.30. This simple architecture adds small noise and parasitics to the circuit, being able to achieve resistance values in the order of GΩ [16]. Pseudo-resistors, like the one in Figure 2.30, also present a variation in resistance for large voltage swings and are sensitive to process mismatch.

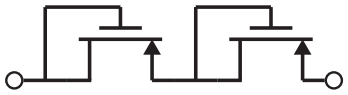


Figure 2.30: A pseudo-resistor.

Using pseudo-resistors, resistance values in the order of GΩ can be achieved. This satisfies the need of having a high-pass pole in very-low frequencies. However, the pseudo-resistor of Figure 2.30 has a fixed resistance value, determined by the dimensions of the transistors used and the voltages applied, not being able to be changed after fabrication. In [5] and [16], a tunable pseudo-resistor is proposed, in which the gate voltage V_G of the transistors is changed using a voltage source, in order to change the ”ON” and ”OFF” state of the transistor, therefore controlling its resistance.

Given the discussed techniques, the pre-amplifier of the ASIC was chosen to be implemented as a CCCIA with a DSL. To implement the DSL, pseudo-resistors will be used to create the low-frequency high-pass pole.

2.7 Summary

In the previous sections, the theoretical context of this work is presented. An Eddy-Current (EC) Non-Destructive Testing (NDT) system, used to detect flaws in metallic materials via induced electric currents, is explained. It makes use of MR sensors and an ASIC to pick up and process signals that indicate the presence of flaws. The ASIC is composed by a pre-amplifier that introduces significant amounts of flicker noise.

Flicker noise can be mitigated by using two techniques: Autozero and Chopper Stabilization.

The first one is a sampling-based technique that stores the noise quantity in a first phase and subtracts it from the input signal, in a second phase. The other technique, Chopper Stabilization, uses modulation to avoid the overlapping of spectral components of signal and noise. Chopper Stabilization will be implemented on the pre-amplifier since it is fully analog, does not introduce aliasing and the modulators are simpler circuits than the S&H block needed in Autozero.

To implement chopper, modulators are added to the input and output of the amplifier. These modulators are composed by four switches that introduce charge injection and present reduced input signal swing, that can increase noise levels and add distortion, respectively. These problems can be mitigated by using TGs with half-sized dummy switch compensation.

Since the modulators are differential circuits, the implementation of a fully-differential pre-amplifier is considered, however this type of amplifier requires a CMFB circuit to establish their output CM voltage.

The pre-amplifier will be implemented as a Capacitively Couple Chopper Instrumentation Amplifier (CCCIA) that is composed by a chopper fully-differential amplifier in a capacitive feedback loop. The NDT system of this work presents large input DC components that need to be suppressed. For this reason, a DSL can be used when DC blocking capacitors cannot solve this issue, for example when using the CCCIA. Basically, the DSL isolates the amplified DC component from the amplifier output, up-modulates it and feeds it back into the amplifier input, creating a very low-frequency high-pass pole. However, to achieve this very low-frequency pole, the unitary-gain frequency of the integrator needs to be very small, leading to very large input resistors. To achieve GΩ resistance values, pseudo-resistors will be used.

3

System Overview and Pre-amplifier Implementation

Contents

3.1 Introduction

Chapters 1 and 2 provide the goals and a short description of this work, as well as a theoretical review of concepts and state-of-the-art work developed by other authors. As seen, this thesis focus an Eddy-Current (EC) Non-Destructive Testing (NDT) system, based on Magneto-Resistive (MR) sensors to detect flaws in metallic materials. The usage of low frequency magnetic signals leads to the presence of flicker noise, that corrupts readings. Also, the sensors DC biasing signal may saturate the amplifier if not blocked. In order to understand how the techniques explained in Chapter 2 may or may not be applied to this system and which options must be taken, a full description of this system is performed in this chapter. It starts by defining the how biasing of the sensors, their multiplexing and reading is performed. Afterwards, Chopper Stabilization will be implemented on the original single-ended pre-amplifier and in a test amplifier to evaluate their performance and evaluate significant aspects regarding Chopper Stabilization. Afterwards, both amplifiers will be converted into fully-differential amplifiers to be used in a Capacitively Couple Chopper Instrumentation Amplifier (CCCIA). The amplifier that achieves the best performance will then be used in the final implementation, where a DC Servo Loop (DSL) is included.

3.2 The ASIC

As described previously, the system in focus, shown in Figure 3.1, is formed by a sensor array and an Application Specific Integrated Circuit (ASIC), which is composed by a current source, a pre-amplifier and a cancellation block. The current source produces the sensors biasing current, originating a voltage signal that is multiplexed and fed to the pre-amplifier. The cancellation block is used to mitigate the sensors DC biasing signal component, by creating a DC component equal to the one of the sensors, which is also applied to the amplifier. This way, the biasing signal is seen as Common-Mode (CM), therefore being rejected. The current source, sensor reading and cancellation blocks are described in the following subsections.

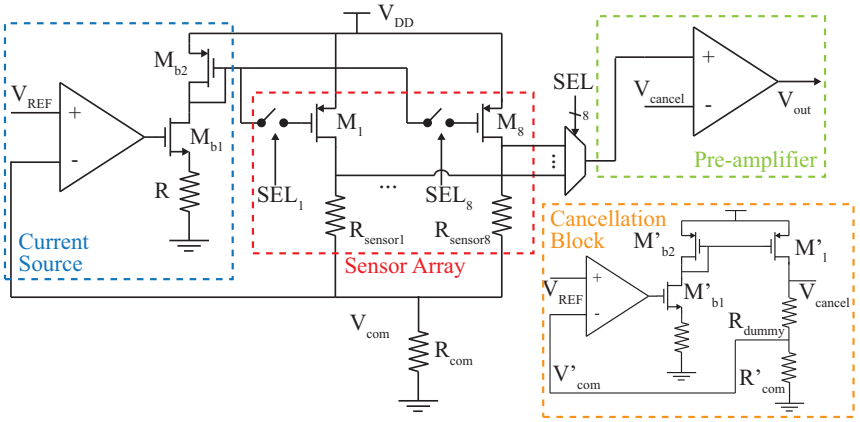


Figure 3.1: Full circuit schematic.

3.2.1 Current Source and Sensor Addressing

The system in [4] has four ASICs, each one responsible for the biasing, multiplexing and signal amplification of 8 sensors, making a total of 32 MR sensors. The MR sensors are here treated as simple resistors and, in order to produce a measurable electrical signal that represents the variation of resistance with the magnetic field, these sensors must be biased by a well determined current.

The biasing current is supplied by the current source shown in Figure 3.2, which is composed by an amplifier, a common-source (CS) stage and a diode-connected transistor that mirrors the current to the sensors. This current source is presented in [17].

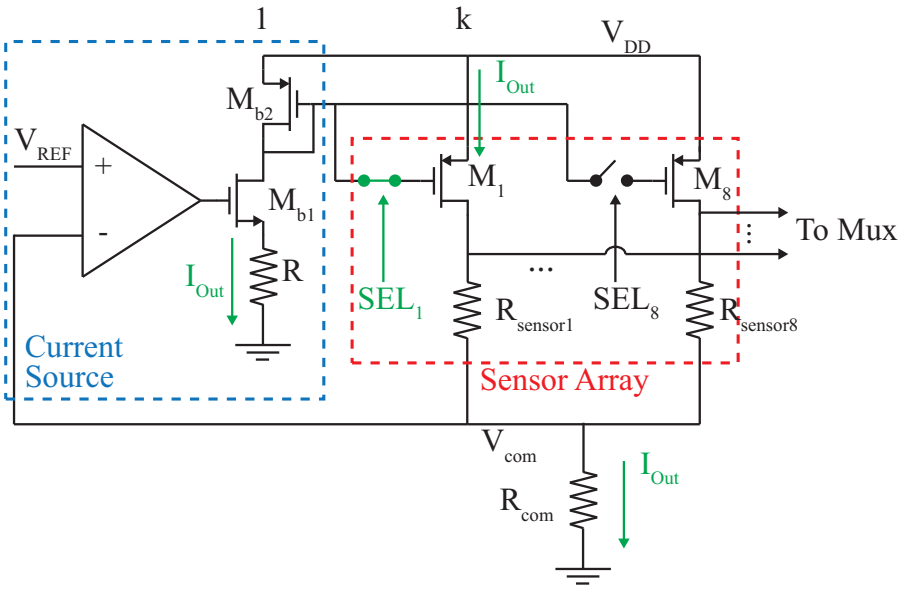


Figure 3.2: Full circuit schematic.

A reference voltage V_{REF} is applied to the input of the amplifier, producing an output voltage that ensures an output current I_{Out} across the CS stage. The CS stage is here present to make sure that the output voltage is independent from the sensor resistance. The current I_{Out} is then mirrored by a diode-connected transistor (M_{b2}) to the selected sensor [17]. The selection of sensor 1, for example, is made by closing a switch connecting the gates of M_{b2} and M_1, mirroring the current to this sensor and to a common external variable resistor R_{com} [4]. As the amplifier forces V_{com} to be equal to V_{REF}, R_{com} is used to adjust the current. V_{com} is fed back into the amplifier, achieving a negative feedback configuration with a loop transfer function given by

$$I_{Out} = \frac{G.\frac{g_{mb1}}{1+g_{mb1}R}.k}{1+G.\frac{g_{mb1}}{1+g_{mb1}R}.k+R_{com}}.V_{REF} \approx \frac{V_{REF}}{R_{com}}, \tag{3.1}$$

where G is the gain of the amplifier, k is the current mirror gain and g_{mb1} is the transconductance of transistor M_{b1}. Since the output current I_{Out} is given by the feedback loop, several parallel sensor biasing branches can be connected, while using the same amplifier and R_{com} [17].

A very important aspect regarding the current source is its noise. As it produces the biasing current, its noise contribution will be present at each sensor, which can corrupt readings. For this reason the current source noise must be kept at its minimum. In [17] the noise of the current source is analyzed. The total noise power may be found by summing the individual current noise contributions of the circuit components and is given by

$$\overline{I_{Out}^2} = \frac{\overline{V_{amp}^2}}{R_{com}^2} + \frac{\overline{V_{Mb1}^2}}{G^2.R_{com}^2} + \frac{\overline{I_{Mb2,R}^2}}{G^2\left(\frac{g_{mb1}}{1+g_{mb1}}\right)R_{com}^2} + \frac{\overline{I_{M1}^2}}{G^2\left(\frac{g_{mb1}}{1+g_{mb1}}\right)R_{com}^2 k^2} + \overline{I_{Rcom}^2}, \tag{3.2}$$

where $\overline{V_{amp,Mb1}^2}$ is the noise voltage contribution of the current source amplifier and M_{b1}, respectively, and

$\overline{I_{Mb2,M1,R,Rcom}^2}$ is the noise current contribution of M_{b2}, M_1, R and R_{com}, respectively. If G is large, equation 3.2 simplifies into

$$\overline{I_{Out}^2} \approx \frac{\overline{V_{amp}^2}}{R_{com}^2} + \overline{I_{com}^2}. \tag{3.3}$$

By measuring the voltage drop in the sensor, the total noise voltage power is given by

$$\overline{V_{Out}^2} = \overline{I_{Out}^2}R_{sensor}^2 + \overline{V_{sensor}^2} = (\overline{V_{amp}^2} + 4k_BTR_{com})\left(\frac{R_{sensor}}{R_{com}}\right)^2 + \overline{V_{sensor}^2}, \tag{3.4}$$

where $\overline{V_{sensor}^2}$ is the sensor noise voltage contribution, k_B is Boltzmann's constant and T is the temperature in Kelvin. As can be seen, the total noise is directly related to the values of resistance of both the common resistor R_{com} and the sensors. As the sensors have a fixed resistance value, R_{com} can be set in order to provide the desired biasing current and reduce the noise contribution, leaving the amplifier of the current source as the main noise source.

3.2.2 Cancellation Block

The cancellation block is a circuit used to mitigate the sensors DC biasing signal, that can saturate the amplifier due to its large value (up to 1 V). It is composed by a current source equal to the one responsible for the sensor biasing, represented in Figure 3.2, a dummy sensor R_{dummy} and common-resistor R'_{com}.

The idea behind this block is shown in Figure 3.3, where all components from the Current Source & Sensor 1 block are ideally matched with the respective components from the cancellation block. Both current sources provide an equal current that bias the sensor $R_{sensor1}$ and the dummy sensor R_{dummy}, which leads to equal biasing DC signals. By exposing the sensor $R_{sensor1}$ to the magnetic fields produced by the ECs and keep the dummy sensor way from them, the sensor $R_{sensor1}$ presents an additional AC component that the dummy sensor R_{dummy} does not. This way, if one feeds both output signals of each block ($y_1(t)$ and V_{cancel}, in Figure 3.3) into the pre-amplifier, the DC components present themselves as a CM signal (as they are equal) to the pre-amplifier, which are greatly attenuated, given the nature of the amplifier.

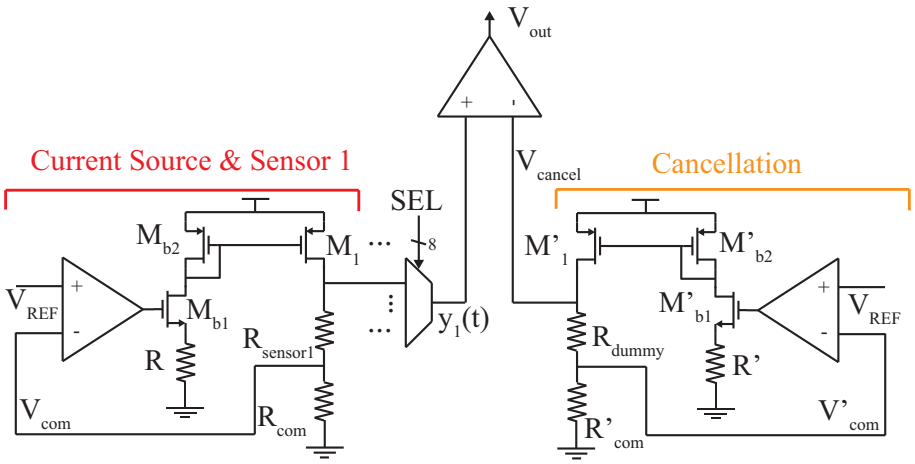


Figure 3.3: Cancellation block working principle.

Once again, this technique only results in perfect cancellation if the components are matched. If that is not the case, the DC components present small changes that are seen as a differential signal by the amplifier, thus being amplified. This results in a residual DC offset that should be taken into account and dealt with, as process mismatch may be such that the resulting DC components have significantly different values, leading to large differential components that are amplified and are capable of saturating the amplifier.

3.3 Pre-amplifier and Typical Chopper Implementations

The existing pre-amplifier of the NDT will be the target of improvements to mitigate its thermal and flicker noise. The amplifier is optimized to achieve a lower noise floor and Chopper Stabilization is implemented and tested to reduce flicker noise. Chopper Stabilization was chosen over Autozero as the latter is a sampling based technique that introduces aliasing, that increases the noise floor, as discussed in Chapter 2, thus being more suitable for discrete signal systems [11]. The optimization process of the existing amplifier is not here object of analysis, as it was carried out by the project team and falls out of the scope of this work. For this reason only performance results of the optimized amplifier are shown. During the process here discussed, another amplifier (from now on called test amplifier) was used to make a preliminary assessment of the performance of Chopper Stabilization and important aspects, and to infer what is the best way to implement it on the final amplifier. For this reason, a brief description of both amplifiers is made, followed by the implementation of a typical Chopper Stabilization configuration on the test amplifier. To finalize, the final amplifier is converted into a fully-differential one to be included in a Capacitively Couple Chopper Instrumentation Amplifier (CCCIA) configuration, which will compose the final pre-amplifier circuit. This conversion process is described with focus on the additional circuitry, needed to make the final amplifier work, and the important aspects regarding this configuration.

3.3.1 Characterization of the Amplifiers

In this subsection, both amplifiers are briefly reviewed since, they will be target of significant changes needed to implement Chopper Stabilization and, given their different performances, they are expected to present different results when subjected to this flicker noise reduction technique, which may reveal important details regarding this process.

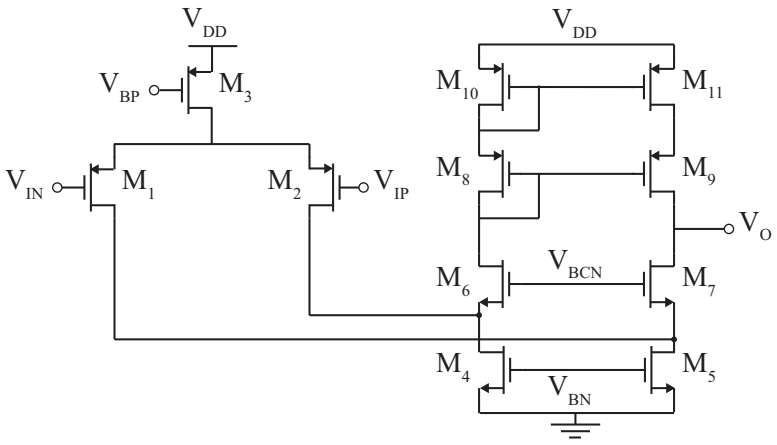


Figure 3.4: Pre-amplifier circuit.

The internal structure of the amplifiers is presented in Figure 3.4. They were chosen to be folded cascode OTAs, since from the three OTA topologies, it is the one that offers the best balance between gain, bandwidth, IRN and voltage headroom, as discussed in Chapter 2. As the major concern in this work is to improve the flicker noise performance, PMOS differential pairs were chosen, as PMOS transistors have a lower flicker noise corner frequency f_k.

The test amplifier was designed for an introductory course on Microelectronics, with the goal of introducing the full design process of an amplifier. This amplifier achieves the specifications presented in Table 3.1.

Table 3.1: Test amplifier's specifications.

Specification	Value
Open-loop Gain	63 dB
Bandwidth	10 kHz
Load Capacitor	4 pF
Phase Margin	50 º
Total Current	400 µA

The final amplifier is an optimized version of the original amplifier of the NDT system, that was developed by the project team. A summarized overview of the final amplifier main characteristics is shown in Table 3.2. and, in Table 3.3, its transistor dimensions and drain currents are also shown. The transistors are divided in instances with the specified dimensions to allow the creation of fingers in the layout, therefore, the total transistor drain current I_D is found by multiplying

Table 3.2: Final amplifier's specifications.

Specification	Value
Open-loop Gain	85 dB
Bandwidth	20 kHz
Load Capacitor	2 pF
Phase Margin	58 º
Total Current	4.5 mA

the number of instances by the drain current per instance. For example, each transistor of the differential pair as a total drain current of $29.55 \times 10^{-6} \times 50 \approx 1.5$ mA.

Table 3.3: Transistor parameters of the final amplifier.

Transistor	Width [µm]	Length [µm]	Number of Instances	I_D per instance [µA]
$M_{1,2}$	40	0.35	50	29.55
M_3	48.55	2.15	20	147.7
$M_{4,5}$	54.5	5.1	20	110.8
$M_{6,7}$	55	2.8	10	73.94
$M_{8,9}$	50	0.35	20	36.97
$M_{10,11}$	50	3.35	20	36.97

Both amplifiers are configured in a capacitive feedback scheme, as shown in Figure 3.5. The capacitor ratio C_{in}/C_{fb} defines the close-loop gain to 20 dB, by using 10 pF and 1 pF for the respective capacitors. The resistor R_{fb} is used to allow the feedback of the DC component, assuring the correct biasing of the input stage. It also sets a high-pass pole with frequency $f = 1/(2\pi C_{fb} R_{fb})$.

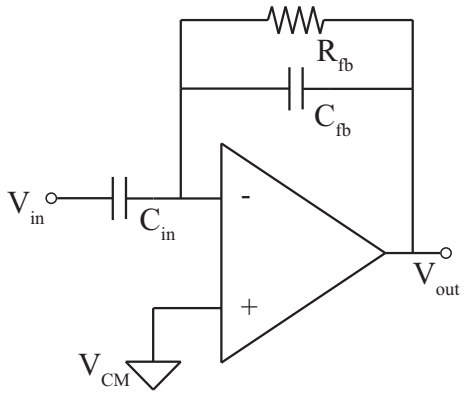
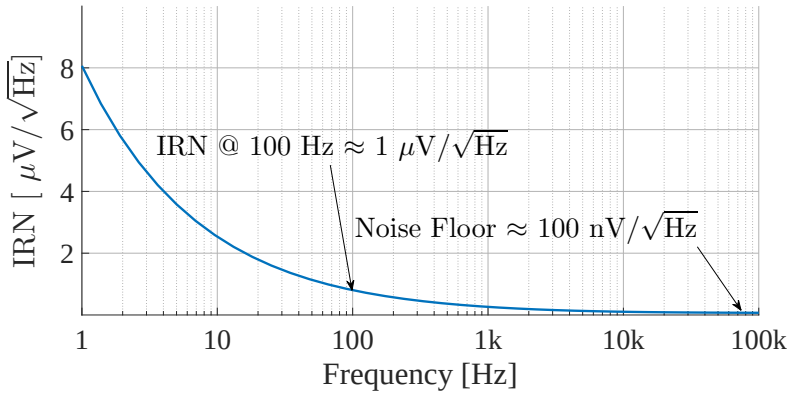


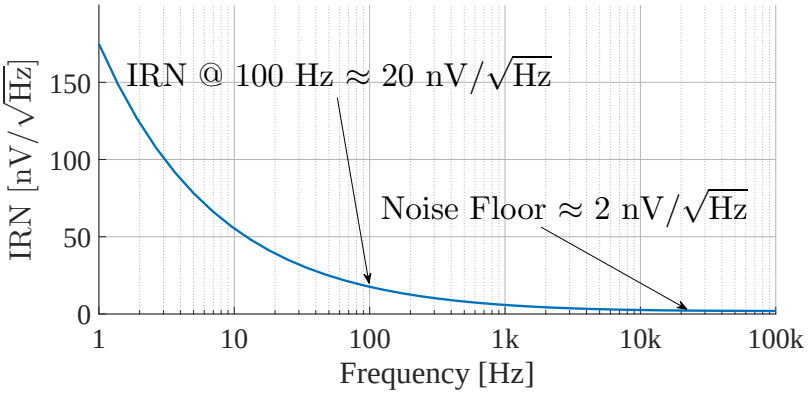
Figure 3.5: Pre-amplifier feedback configuration.

With this configuration, the IRN of both amplifiers is simulated and presented in Figure 3.6. The test amplifier presents very high noise levels of about 1 µV/$\sqrt{\text{Hz}}$ at 100 Hz and a noise floor of 100 nV/$\sqrt{\text{Hz}}$, which are unacceptable for this application. Nevertheless it presents itself as a control circuit that will be useful for performance comparison. As for the final amplifier noise, it shows a significantly low noise floor of 2 nV/$\sqrt{\text{Hz}}$, however, bellow 100 Hz, flicker noise contribution raises the noise above the established specification for this circuit, 20 nV/$\sqrt{\text{Hz}}$, which must be dealt with.

Notice that the final amplifier has a very low noise floor since it was designed to have a very large output current of about 1.5 mA and the test amplifier an output current of 100 µA. Also, both amplifiers present a flicker noise corner frequency of about 10 kHz.



(a)



(b)

Figure 3.6: Pre-amplifier IRN: (a) test amplifier; (b) final amplifier.

3.3.2 Typical Chopper Stabilization Implementation

In the previous chapter, dummy compensated TGs were chosen to implement the modulators needed to apply Chopper Stabilization to the amplifiers described. The typical way to do this, is to simply add the modulators to the input and output of the amplifier, inside the feedback loop, as shown in Figure 3.7(a).

The input modulator is directly connected to the inputs of the amplifier. As the pre-amplifier is single-ended and the modulator is differential, one of the inputs of the modulator is connected to the CM voltage V_{CM} and the other is connected to the signal (Figure 3.7(a)). This is essential since the amplifier needs a certain V_{CM} to correctly bias its transistors in order to function. This way, V_{CM}, set to half the supply voltage, is periodically applied to the inverting and non-inverting

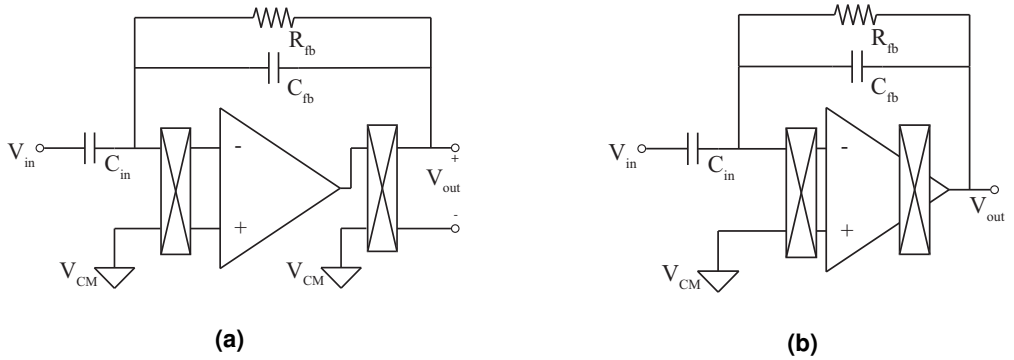


Figure 3.7: Implementations of Chopper Stabilization: (a) typical implementation; (b) implementation with modulators in the cascode stages of the amplifier.

inputs, respectively, due to the action of the chopper modulator. The other input (the one which is connected to the signal) is supplied with V_{CM} by means of the feedback resistor R_{fb}, which takes the output CM voltage and feeds it to the input.

Directly connecting the input modulator to the inputs of the amplifier is a common practice, however, in some cases, it may lead to some problems related to charge injection. It is stated in [18] that the injected charges, due to chopper action, causes transient current spikes with an average value I of

$$I = 2f_{chop}(WLC_{OX}V_{OD} + C_{OL}V_{CLK}) \tag{3.5}$$

where, f_{chop} is the chopping frequency, C_{OX}, C_{OL} and V_{CLK} are, respectively, the gate oxide capacitance per unit of area, the overlapping capacitance and the amplitude of the clock signal. This current, if not compensated, can have a value up to tens of pA, which is greater than the gate leakage current of the differential pair [18]. Thus the current associated with chopper action, when injected into high impedance nodes, such as the inputs of the amplifier, leads to high noise voltage levels. From the simulations performed in [18], it is found that of all noise sources, the contribution associated with charge injection is dominant and proportional to the chopper frequency and transistor area, as shown by (3.5). If chopper is disabled, this noise contribution disappears and the total IRN is significantly lower. To overcome this problem, the current associated to chopper action should be compensated by the presence of dummy switches.

To test this approach, both input and output modulators are added to the test amplifier, in the feedback configuration of Figure 3.7(b). Then simulations are run for different transistor dimensions of the input modulator, to vary their parasitic capacitances and evaluate the effects of the charge injected by the input modulator.

The effect of the injected charge of the input modulator is evaluated by setting the main transistors of the output modulator to an aspect ratio of 2µm/0.4µm. These dimensions were used in order to ensure a low ”ON” resistance of the transistors that compose the output modulator. If the ”ON” resistance it too high, significant voltage drops appear across the modulators, which reduce

the output headroom of the amplifier and can, in fact, force the transistors of the output stage to leave saturation.

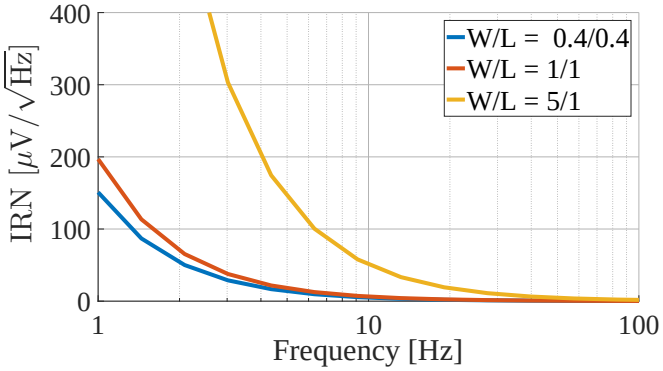


Figure 3.8: Simulated IRN for the different input modulator transistor area.

As can be seen from Figure 3.8, the placement of the input modulator at the inputs of the amplifier leads to IRN levels of hundreds of $\mu V/\sqrt{HZ}$. For increasing transistor area, the parasitic capacitances are also increased, which leads to larger current to be injected in the high impedance inputs of the amplifier, thus increasing the IRN even further.

The output modulator is also a differential circuit, but the amplifier output is single-ended, which makes it difficult to set up a proper feedback path without a single-ended to fully-differential conversion. This is because the feedback must supply both the output signal and CM output voltage simultaneously, which happens only during half the chopper period. On the other half, the modulator outputs switch, feeding back only the CM voltage.

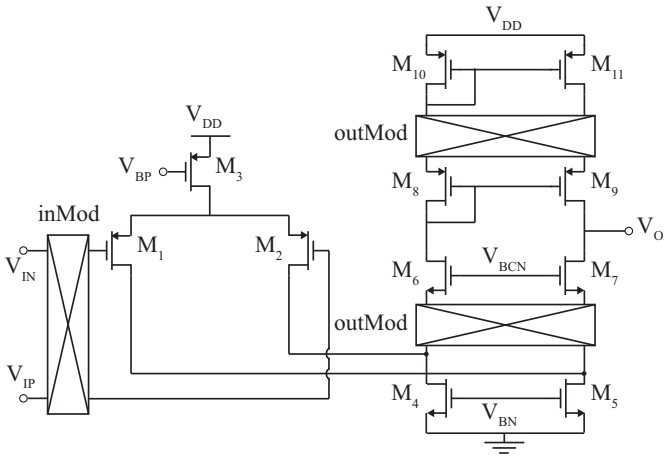


Figure 3.9: Schematic of a chopped folded cascode with modulators in the low impedance cascode nodes.

The most common solution to the problem just described is to embed the output demodulation in the second stage of the folded cascode amplifier [10] [19], as shown in Figures 3.7(b) and 3.9. Two modulators are added to the sources of $M_{6,7}$ and $M_{8,9}$, respectively. This way, the currents flowing through the cascode stages are swapped periodically, leading to a demodulated signal, as

expected. The placement of the modulators in the cascode stages has two advantages. The first one is that the signals currents are demodulated within the output stage, which are mirrored to the output, achieving the differential to single-ended conversion and the demodulation at the same time. The second advantage is that the modulator placed at the sources of $M_{8,9}$ up-modulates the errors of M_{6-9} [10] and reduces the effects of the injected charge on the IRN, as they are injected in lower impedance nodes.

However, the size of the transistors of the output modulator must be chosen carefully, for them to have small "ON" resistance. As already mentioned, high "ON" resistance leads to significant voltage drops across the modulators, which may lead the transistors of the output stage to leave saturation.

The typical chopper topology proposed could not lead to a desired outcome due to the elevated IRN, originated by the action of the input modulator at high impedance nodes, when using capacitive feedback. According to [18], the dominant cause of chopper noise is the injected charge which is proportional to the chopper frequency and transistor area. Thus, these two quantities must be reduced.

As the typical chopper topology could not be put to work, other ways to implement Chopper Stabilization were studied and the ones described in [19], [13] and [20] seem promising as they do not have the input modulator in the inputs of the amplifier, that causes high noise voltage. Instead, in these works, the modulation and demodulation occurs outside the feedback paths. This solution will be tested on both the test and the final amplifier, on the next section.

3.4 Capacitively Coupled Chopper Instrumentation Amplifier

As seen in Chapter 2, a state-of-the-art Capacitively Couple Chopper Instrumentation Amplifier (CCCIA) topology is proposed in [13] and [20], that include the amplifier and its feedback paths within the chopper path.

Figure 3.10 shows a top level diagram of the proposed topology, which have several differences when compared to the ones already presented. The first one is that it is a differential topology and, as seen in Section 2.5, differential circuits have higher output voltage swing and less susceptibility to CM and power supply noise. Moreover, they are more suitable to fit with chopper modulators, since they are also differential circuits. Other difference is that the input modulation is done prior to the input capacitor and not in the amplifier inputs. The placement of the input modulator before the input capacitor will allow the DC biasing signal of the sensors to reach the amplifier, as this signal is up-modulated by the input modulator and thus it is not blocked by the capacitor. In this section, the CCCIA topology is reviewed with emphasis on its feedback paths, the single-ended to fully-differential conversion of the amplifier and DC blocking techniques, as it will be implemented as the pre-amplifier of the ASIC.

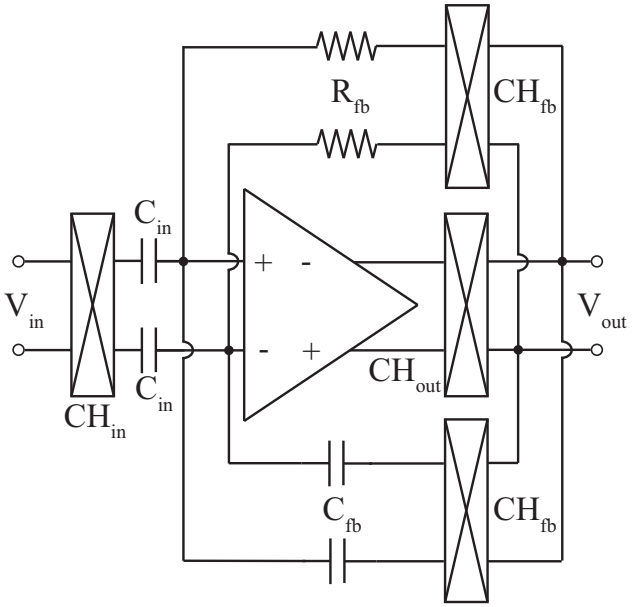


Figure 3.10: Top-level diagram of the proposed CCCIA.

3.4.1 Feedback Configuration

Feedback is a technique used to stabilize the gain of an amplifier, improve linearity and reduce sensitivity to process variations and is crucial to any amplifier circuit. This case is no exception, thus, the CCCIA makes use of the amplifier inside a capacitive feedback loop as shown in Figure 3.10. The use of a capacitive feedback network has some advantages when compared to a resistive feedback network such as the fact that integrated capacitors have superior process accuracy than resistor, which result in reduced gain variations due to mismatch.

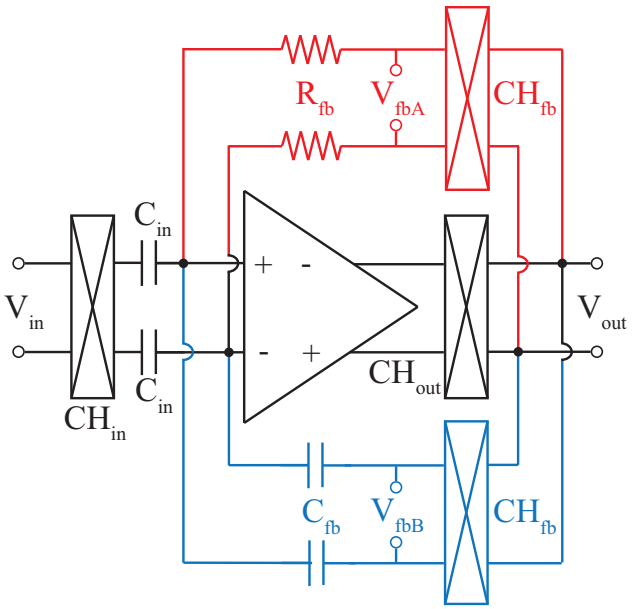


Figure 3.11: Feedback paths of the CCCIA.

As the amplifiers used in the proposed CCCIA are fully-differential ones, the feedback paths must also be differential. In this configuration two paths for each feedback are used: one resistive path and another capacitive, highlighted in red and blue, respectively, in Figure 3.11. The resistive feedback is here employed to ensure that the CM output voltage is fed into the amplifier inputs to accomplish their correct bias. To do this, a very large feedback resistor must be used to be able to not allow any current through it that can cause a voltage drop. If any significant current is present, the voltage drop across the resistor is significantly large and the CM voltage at the inputs of the amplifier is no longer equal to the one at its outputs.

The gain of the CCCIA is established by the ratio between the input and feedback capacitors, for an infinite gain amplifier. Since both amplifiers used have finite gain A_0, the overall gain of the CCCIA G is given by

$$G = \frac{A_0}{1 + A_0 C_{fb}/C_{in}}. \tag{3.6}$$

However, if the gain of the amplifier A_0 is made sufficiently large, (3.6) simplifies in

$$G \approx \frac{C_{in}}{C_{fb}}. \tag{3.7}$$

In this work, to set the close-loop gain to 20 dB, $G = 10$, C_{in} was chosen to be 10 pF as C_{fb} was chosen to be 1 pF. They were set this way, since due to the action of the chopper modulators, both capacitors can be seen as a Switched Capacitor (SC) resistor [13] with a resistance given by

$$R_{eq} = \frac{1}{2 f_{chop} C_{in,fb}}, \tag{3.8}$$

thus, having a thermal noise contribution of $4k_B T R_{eq}$, which can be minimized by increasing both capacitors. However, the input equivalent resistor defines the amplifier input impedance, which can not be too small, thus the capacitors can not be too large.

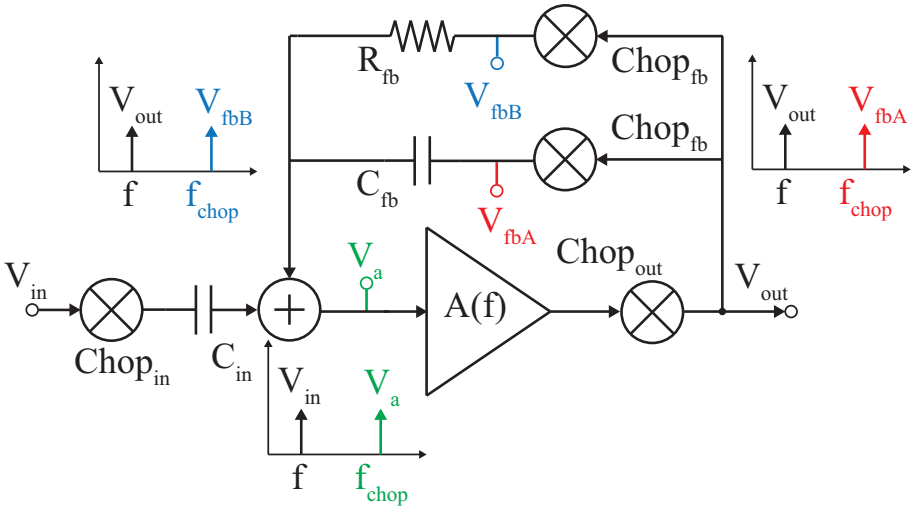


Figure 3.12: CCCIA block diagram: signal components along the feedback paths.

The CCCIA makes use of two additional chopper modulators in both feedback paths to up-modulate the output signal and feed it back into the amplifier inputs. Considering Figure 3.12,

these two additional modulations allow the matching of the signal components frequency in the amplifier input node V_a (note that in each node, a representation of the signal component is present, however the components in black are not present at those nodes, being there just to make a frequency comparison). As the input signal, with frequency f, is modulated by the input chopper CH_{in}, its signal components are shifted from their baseband to the chopper frequency f_{chop}, resulting in an amplifier input signal V_a in that same frequency (highlighted in green). After amplification, the signal is demodulated by CH_{out}, resulting in V_{out} with the same f frequency as the input. To be able to apply feedback, one can not simply connect the output and input nodes as the signal components of interest are at different frequency bands. If such connection is done, the node V_a would have a component in f_{chop} and in f, thus the signal feedback is not achieved. Therefore, to be able to correctly apply feedback, V_{out} must be modulated to f_{chop}, using the modulators CH_{fb}. Then the up-modulated signal can be fed into the feedback resistor R_{fb} and into the feedback capacitor C_{fb} to accomplish the DC feedback (in blue) and the signal feedback (in red), respectively, as all three components are at the same frequency band in the input node V_a. The inclusion of four chopper modulators is a disadvantage since more modulators lead to increased spike amplitude, thus a larger unwanted spectral component, that must be eliminated, is present.

Another very important aspect is that due to action of the input chopper, DC signals are no longer blocked, since they are modulated to the chopper frequency. This way, the high-pass pole, which is present in the typical chopper implementation, no longer exists. This problem can be solved by apply a DC Servo Loop (DSL) to the CCCIA, as discussed in Section 3.5. However, to be able to implement the CCCIA of Figure 3.10 and, consequently, the DSL, the single-ended amplifiers covered in Subsection 3.3.1, must be converted into fully-differential amplifiers. This conversion will be covered in the following subsection.

3.4.2 Single-ended to Fully-differential Conversion of the Amplifiers

As referred above, this CCCIA uses a fully-differential amplifier with a differential capacitive feedback. To implement it, the previously studied amplifiers must be altered to accommodate fully-differential operations, by adding biasing and CMFB circuits (the test amplifier modifications are similar to the ones discussed for the final amplifier, thus they will not be covered in detail).

Final Amplifier

To convert the final single-ended amplifier into a fully-differential one, the self-biased current mirrors are eliminated by disconnecting the gates and drains of M_{10} and M_8, respectively, as shown in red in Figure 3.13, and take the nodes at the drains of $M_{8,9}$ as the inverting and non-inverting outputs (in blue), respectively. This way, the branches of the output stage of the folded cascode amplifier are independent form each other and a differential output voltage can be taken

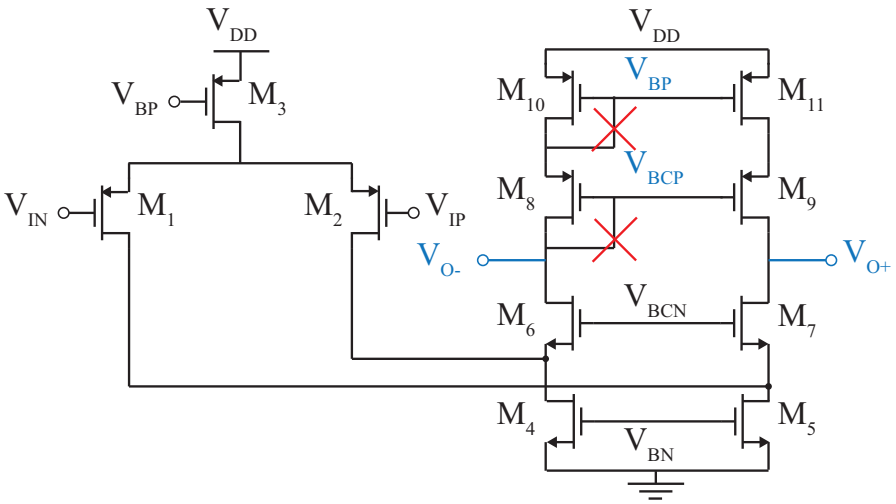


Figure 3.13: Single-ended to fully-differential conversion.

as $V_O = V_{O+} - V_{O-}$. However, this transformation leads to two aspects that must be addressed. Firstly, since transistors M_{8-11} no are no longer biased by the pre-existing current mirror, they will require additional circuitry to generate the appropriate biasing voltages for these transistors. Secondly, as studied in Section 2.5, full-differential amplifiers require a Common-Mode Feedback (CMFB) to force the outputs to be at a desired CM voltage, as the input is no longer capable to control the output CM.

In order to design the needed circuits to include in the final amplifier, its transistor drain currents and sizes, presented in Table 3.3, must be considered.

Biasing Circuit

The original amplifier has a biasing branch used to generate V_{BDP}, V_{BCN} and V_{BN}, which is shown in Figure 3.14(a). It is composed by a PMOS and two NMOS current mirrors and two parallel 10 kΩ resistors that are used to generate the reference current of the mirrors.

Since to convert the original amplifier, the current mirrors in the output stage are removed, two new voltages (V_{BCP} and V_{BP}) must be generated to correctly bias those transistors. In order not to change the original biasing circuit, as it was optimized for low noise, a similar circuit is added to generate V_{BCP} and V_{BP}, which is composed by another resistor and two PMOS current mirrors (Figure 3.14(b)).

The simplest solution to find the transistor parameters for the new biasing circuit is to use the same parameters of the transistors corresponding to each mirror. This way, the correct drain current and overdrive voltages are achieved, without changing any parameters that were optimized to get very low noise. To set the reference resistor correctly, a parametric DC analysis was performed to vary the resistance value and evaluate the drain current of the transistor, in order to choose the resistance that leads to the desired current value. The resistor was set to a value of

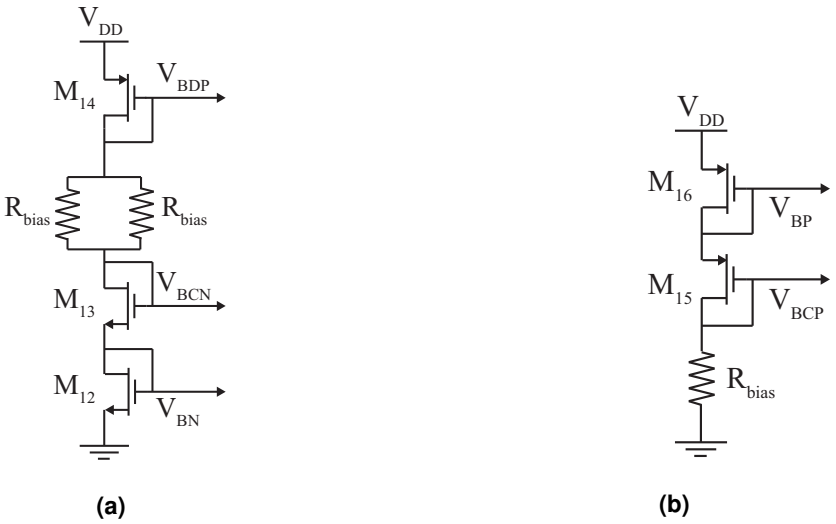


Figure 3.14: Biasing circuits: (a) original; (b) added.

36 kΩ. Transistor parameters of the biasing circuit are presented in Table 3.4.

Table 3.4: Transistor parameters of the biasing circuit.

Transistor	Width [µm]	Length [µm]	Number of Instances	I_D per instance [µA]
M_{12}	53.85	7.25	1	79
M_{13}	50	0.35	2	39.5
M_{14}	55.55	5.05	1	79
M_{15}	50	0.35	1	39.5
M_{16}	50	3.35	1	39.5

Common-mode Feedback

The CMFB is an essential part of the amplifier, as it sets the output CM voltage to a desired value that bias the output stage correctly and maximizes the output swing, by means of negative feedback. This feedback can be implemented using the circuits studied in Chapter 2, where a CM detector block is used to sense the CM output voltage V_{OCM}, that is then compared with the desired value, V_{CM}, by means of an amplifier. The difference is used to generate a control voltage that will, in this case, control the differential pair's tail current, therefore correcting V_{OCM}. To implement this concept, the two differential pair circuit of Figure 3.15 will be used, as this one does not resistively load the amplifier and does not use very large resistors to implement the CM detector, as the other circuits presented in Chapter 2.5.

To briefly review the operation of the circuit, it calculates the difference between V_{OCM} and V_{CM}, which unbalance the differential pairs, causing a variation on the drain currents of M_{18} and M_{19}. These currents are summed in the diode-connected transistor, M_{23}, and originate a control voltage, V_{CMC}, that controls the amplifier tail current. Therefore, when $V_{OCM} = V_{CM}$, the nominal biasing voltage must be applied in order to provide the tail current set upon design. Since

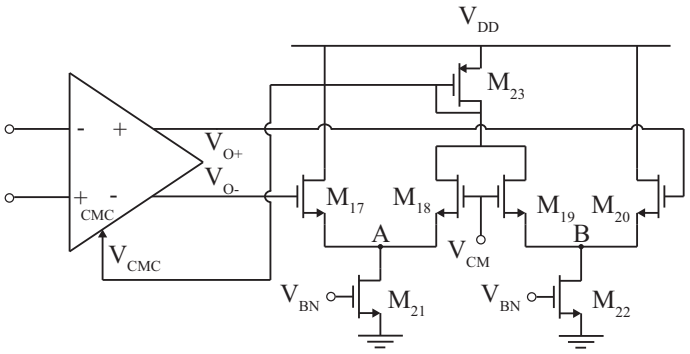


Figure 3.15: CMFB circuit implemented.

the amplifier was optimized for minimal noise, the CMFB circuit must be applied without changing transistor parameters of the folded cascode circuit. Thus, M_{23} should provide the same voltage as the one in the original biasing circuit, that is $V_{CMC} = V_{BDP}$ (Figure 3.14(a)), in order to provide the correct tail current. For this reason M_{23} was made equal to M_{14} (Figure 3.14(a)), which is the original current mirror that bias M_3 (Figure 3.13), and V_{BDP} was disconnected from the gate of M_3 to allow the control of the tail current by V_{CMC}.

As for the two differential pairs formed by M_{17-20}, all transistors must be matched, so that when $V_{OCM} = V_{CM}$, they all have the same drain current. This means that their drain current must be half the drain current of M_{23}, that is $I_{D17-20} = I_{D23}/2 = 39.5$ µA. To allow large voltage swings at the inputs of the differential pairs without leaving saturation region, these transistors where designed to allow large overdrive voltages (about 400 mV). This way, the aspect ratio of these transistors can be written as

$$\left(\frac{W}{L}\right)_{(17-20)} = \frac{2I_{D17-20}}{K_N V_{OD}^2} = 1.45. \tag{3.9}$$

To set the CMFB differential pairs tail current, another two simple current mirrors, formed by $M_{15,16}$, are used. Their drain current must be twice the drain current of M_{17-20}, that is 79 µA, which is the same as the drain current of M_{12} of the original biasing circuit. For this reason, $M_{21,22}$ are made equal to M_{12} and a copy of the original biasing circuit is used to provide the correct biasing for the CMFB. The same biasing circuit could have been used to bias the NMOS transistors of the output stage of the amplifier and the CMFB circuit. However, the CMFB circuit can be subjected to large variations due to the action of the differential pairs, which can drastically change the voltage of nodes A and B. This action will make the drain-to-source voltages V_{DS} of the current mirrors vary, therefore varying the biasing voltage of the NMOS transistors (V_{BN}), which is undesirable. Table 3.5 presents the transistors dimensions of the final amplifier.

Test Amplifier: Single-ended to Fully-differential Conversion

The test amplifier (Figure 3.16(a)) is also converted to a fully-differential amplifier. As in the final amplifier, the self-biased current mirrors in the output stage were removed and a different

Table 3.5: Transistor parameters of the final fully-differential amplifier.

Transistor	Width [µm]	Length [µm]	Number of Instances	I_D per instance [µA]
$M_{1,2}$	40	0.35	50	29.55
M_3	48.55	2.15	20	147.7
$M_{4,5}$	54.5	5.1	20	110.8
$M_{6,7}$	55	2.8	10	73.94
$M_{8,9}$	50	0.35	20	36.97
$M_{10,11}$	50	3.35	20	36.97
M_{12}	53.85	7.25	1	79
M_{13}	50	0.35	2	39.5
M_{14}	55.55	5.05	1	79
M_{15}	50	0.35	1	39.5
M_{16}	50	3.35	1	39.5
M_{17-20}	4	3	2	19.75
M_{21-22}	53.85	7.25	1	79
M_{23}	55.55	5.05	1	79

CMFB circuit (which is here described) was added to set its CM output voltage to a desired level. The test amplifier is also included in the CCCIA and its performance is evaluated and compared to the performance of the CCCIA with the final amplifier.

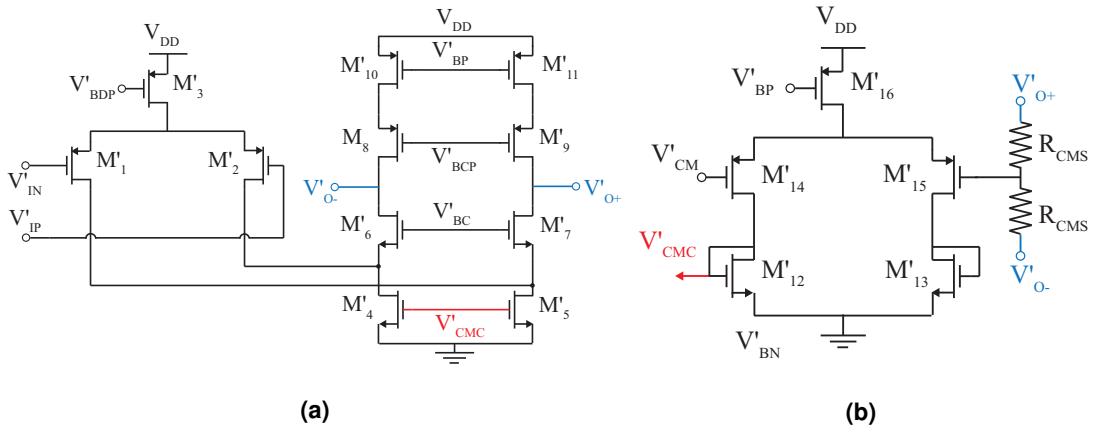


Figure 3.16: Test amplifier: (a) folded cascode circuit; (a) CMFB circuit.

The test amplifier makes use of the simplest CMFB circuit to accomplish to control of the output CM voltage. As seen in Chapter 2, this circuit senses the output CM voltage V_{OCM} by using a resistive voltage divider using two very large resistors R_{CMS}. These resistors are made large to create a high impedance at the output, avoiding the output current to follow to the voltage divider. V_{OCM} is compared to V_{CM} using the differential pair formed by $M'_{14,15}$, which originates a corresponding current that is mirrored to $M'_{4,5}$, achieving the control of the current on the output stage of the test amplifier.

The biasing circuits of this amplifier are not discussed since the are somewhat similar to the ones used in the final amplifier, composed by simple current mirrors. This way, the transistor parameters of the test amplifier can be summarized in Table 3.6.

Table 3.6: Transistor parameters of the biasing circuit.

Transistor	Width [µm]	Length [µm]	I_D [µA]
$M'_{1,2}$	43.1	1	64
M'_3	51.8	0.6	128
$M'_{4,5}$	18.6	0.65	75
$M'_{6,7}$	10	0.7	11
$M'_{8,9}$	103.4	2.4	11
$M'_{10,11}$	99.1	2.3	11
$M'_{12,13}$	63	1.1	152
$M'_{14,15}$	94.5	1.1	152
M'_{16}	189	1.1	304

3.4.3 Fully-differential Amplifiers Comparison

The test amplifier is compared to the final amplifier, when using each of them in the CCCIA. In Figure 3.17, the gain of both amplifiers is shown. They achieve 20 dB in their pass-band, which is defined by the capacitive feedback and test amplifier presents a significantly lower bandwidth than the final amplifier.

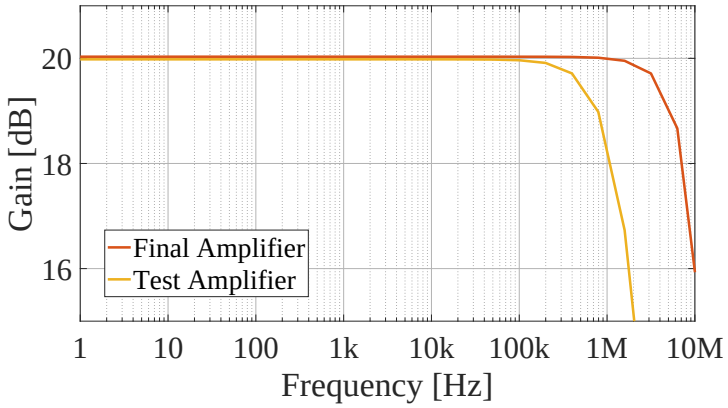


Figure 3.17: Gain of the CCCIA with the test and final amplifiers.

As for their IRN, the amplifiers present almost constant characteristics, however the test amplifier presents an IRN value of about 54 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, while the final amplifier only has 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, which is expected has the final amplifier was optimized for low noise, as discussed.

For these reasons, the final amplifier is the one chosen for the CCCIA and from now on, it is the only amplifier considered. However, with the test amplifier, the CCCIA can also be put to work and can be used for applications where the noise requirements are not so tight and less output current is required.

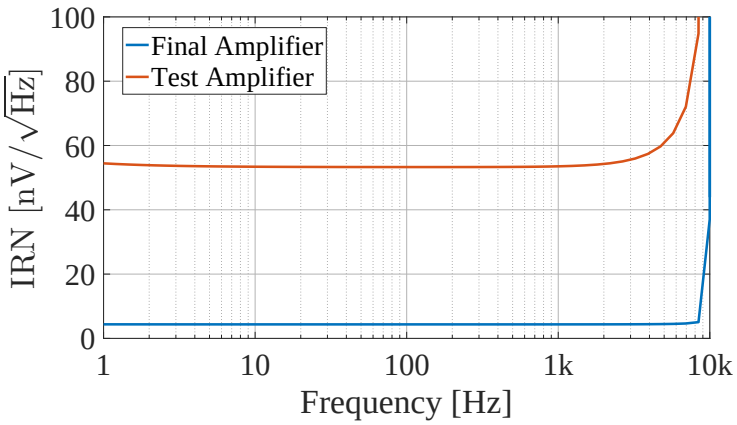


Figure 3.18: IRN of the CCCIA with the test and final amplifiers.

3.5 DC Servo Loop

In Chapter 2, the DSL was introduced as a DC suppression technique, that creates a high-pass characteristic, enabling the cancellation of large sensor DC biasing signals. The basic principle behind this technique (presented in Section 2.6) is to take the DC component of the output voltage of the CCCIA and apply it to the amplifier input node by means of a negative feedback. In this section, the DSL feedback path and its components are described, with special attention to the integrator specifications, feedback capacitors and high-pass pole frequency.

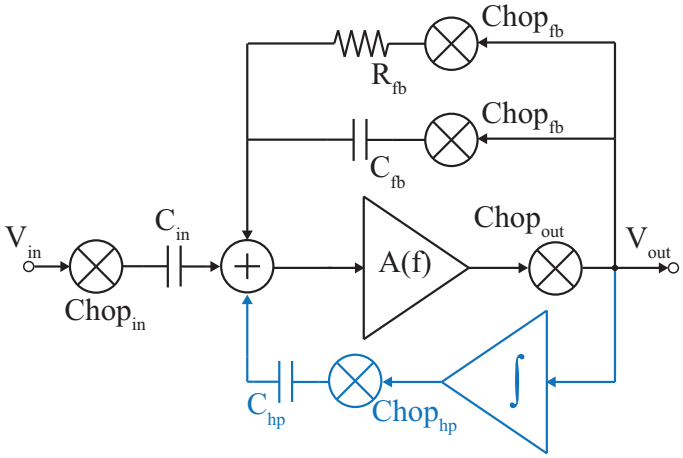


Figure 3.19: Inclusion of the DSL.

To start the analysis, consider Figure 3.19, where the DSL was added as a new feedback back. It is composed by an integrator, a chopper modulator and a feedback capacitor, here called high-pass capacitor C_{hp}, since these components establish a high-pass pole in the system.

To take the DC component from the output signal, an inverting (or Miller) integrator is implemented to create low-pass filter with a very narrow bandwidth, to allow only the DC component to be amplified and reject other frequencies. The integrator is shown in Figure 3.20(a) and makes

use of an input resistor R_{int} and a feedback capacitor C_{int}, having a frequency response shown in Figure 3.20(b).

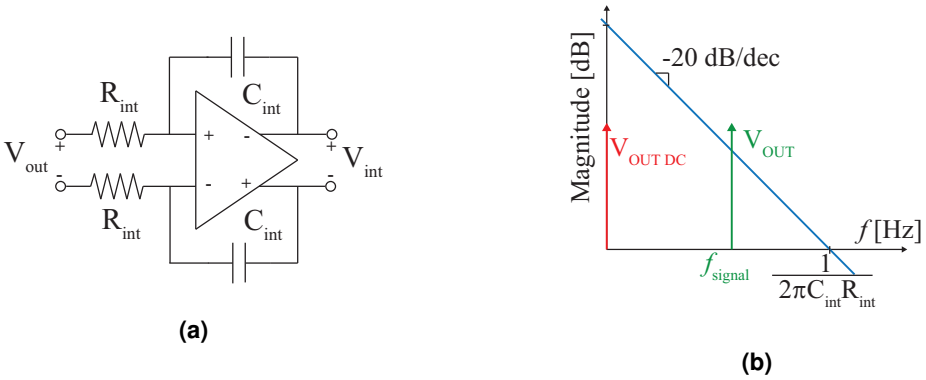


Figure 3.20: Integrator: (a) schematic; (b) frequency response.

The unity-gain frequency f_0 of the Miller integrator is given by

$$f_0 = \frac{1}{2\pi C_{int} R_{int}}, \tag{3.10}$$

and needs to be sufficiently small to allow enough attenuation of the signal component, while amplifying only the DC component. This filtered DC component is then up-modulated to the chopper frequency f_{chop}, in order to match the up-modulated sensor DC biasing signal present at the amplifier inputs, as shown in Figure 3.21. The up-modulated DC component of the DSL, V_{hp} is fed to the amplifier input node through C_{hp}, achieving a negative feedback configuration that cancels out the sensor DC biasing signal and places a low-frequency high-pass pole in the circuit transfer function.

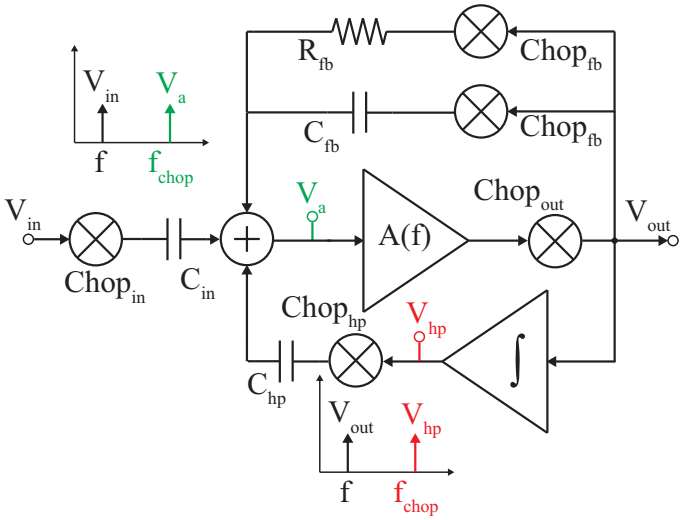


Figure 3.21: Component frequency matching to achieve DC cancellation.

There are two ways to control the frequency of the high-pass pole (f_{hp}) and set it to very low values, as it is a function of both the unity-gain frequency of the integrator $f_{0,int}$ and the ratio

between C_{hp} and C_{fb}, described by (3.11):

$$f_{hp} = \frac{C_{hp}}{C_{fb}} f_{0,int}. \tag{3.11}$$

The first way is to decrease the unity-gain frequency of the integrator $f_{0,int}$ as much as possible, which can be accomplished by choosing large C_{int} and R_{int}, as described by (3.10). If the capacitor ratio of (3.11) is set to 1, then the high-pass pole frequency is equal to the unity-gain frequency of the integrator. Since the pole must be placed in a region typically below 1 Hz, $C_{int} \times R_{int}$ must be set to at least $1/2\pi$ s, which requires a GΩ resistor for a typical 10 pF capacitor.

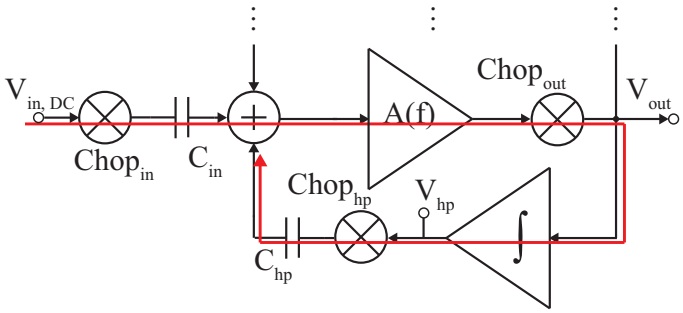


Figure 3.22: Feedback path formed by the DSL.

The second way is to change the ratio between C_{hp} and C_{fb}, specifically by making C_{hp} smaller than C_{fb}. However, the additional feedback path formed by the DSL, shown in Figure 3.22, establishes a relation between the DC sensor biasing signal $V_{in,DC}$ and the output of the integrator V_{hp}, given by

$$\frac{V_{hp}}{V_{in,DC}} = \frac{C_{in}}{C_{hp}}. \tag{3.12}$$

This means that by reducing C_{hp}, the maximum sensor DC biasing signal $V_{in,DC}$ that can be attenuated is also reduced, for the same V_{hp}. Noting that V_{hp} is limited by the maximum and minimum output voltages of the amplifier that composes the integrator, the maximum input DC voltage that can be attenuated is given by $(C_{hp}/C_{in})V_{hp}$, thus for a maximum V_{hp} of 1 V, to attenuate 1 V, C_{in} and C_{hp} must be equal.

To ease the requirement of having to attenuate the input DC voltage $V_{in,DC}$ by 1 V, the previously referred cancellation block is used (Section 3.2.1). As the cancellation block uses a dummy sensor R_{dummy} with a dummy common resistor R'_{com}, it is able to block all the sensor DC biasing signal $V_{in,DC}$, if the components of the cancellation block are matched with their counterparts. However, due to process mismatch such cancellation is not achieved, leaving a residual offset, which can be up to few hundreds of mV. This residual offset generated by mismatch presents itself as a much more viable target for the DSL to cancel, since it is much lower than the referred sensor DC biasing signal $V_{in,DC}$ of 1 V. Taking into account (3.11) and (3.12), a smaller $V_{in,DC}$ allows the usage of smaller C_{hp}, for the same V_{hp}, which helps to achieve a lower high-pass pole frequency.

With this solution, this circuits aims to cancel residual offsets of 200 mV, as the cancellation block deals with most of the input DC voltage. With this new relaxed specification, the high-pass capacitor C_{hp}, the integrator unity-gain frequency $f_{0,int}$ and the integrator capacitor C_{int} can be dimensioned, as shown in Table 3.7.

Table 3.7: DSL dimensioning parameters.

Parameter	Equation	Value	Comments
C_{int}	3.10	10 pF	To make $f_0 \approx 1$ Hz.
R_{int}	3.10	15.9 GΩ	To make $f_0 \approx 1$ Hz.
C_{hp}	3.12	2 pF	For $V_{in,DC} = 200$ mV, $C_{in} = 10$ pF and $V_{hp} = 1$ V.
f_{hp}	3.11	2 Hz	For $C_{fb} = 1$ pF

Notice that from Table 3.7, f_{hp} is made higher than f_0. This seems to contradict the above discussion, where was stated that C_{hp} should be smaller than C_{fb} to ease the need of having a very low integrator unity-gain frequency $f_{0,int}$, which needs very large capacitors and/or resistors. However, C_{hp} was made larger than C_{fb}, to ensure that an higher sensor DC biasing signal could be attenuated by the DSL. To deal with the requirement of a 15.9 GΩ to achieve $f_{0,int} = 1$ Hz, a pseudo-resistor was used, which is composed by two diode connected PMOS transistors, that will mostly work in subthreshold region, providing a very large resistance [21]. This way, the only current passing through them is a leakage current in order of hundreds of fA up to few pA. Thus, these transistors can be seen as very large resistors, without occupying huge chip areas. In cut-off region, these transistors may present very different resistance values from the one proposed in the DSL dimensioning. However, as long as the resistance value is greater than the one referred, the high-pass pole is guaranteed to be at any frequency below 1 Hz, which is the main goal.

3.6 Summary

In this chapter, the full system is described with special focus on dimensioning the pre-amplifier and the techniques applied to mitigate its flicker noise and sensor DC biasing signals. It is shown that the sensors are biased by a low-noise current source similar to the one described in [17], that supplies a DC current to each sensor and a common resistor. The resulting voltage is then fed to the amplifier that rejects DC and amplifies the remaining frequency components. In this study, two previously designed amplifiers are used to evaluate the feasibility of Chopper Stabilization in this kind of system, by taking each one and apply chopper modulators with different dimensions, in a capacitive feedback configuration. Results show that with this configuration, a large noise current associated to the modulators is injected into the high impedance node of the amplifiers, leading to impracticable IRN levels [18].

To overcome this problem, a differential CCCIA topology, that performs the modulations needed in Chopper Stabilization outside the capacitive feedback loop, is implemented. Since the final amplifier is the one that shown the smallest IRN, it is converted to a fully-differential amplifier by using

additional biasing circuitry and a CMFB mechanism. Since the modulation is performed before the capacitive feedback loop, the noise current component associated with chopper modulators is not injected in the amplifier input, which avoids the increased IRN, as in the previous case. However, the up-modulated DC components are allowed to pass through the input capacitors, which will saturate the amplifier. To solve this issue, a DSL is added, which consists of an integrator that senses the output DC component, up-modulates it and then subtracts it from the amplifier input, in a negative feedback configuration, that places a very low-frequency high-pass pole in the system transfer function. Since to be able to cancel 1 V of input DC, very large capacitors and/or resistors are needed, the previously developed cancellation block is used to mitigate most of the sensor DC biasing signal, while the DSL is used to mitigate eventual offsets originated by process mismatch between sensors of the sensor array and the cancellation block. To further relax the requirement of large capacitors and resistor, pseudo resistors are used to achieve GΩ resistance values, without using huge chip areas.

4

Results

Contents

4.1 Introduction

This chapter will cover the most important simulated results obtained for several components of the final circuit. These results will be used to evaluate the performance of the solutions proposed, the meeting of specifications and to explore the causes of the problems presented.

To begin, both the original single-ended amplifier of the ASIC and final fully-differential amplifier are characterized by simulating their gains, stability parameters and noise performance. This testing will be performed using a capacitive feedback configuration without Chopper Stabilization. The CCCIA is then characterized by simulating the gain and IRN without the DSL, which is simulated alone and its performance evaluated. Then, the DSL is included in the CCCIA and new simulations are performed to compare the performance of the CCCIA with and without the DSL. Monte Carlo simulations are also presented to validate the results obtained in the presence of process mismatch, followed by the final circuit layout.

4.2 Amplifier Comparison

As seen in Chapter 3, the original pre-amplifier of the NDT system described was modified to be able to perform in a differential manner. These modifications include the use of additional biasing circuitry and a Common-Mode Feedback (CMFB) circuit, in order to supply the correct biasing voltages and keep the output at a desired Common-Mode (CM) voltage, respectively. To be sure that these alterations do not negatively affect the performance of the final amplifier, both are simulated and compared, regarding their gain, phase, phase margin and IRN.

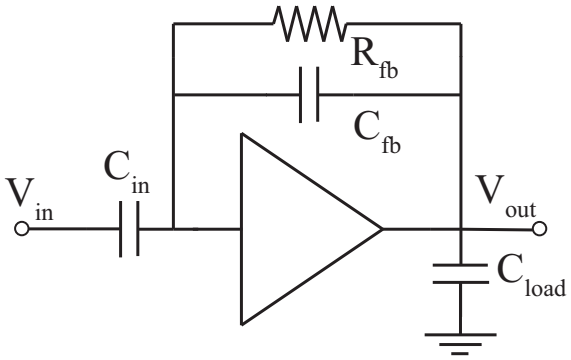


Figure 4.1: Feedback configuration used in simulations.

Both amplifiers have a supply voltage of 3.3 V and are set to have a CM voltage of half the supply. They are included in a capacitive feedback configuration, as shown in Figure 4.1, with the input C_{in} and feedback C_{fb} capacitors set to 10 pF and 1 pF, respectively, to achieve a gain of 20 dB. The load capacitor C_{load} was set to 2 pF, while the feedback resistor R_{fb}, here present to allow the DC voltage feedback, as explained in the previous chapter, was set to 1 TΩ.

With the referred parameters the stability of the amplifiers is evaluated by checking their phase

margin, open-loop gain and phase. Figure 4.2 shows the the open-loop gain of both the original single-ended and the final fully-differential amplifiers. Both present similar gain performances with a DC gain of 85 dB and a bandwidth of about 20 kHz for the original amplifier and 50 kHz for the final amplifier, defined by the frequency where the gain drops 3 dB below the DC gain. Also, the original amplifier has a unity-gain frequency of about 200 MHz, while the final amplifier has a unity-gain frequency of 400 MHz.

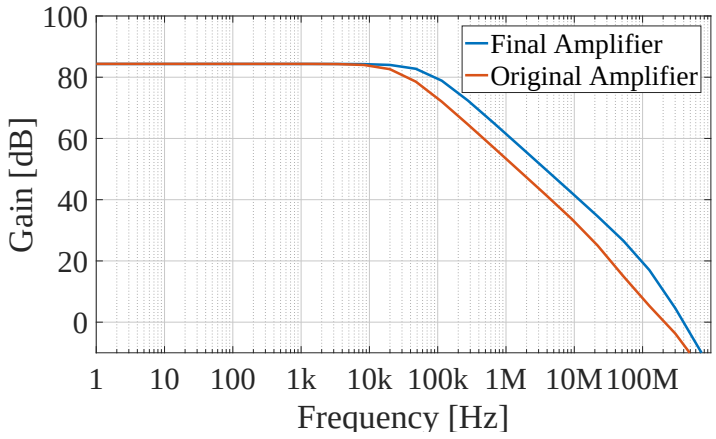


Figure 4.2: Open-loop Gain.

To be able to define the phase margin of both amplifiers, their phases were also simulated for the same conditions and are shown in Figure 4.3. For both amplifiers, their phase margin is found by measuring the phase at their unity-gain frequency and then, by taking this value and calculate how much phase deviation is allowed before the signal achieves a 180º phase shift.

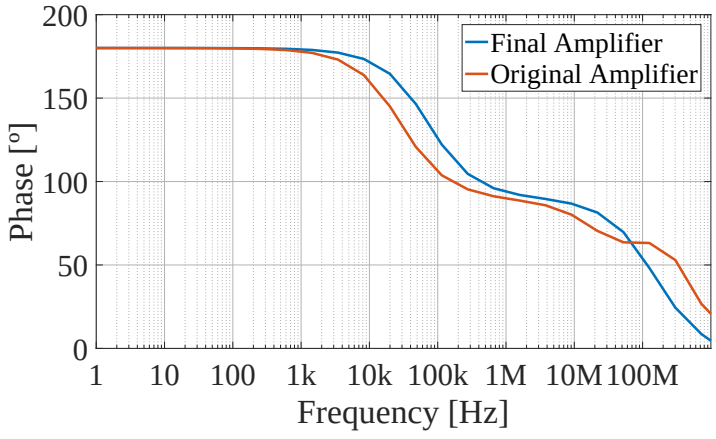


Figure 4.3: Open-loop phase.

For the original amplifier, at its unity-gain frequency, it presents a phase 58º above the point of instability, thus it has phase margin of 58º. As for the final amplifier, at its unity-gain frequency, it has a phase of 20º, thus a phase margin of the same value, which is near instability. For this reason, a 200 Ω resistor in series with a 2 pF capacitor is added to each output of the amplifier to

compensate the phase margin, achieving a value of 56°.

Now, their IRN is analyzed and since additional circuits were added to the final amplifier to perform the conversion to fully-differential, namely the additional biasing circuits and CMFB, new noise contributions are added to the final amplifier that must be considered and kept as low as possible to maintain the noise performance. As shown by Figure 4.4, both amplifiers show the same noise floor of just 2 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. However, the additional circuits increase the IRN at low frequencies, as the final amplifier presents 185 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, while the original one presents 170 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, at 1 Hz. The increased IRN may not present a significant problem, as it still is similar to the original IRN. Also, Chopper Stabilization is applied to this amplifier, which will mitigate this effect.

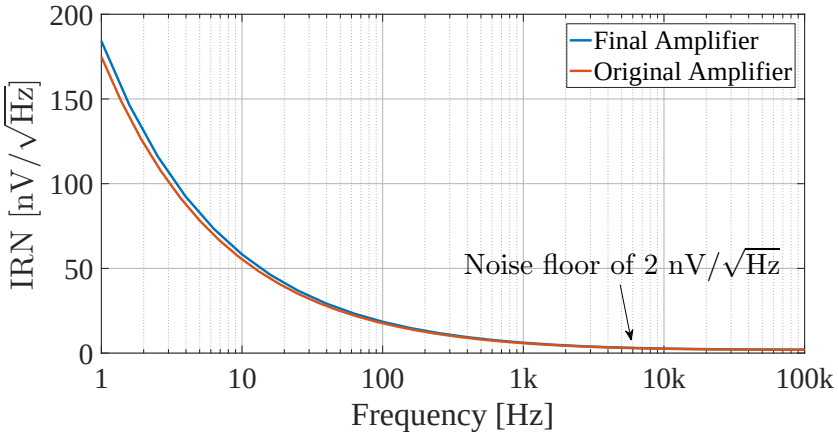


Figure 4.4: IRN analysis.

To finish this analysis, an AC analysis was also carried out to evaluate the gain response of the capacitive feedback configuration (Figure 4.5). As expected, the gain performance is very similar and has a value of 20 dB at the amplifiers pass-band. The original amplifier presents a bandwidth of about 20 MHz, while the final amplifier presents a bandwidth of about 30 MHz.

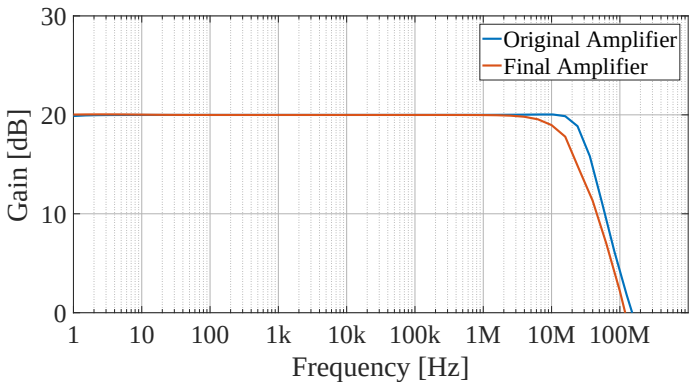


Figure 4.5: IRN analysis.

In an overall view, the conversion process from single-ended to fully-differential is accom-

plished without major disturbances in the amplifier performance. This is crucial because, as already referred, the original amplifier was optimized to achieve low noise and without carefully planed modifications this optimization process could have damaged, which was not the case.

4.3 Capacitively Coupled Chopper Instrumentation Amplifier

In this section, simulations were performed to evaluate the behavior of the final CCCIA circuit. To start this analysis, the CCCIA gain, IRN stability parameters were simulated for the CCCIA without the DSL. Then, the DSL is characterized, regarding its behavior for different input resistances, and is added to CCCIA to evaluate its effects, by comparing it to the CCCIA without the DSL. The effect of the high-pass capacitors is also tested, since they define the maximum input DC signal that can be attenuated by the DSL. To finish, Monte Carlo simulations are performed to verify the obtained results and the final system layout is presented.

4.3.1 CCCIA Characterization

In Chapter 3, the CCCIA was described with focus on its amplifier, feedback paths and DC cancellation. In this section, the CCCIA is characterized to evaluate the correct functioning of the circuit regarding the gain, IRN and DC cancellation. Here, the final amplifier is used in the capacitive configuration already discussed, with the inclusion of Chopper Stabilization and without the DSL circuit, as seen in Figure 4.6(b). To perform this evaluation, two load capacitors of 1 pF were used in each output branch of the differential amplifier and the input signal is produced by simulating the behavior of the sensor configuration with two 1 kΩ resistors in series, that are biased by a current source, as shown in Figure 4.6(a).

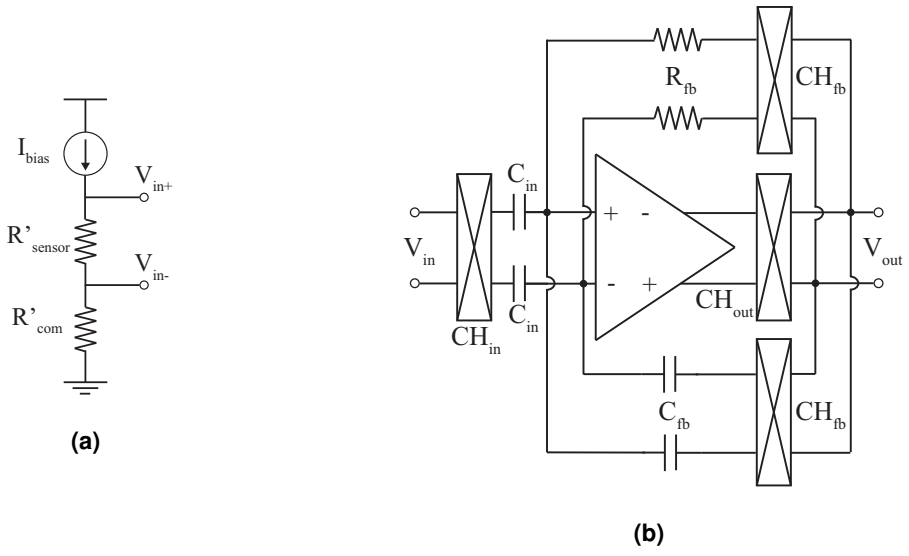


Figure 4.6: CCCIA test setup: (a) input signal generation; (b) Circuit of the without the DSL.

In this test, chopper modulators are present, which are clocked circuits that have a periodically changing DC operating point: in half the period, a pair of switches is closed while the other is opened, and in the other half they switch roles. This changing DC operating point prevents the usage of the typical AC and noise analysis to evaluate both gain/phase and IRN, respectively. To overcome this problem the Periodically Steady-State (PSS) analysis is used. This analysis allows the determination of the periodic operating point by performing an initial transient analysis and then by performing iterations, in each certain nodes of the circuit are stimulated and their time response evaluated. These responses are then compared to the ones of the previous iteration and a conversion norm is established. The process stops when the conversion norm achieves a certain threshold. At the end, the information generated regarding the periodic operation point can be used to perform small-signal analysis, such as AC and noise analysis.

To perform a PSS on clocked circuits, such as this one, several parameters must be chosen. The first one is the fundamental frequency f_{fund}, which corresponds to the minimum common multiple of all frequencies present in the circuit. Then, the number of harmonics of f_{fund} to be calculated or a frequency range must be set, to allow enough information to be created for the subsequent small-signal analysis.

Following the PSS analysis, a Periodically AC (PAC) and Periodically Noise (PNOISE) analysis are performed to evaluate the gain and IRN of the circuit, respectively. In this case, the fundamental frequency f_{fund} of the PSS was set to the chopper frequency f_{chop} that is 10 kHz. This frequency was chosen since it is above the flicker noise corner of the final amplifier and allows a Nyquist rate of 5 kHz, above which Chopper Stabilization is no longer necessary and it can be switched off. As for the input signal, it was removed during the PSS analysis to allow only the clock signals to influence the periodic operating point of the circuit. The PAC analysis was set to have a current signal magnitude I_{bias} (Figure 4.6(a)) of 1 mA, which results in 1 V input voltage signal, as the resistor modeling the sensor has a value of 1 kΩ.

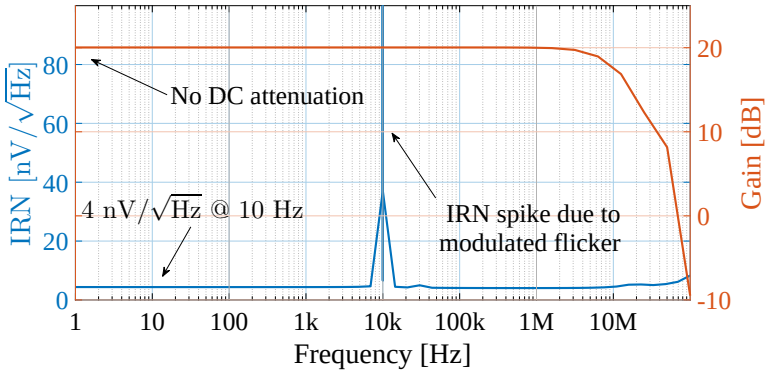


Figure 4.7: Gain and IRN of the CCCIA without the DSL.

As can be seen from Figure 4.7, the circuit without the DSL achieves a low-pass characteristic

with 20 dB at its pass-band and a cut-off frequency of about 7 MHz. The gain specification is met, however the cut-off frequency is 3 MHz bellow the specification of 10 MHz. Also, without DSL, the input DC components are also amplified with a 20 dB gain, which will saturate the amplifier, as they can be up to 1 V. As for the IRN, with this configuration an almost constant value of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ is achieved, even at very low frequencies, except for the spike present at 10 kHz, which represents the modulated flicker noise component. However, this spike presents no problems for the circuit, since with chopper turned on, only signals up to 5 kHz will be used and this modulated flicker noise can be filtered out. With higher frequencies, the chopper modulators are turned off, as it would not be advantageous to use them, because of the very low noise floor.

4.3.2 The DC Servo Loop

The above subsection has shown that the CCCIA presents very low noise in low frequencies and the intended 20 dB gain in the amplifier's pass-band. However, it also amplifies DC signals instead of attenuating them as wanted. For this reason, the DSL is a must. As discussed in Chapter 3, it is composed by a fully-differential Miller integrator that uses the same final amplifier, a 10 pF feedback capacitor C_{int} and a very large resistor, which together set a very narrow bandwidth, only capable of amplifying DC signals. The integrator extracts the output DC component of the CCCIA, up-modulates it to the chopper frequency f_{chop} and feeds it into the input node of the main amplifier by means of an high-pass capacitor C_{hp} to achieve negative feedback, thus rejecting the input DC component.

In this subsection, the DSL is first analyzed isolated from the CCCIA to evaluate its characteristics regarding stability and the influence of the input resistor on the unity-gain frequency. Then, the DSL is included in the CCCIA (Figure 4.8) and its impact is checked and compared to the CCCIA without it. Also, the influence of the high-pass capacitor C_{hp} on the amount of DC attenuated and IRN is analyzed.

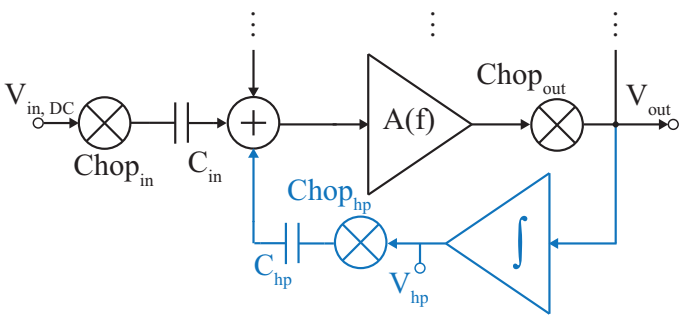


Figure 4.8: Inclusion of the DSL in the CCCIA.

Integrator Characterization

The fully-differential Miller integrator, shown in Figure 4.9, is set up with 1 pF load capacitors to perform a stability and AC analysis with a 1 V input differential signal. For the AC analysis, the input resistor R_{int} was swept from 10 kΩ to 100 GΩ, to check the resistance value needed to create a sufficiently narrow pass-band, to allow only the DC to be amplified by the integrator.

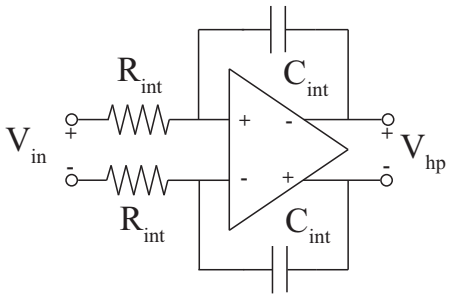


Figure 4.9: Schematic of a fully-differential Miller integrator.

From Figure 4.10, one can check that the unity-gain frequencies vary from about 0.2 Hz up to 2 MHz, for 100 GΩ and 10 kΩ input resistor R_{int}, respectively. In Chapter 3, unity-gain frequency of the integrator was set to about 1 Hz to ease the capacitor ratio C_{hp}/C_{fb} in order to set the system high-pass pole frequency to 2 Hz (Table 3.7).

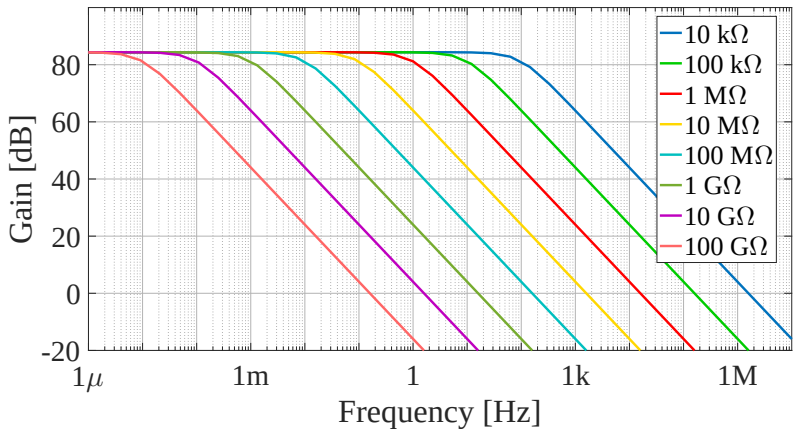


Figure 4.10: Variation of the cut-off frequency of the integrator with the input resistance.

From calculations and from Figure 4.10, one can find that to achieve such low frequency, a resistance of 15 GΩ must be used, which is a difficult task to perform in integrated circuits, as such resistors occupy very large chip areas. As proposed before, a pseudo-resistor is used to achieve such resistance. Here, the gates of the pseudo-resistors were connected to the supply voltage to ensure the maximum resistance. This way the unity-gain frequency of the integrator is ensured to be lower than the one designed. A new AC analysis was made to check the unity-gain frequency of the integrator and it was found that it is about 10 mHz, with the pseudo-resistor. To

check the stability of the integrator, a stability analysis was performed with the pseudo-resistor. From its stability summary, it was verified that its phase margin was about 62 º.

CCCIA with DSL

The simulations made on the CCCIA shows that it requires the DSL to place an high-pass pole on the system to be able to block input DC components. It was also seen that to accomplish this, the DSL uses a fully-differential Miller integrator that has a unity-gain frequency that varies from 0.2 Hz up to 2 MHz, for an input resistor of 100 GΩ and 10 kΩ, respectively.

Now, the DSL is included in the CCCIA (Figure 4.8) and its effects on the AC response and noise are evaluated. The test setup is somewhat similar to the previous ones, with the exception that initial conditions were set to help the PSS analysis to converge more easily. The initial conditions are needed, since the DSL introduces a very low-frequency high-pass pole and, therefore, the time constants of the circuit are too large, which lead to very large transients that take a very long time to settle. This means that to inspect the DC attenuation in the time domain, a very long time has to be simulated, which is not practical.

The initial conditions indicate that circuit nodes have specified voltage values at the begging of the simulation, which are the values those nodes achieve in the steady state. They were set for the outputs of the integrator, V_{hp+} and V_{hp-} , and were found by performing a sequence of n transient simulations, in each the values of V_{hp+} and V_{hp-} were checked. By considering the values of V_{hp+} and V_{hp-} in the $n-1^{th}$ simulation, these values can be set as initial conditions for the next transient simulation, n, thus skipping the transient of simulation $n-1$. At the end of the n^{th} simulation, the outputs of the integrator reach the steady state, where there is no DC, with values of 1.9 V and 0.9 V for V_{hp+} and V_{hp-}, respectively. This way, one can skip the transient and is able to verify the DC attenuation in time domain, as well as help the PSS analysis to converge to the steady state solution, where no DC signal is present.

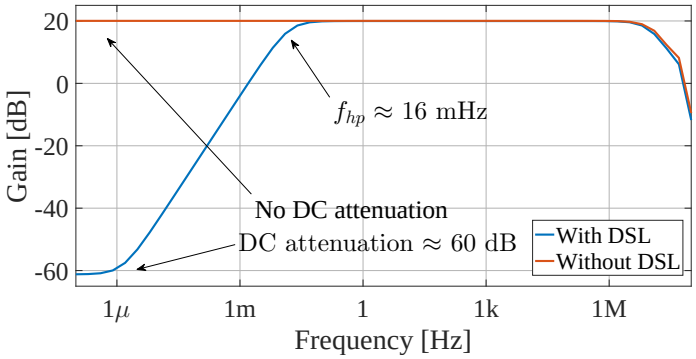


Figure 4.11: Gain of the CCCIA with the DSL.

With the referred setup, the PSS computes the periodic operation point of the circuit and allows the PAC analysis to be performed. In Figure 4.11, the results of the PAC analysis are shown in

contrast with the ones of the CCCIA with no DSL. The DSL is able to place the high-pass pole in a frequency of 16 mHz and attenuate DC signals by 60 dB.

Figure 4.12 shows a transient simulation of the output signal V_{out}, with and without the DSL, for an input signal with a DC component of 200 mV and 100 mV, respectively, and a signal amplitude of 100 mV and 10 mV, also respectively. In both cases, the same initial conditions ($V_{hp+} = 1.9$ V and $V_{hp-} = 0.9$ V) where used to skip the large transient of the circuit. As can be seen, the DSL allows an almost total cancellation of DC components up to 200 mV, which are attenuated 60 dB (Figure 4.11). Without the DSL, 100 mV DC components were injected at the inputs and were amplified by 10 times, as expected, which resulted in differential offset of 1 V, between each of the individual signals that compose the differential output, namely V_{hp+} and V_{hp-}.

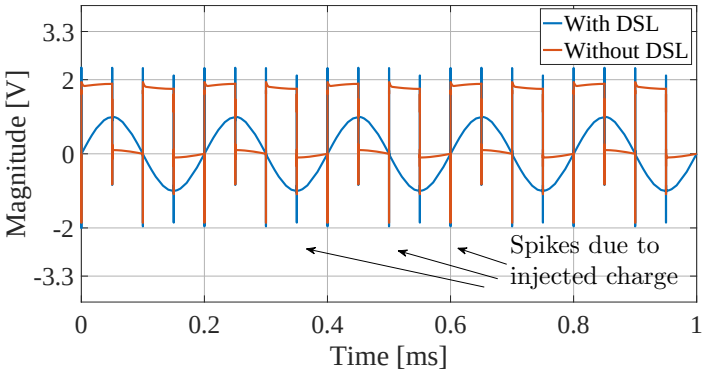


Figure 4.12: Transient response the output V_{out} of the CCCIA.

As all chopper modulators are driven by the same clock, their switches can be grouped in two groups, where in Group 1 are the switches that are turned on by the first clock phase ϕ_1 and the on Group 2, the ones that are turned on by the second clock phase ϕ_2. This way, two states are defined, where State 1 corresponds to the moment when switches of Group 1 are turned on and when switches of Group 2 are turned off, and State 2 corresponds to the moment when switches of Group 1 are turned off and when switches of Group 2 are turned on. Simulations were performed in both states to evaluate the stability of the circuit, where both of them present similar stability performance, shown in Figure 4.13.

Stability summary indicates a phase margin of 87.5º for each state. However, the behavior of each separate state may not reflect the final behavior of the CCCIA, where modulators are constantly switching from one state to another. Still, the fact that the PAC analysis of the CCCIA presented no gain overshoot and each state has phase margin of 87.5º are positive indicators of the stability of the circuit.

As for the noise analysis, the DSL increases significantly the IRN to 43 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, about 10 times the IRN of the CCCIA without it, at 1 Hz (Figure 4.14). However, at 10 Hz the IRN is increased about 3 times and the noise floor is kept at the same level. This happens because the amplifier used in the integrator is a copy of the one used as main amplifier in the CCCIA thus,

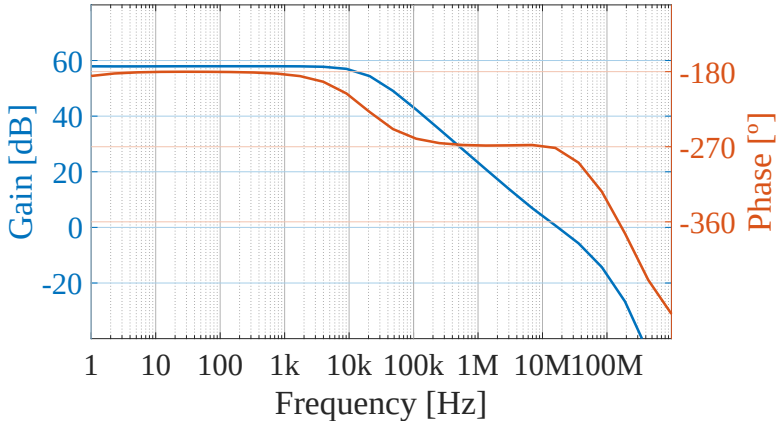


Figure 4.13: Stability analysis results: loop gain and phase.

it has a noise contribution in the same order as the main amplifier. Nonetheless, it was found that this contribution can be mitigated by reducing the high-pass capacitor C_{hp}, with the cost of reducing the maximum sensor DC signal level that can be attenuated, which is given by equation 3.12. Further analysis of the effects of these capacitors are made ahead.

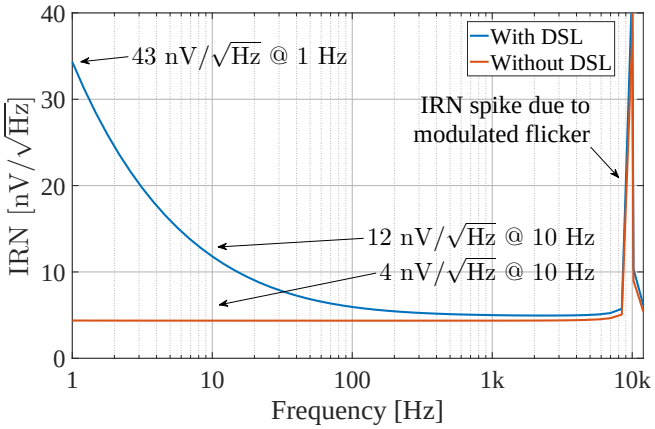


Figure 4.14: IRN analysis of the CCCIA with the DSL.

Impact of High-pass Capacitors

The high-pass capacitors C_{hp} have a major impact on the circuit, as they establish the relation between the high-pass pole frequency of the CCCIA and the unity-gain frequency of the integrator (3.11), as well as set the maximum input DC biasing signal level that the circuit can reject, for a given output voltage of the integrator (3.12). For this circuit, the output voltage of the integrator V_{hp} was set to 1 V, thus (3.12) sets the maximum input DC biasing signal amplitude to C_{hp}/C_{in}, that is 200 mV, as C_{hp} and C_{in} are set to 2 pF and 10 pF, respectively.

As seen from Figure 4.15, the capacitor ratio C_{hp}/C_{in} as also an impact on the IRN, which increases for increasing C_{hp}. This is problematic, since there is a trade-off between IRN at low-

frequencies and the maximum DC that can be attenuated. For example, to be able to attenuate 1 V of DC input signal, the DSL alone would have to implement high-pass capacitors C_{hp} equal to the input capacitors C_{in}, that is 10 pF. However, such capacitors would lead to a IRN similar to the one of the amplifier without Chopper Stabilization (Figure 4.4), which would invalidate all the efforts made in this work to reduce the IRN.

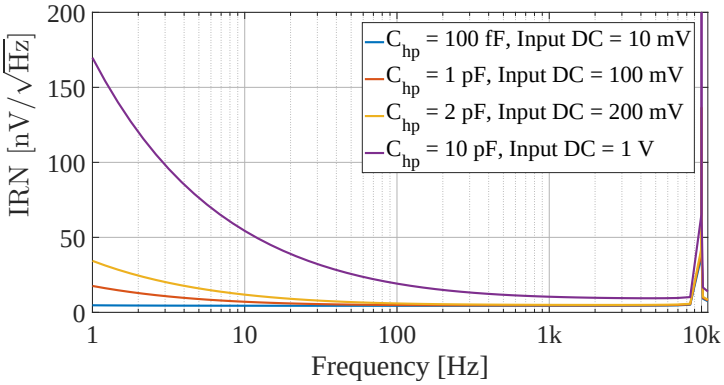


Figure 4.15: Impact of the variation of C_{hp} on IRN.

The referred trade-off occurs because the capacitor ratio C_{hp}/C_{in} sets the maximum DC input that can be attenuated, which is related to the maximum signal contribution of the DSL that is fed into the input of the main amplifier. This is also true for noise components injected by the integrator amplifier, which are equal to the main amplifier. Therefore, if $C_{hp} = C_{in}$, the noise contribution of the integrator amplifier is the same of the main amplifier without chopper. This is the reason why C_{hp} is set to 2 pF, as it allows a maximum DC 200 mV to be attenuated, as well as to limit the noise contribution of the integrator's amplifier to $C_{hp}/C_{in} = 2/10$, that is 20% of its actual noise contribution.

4.4 Monte Carlo Simulations

The simulations performed in the previous section only considered the nominal corner, thus their results may not reflect the real working conditions, as these are always affected by numerous factors that were not taken into account, such as process mismatch.

To be able to predict the behavior of the system in multiple conditions, 500 Monte Carlo runs were performed, in which the band-pass gain, DC attenuation and IRN were evaluated. To perform yield calculation, the metrics just referred were used, having as specifications 20 dB, 40 dB and 10 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, respectively, which where calculated using the PSS, PAC and PNOISE analysis, on top of Monte Carlo.

Figure 4.16 shows the result of the 500 runs for the gain of the CCCIA, in which, for sub-hertz frequencies, the DC components have an average attenuation of 60 dB, however in some cases the attenuation is lower, but never below 40 dB. As for the pass-band gain, it has an average of

20 dB, with the exception of some cases where the signal is attenuated more than 40 dB, which indicates that in these cases the circuit does not work.

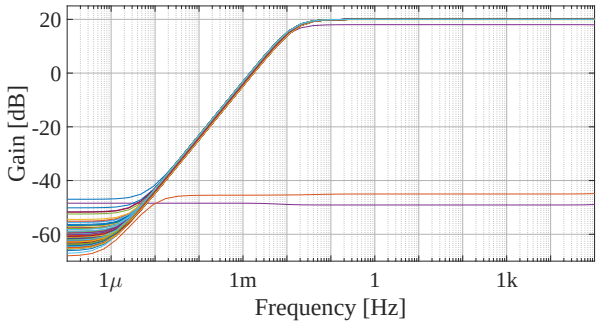


Figure 4.16: Monte Carlo simulations: CCCIA gain.

As for the noise performance shown in Figure 4.17, for all the tested cases, the circuit presents an IRN below 20 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz, with the exception of just one case, which achieves 65 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, thus not meeting the specification. At 1Hz, in all tested cases with the exception of one, the IRN is below 40 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

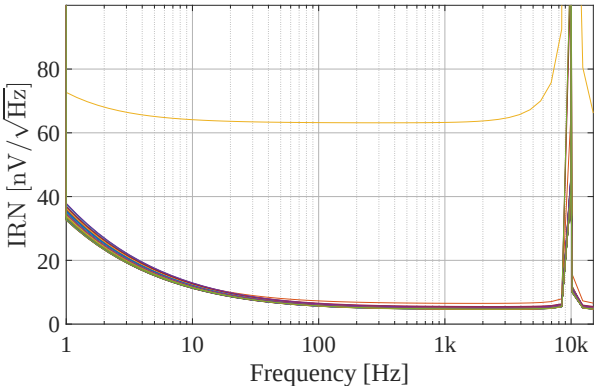


Figure 4.17: Monte Carlo simulations: IRN of the CCCIA.

In these Monte Carlo runs, PSS analysis were made to allow the execution of the PAC and PNOISE analysis. As the PSS analysis uses iterative methods to converge to a solution for the periodic operating point, in some cases tested in Monte Carlo, it did not converge to a solution. This resulted in a failed test, as the simulator could not evaluate the gain and IRN of the circuit, which contributed negatively to the yield calculation, resulting in a value of 71%, which does not really represent the ratio between cases were the specifications were not met and cases that the specifications were met. However, a PSS analysis that could not converge to a solution does not necessarily means that the circuit does not work, it only means that that case could not be evaluated. For this reason, the yield was manually calculated by discarding the cases where the PSS did not converge and take only into account the cases that could be evaluated (362 cases) and and the cases that not met the specifications (5 cases), leading to a yield of 98.6%.

4.5 Circuit Layout

In this section, the layout of the key elements of the CCCIA are presented. In Figure 4.18, the layout of the developed CMFB circuit is shown, where the differential pairs, current mirrors and biasing circuits are highlighted.

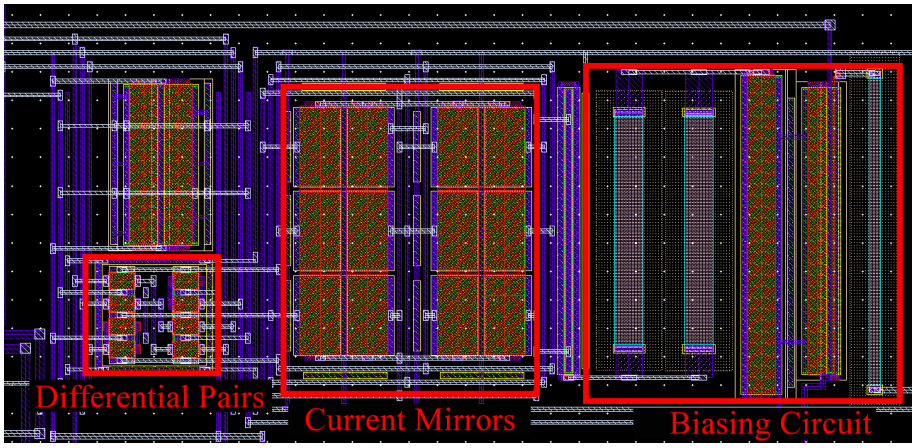


Figure 4.18: Layout of the CMFB circuit of the final amplifier.

In Figure 4.19, the final amplifier (the one used as both main amplifier and the integrator amplifier) is shown and their transistors are indicated.

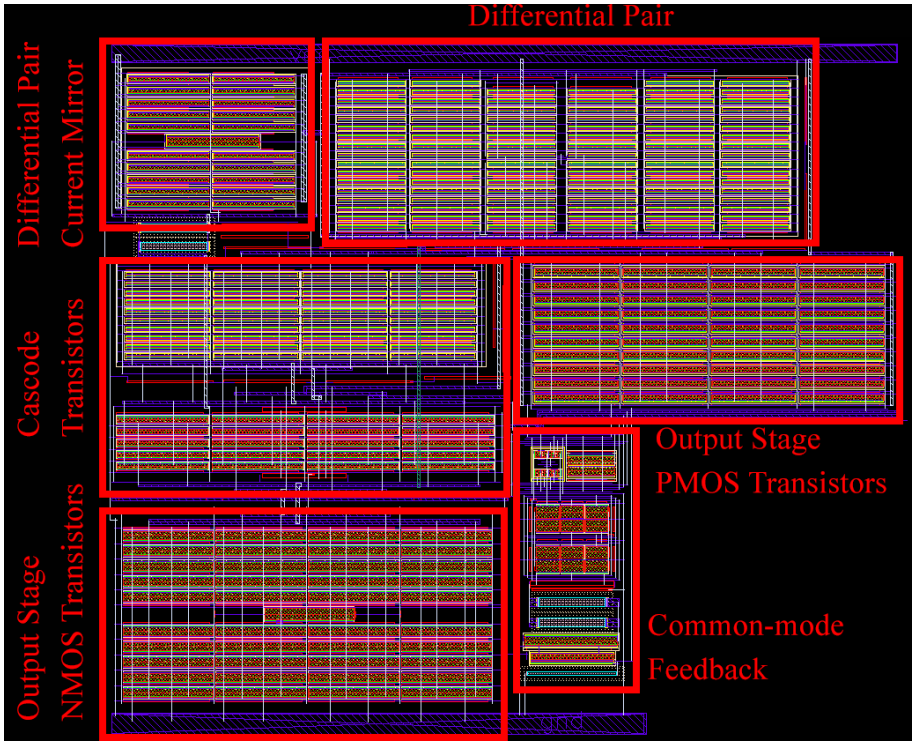


Figure 4.19: Layout of the final amplifier.

Finally, the layout of the complete CCCIA is shown in Figure 4.20. In the same figure, the

integrator amplifier, chopper modulators and all the capacitors are highlighted.

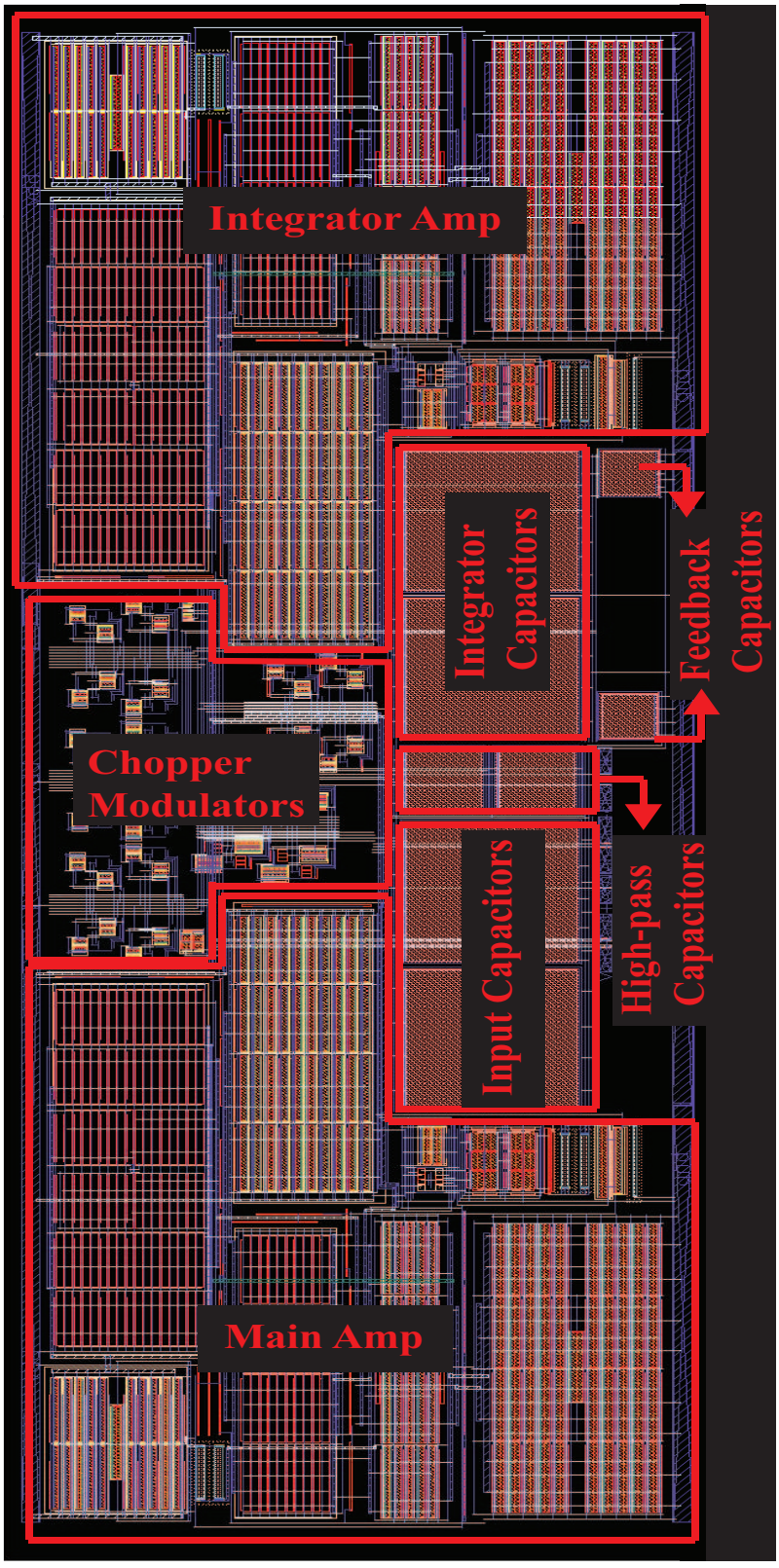


Figure 4.20: Layout of the CCCIA.

4.6 Summary

In this chapter the simulated results of the developed CCCIA are presented. It begins by comparing performances of the original single-ended amplifier and the final fully-differential. It was verified that the final fully-differential amplifier achieves an open loop gain of 85 dB, with a bandwidth of 50 kHz, a phase margin of 56º and an IRN of 185 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 Hz, which are results very similar to the ones of the original amplifier.

The final fully-differential amplifier was included in the CCCIA and this last was tested with and without the DSL, which is used to cancel the input DC components. Without the DSL, the CCCIA present a low-pass characteristic with 20 dB and a cut-off frequency of 7 MHz. As for its IRN, it presents an almost flat characteristic with a value of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ from 1 Hz up to 6 kHz. Since with this configuration, DC components are also amplified with a 20 dB gain, the DSL must be included to attenuate them. The DSL makes use of an integrator that can vary its unity-gain frequency from 0.2 Hz up to 2 MHz by using input resistors with resistances of 100 GΩ down to 10 kΩ. Such low unity-gain frequencies are required to place the high-pass pole of the CCCIA in a sub-hertz region, in order to reject only DC. By including the DSL that uses a pseudo-resistor, the CCCIA is again tested and it presents an high-pass pole frequency of 16 mHz, a cut-off frequency of 5 MHz, a gain in its pass-band of 20 dB and an attenuation of 60 dB for DC signals up to 200 mV. As for its IRN, it is worse than the CCCIA as it has a value of 12 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz. Due to the very low-frequency pole, the CCCIA presents very large time constants that lead to very large settling time upon variations in DC components. To skip these very large transients, initial conditions are set in the simulations.

Monte Carlo simulations were used to validate the previous results. By excluding the cases where the PSS analysis does not converge to a solution, the CCCIA presents an yield of 98.6%.

To finish, in Table 4.1 the simulated results are compared to the specifications. As can be seen, the simulated bandwidth is half the value of the specification set. Both IRN and DC attenuation exceed the expectations set by the specifications. As for the phase margin, it was tested for the states defined in Subsection 4.3.2, obtaining a value of 87.5 °, which may not indicate the stability of the circuit witch chopper modulators switching.

Table 4.1: Circuit specifications and results.

Parameter	Specification	Simulated
Open Loop Gain [dB]	60	58
Close Loop Gain [dB]	20	19.9
Bandwidth [MHz]	10	5
Phase Margin [º]	60	87.5
IRN @ 100Hz [$\mathrm{nV}/\sqrt{\mathrm{Hz}}$]	$<$20	6
DC Attenuation [dB]	40	60

5

Conclusions

The present work addresses an Eddy-Current (EC) Non-Destructive Testing (NDT) system that uses Magneto-Resistive (MR) sensors. This system also makes use of an Application Specific Integrated Circuit (ASIC) that multiplexes and bias the sensors, as well amplify the signals they produce. The work addresses two problems that the ASIC present: large flicker noise when using low signal frequencies, which are required to achieve higher penetration depths, and large sensor DC biasing signals that saturate the pre-amplifier.

To mitigate flicker noise, two techniques are presented in Chapter 2, Autozero and Chopper Stabilization. In short, Autozero is a sampling technique that periodically samples and holds unwanted signal components, namely flicker noise and offsets, in a first half of the period, and in the second half, it subtracts the held components from the signal input, thus removing them. Since this technique uses sampling, it introduces aliasing, which increases the noise levels of the system. Moreover, as it a sampling technique, it is more suitable for already discrete-signal systems.

This way, Chopper Stabilization was chosen to be implemented, as it is a full-analog techniques that modulates the signal to an higher frequency, before being exposed to noise and offsets originated by the amplifier present in the ASIC. This way, the spectral components of signal and noise are not overlapped and, after being amplified, the signals are demodulated, returning to their baseband, as noise and offsets are up-modulated, thus being removed.

To accomplish the referred modulations and demodulations, chopper modulators are designed by using four switches, triggered by opposite clock phases, that periodically switch input signals, producing a signal equivalent to the multiplication of a given signal by a square wave. Typical modulators are implemented with simple MOS transistors that inject charges that make up their channels onto their terminals. These charges are associated to a noise current that, when injected into high impedance nodes, originate significantly high noise voltage levels. In a first approach, a typical chopper implementation was tested by placing the modulators in the inputs and outputs of the pre-amplifier of the ASIC. This implementation could not be put to work, as it present huge noise levels with that configuration. Some testing and research lead to believe that this noise is associated to the noise current produced by the modulators placed at the high impedance input node of the amplifier, thus creating this effect. Also, due to the fact that this input node lies between two capacitors, that implement the capacitive feedback configuration, and a very large resistor, used to allow the feedback of the CM voltage, it is believed that not enough current is allowed to flow to charge and discharge the capacitances in this node, therefore this configuration in this circuit could not work.

To overcome the problem referred, another chopper topology, name Capacitively Couple Chopper Instrumentation Amplifier (CCCIA), was implemented. This topology builds the capacitive feedback within the chopper path, thus the input modulator is placed before and after the input capacitor, which avoids having the noise current of the modulators injected in the high impedance

input node of the amplifier. To implement the CCCIA, the original pre-amplifier was also converted to a fully-differential amplifier to match the differential nature of the modulators and allow larger output voltage swing. The conversion process requires that a Common-Mode Feedback (CMFB) circuit is used to define the output CM voltage, as the input no longer has control of if. This additional circuit was made by using two differential pairs that are unbalanced by the difference between the output CM voltage and the desired value and generates a control current that is mirrored to the differential pair of the main amplifier, thus controlling its tail current and its output CM voltage.

With the implementation of the CCCIA, another problem appears. As the input modulator is placed before the input capacitor, the sensors DC biasing signals are up-modulated and thus, are not block by the input capacitors. This leads to the amplification of DC components, which are significantly large and will saturate the amplifier. To solve the problem, an additional feedback path is implemented, the DSL. The DSL is composed by a Miller integrator that isolates and amplifies the output DC voltage by having a very narrow pass-band. This narrow pass-band is achieved by reducing the integrator unity-gain frequency as much as can be, by implementing GΩ input pseudo-resistors, composed by PMOS transistors in a near cut-off region. This way, the integrator only allows DC signals to be amplified, up-modulated and subtracted from the main amplifier input by means of a negative feedback. This feedback makes use of high-pass capacitors that establish a relation between the integrator output voltage and the maximum sensor DC biasing signal that can be attenuated, as well as a relation between the frequency of the system high-pass pole and the unity-gain frequency of the integrator.

The very high-input resistances used in the integrator that lead to a very low unity-gain frequency, impose very large time constants on the circuit. The large time constants lead to transients that take a very long time to settle, thus when one sensor with a DC voltage value is switched to another with a slightly different DC voltage, a long transient is created and very long time must pass for it to settle.

With the dimensioning done in Chapter 3, the CCCIA targets the amplification of signals with a gain of 20 dB and the attenuation of DC signals up to a maximum of 200 mV. Since the sensors are biased by a 1 V DC signal, the DSL alone is not capable of blocking all this component, therefore, the previously developed cancellation block is used. This cancellation block implements a copy of the sensor biasing circuitry, as well as a dummy sensor, to provide an equal DC biasing voltage as a cancellation signal. The sensors DC biasing voltage and the cancellation signal are applied to the amplifier and, since they are equal, they are seen by the amplifier as a CM voltage, thus being rejected. DC components originated from mismatch between the sensors and cancellation circuit are targeted by the DSL, to allow a complete DC signal canceling.

By simulating the implemented circuit, it was found that the CCCIA presents a pass-band gain of 20 dB, as expected. Its bandwidth is about 5 MHz and its IRN is about 12 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz

and 43 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 Hz. Input DC signals are found to be attenuated by 60 dB. These results are proved by Monte Carlo simulations, where an yield of 98.6% was obtained, when discarding the cases where the PSS analysis did not converge. Regarding stability, it was evaluated for the two states of the circuit, defined by the on and/or off state of the chopper switches. In both states, a phase margin of 87.5º was obtained but gives no guarantees that with chopper switching the circuit does not become unstable. However, this phase margin and the fact that there is no gain overshoot are good indicators of the stability of the circuit. This way, it can be said that the gain and DC attenuation specifications are met, while the requirement of having a bandwidth of 10 MHz was not achieved. However, the IRN obtained at 100 Hz was almost 4 times less than the specification.

To finish, the CCCIA achieves its gain requirements and surpasses the IRN specification, however with the cost of a very high current and die area. The stability of the circuit could not be fully evaluated and it presents a very long settling time, aspects that can compromise the correct functioning of the circuit.

Future work

The developed work makes use of chopper stabilized folded cascode amplifier with a capacitive feedback, to amplify signals from MR sensors, with very low noise.

The MR sensors have a DC biasing component that is canceled within the circuit developed by using a feedback path that includes an integrator with a very low unity-gain frequency, by using pseudo-resistors with a very large resistance. This feedback introduces a very low-frequency high-pass pole that is associated to a very large time constant, which will make the DC signals to take a very long time to be fully attenuated. As a future task, it is proposed to reduce this settling by implementing variable pseudo-resistors, as described in [15], which can vary their resistance, thus varying the pole frequency, accelerating this process. In [20], a mechanism that controls the integrator time constant is implemented. The mechanism senses the integrator output voltage and regulates the resistance of the pseudo-resistors, therefore changing the time constant and the settling time. This mechanism would be another interesting functionality to add to the system of this work in the future.

In the future, different implementations of the DSL should be explored like the VLTC-SC integrator described in [13], which uses switched-capacitors that provide superior precision in gain and superior control of the high-pass pole of the CCCIA, by changing the switching frequency. Also, further testing regarding the circuit's stability must be performed, as well as exploring the problems with the typical chopper implementation of Section 3.3.

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