TÉCNICO LISBOA

# Development and implementation of a device for $LiFePO_4$ batteries state-of-charge estimation

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Thesis to obtain the Master of Science Degree in

## Electrical and Computer Engineering

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# Resumo

As baterias de lítio ferro fosfato ($LiFePO_4$) despontam como uma nova gama de baterias de iões de lítio no mercado de sistemas de armazenamento de energia. É, deste modo, essencial a utilização de métodos precisos e fiáveis para a medição do seu estado de carga.

Após a revisão dos principais métodos de estimação do estado de carga, um novo procedimento com a mesma finalidade é proposto, tendo por base a impedância interna da bateria e um sistema de lógica difusa.

A resposta em frequência de uma bateria de $LiFePO_4$, representando a sua impedância interna, é adquirida por espectroscopia de impedância electroquímica. Devido à relação não-linear desta variável para com o estado de carga, é sugerida uma abordagem por sistemas adaptativos. A impedância interna adquirida representa a entrada de um sistema de lógica difusa, responsável pela estimação do estado de carga da bateria através de uma análise comparativa entre a presente impedância adquirida e impedâncias observadas anteriormente, associadas a certos valores de estado de carga. Para tal, o sistema de inferência difusa é previamente composto, através da aplicação de sistemas adaptativos de inferência neuro-difusa.

Um dispositivo é desenvolvido, através da plataforma Arduino Due e de uma placa de circuito impresso, de forma a que os processos mencionados acima sejam implementados. Os resultados verificados provam que o sistema é capaz de inferir correctamente o valor do estado de carga da bateria, embora seja altamente dependente da quantidade de informação adquirida no passado, informação essa responsável pelo modelo do sistema de inferência difusa.

**Palavras-Chave:** Arduino Due; Bateria de $LiFePO_4$; Espectroscopia de impedância electroquímica; Estimação de estado de carga ; Impedância interna; Lógica difusa; Sistema adaptativo de inferência neuro-difusa.

# Abstract

Lithium iron phosphate batteries ($LiFePO_4$) appear as a new type of lithium ion batteries on the energy storage systems market. Therefore, it is essential to have accurate and reliable methods of measurement of a $LiFePO_4$ battery state-of-charge (SOC).

After revising the main SOC estimation methods, a new technique, based on the internal impedance of the battery and fuzzy logic, is proposed.

The frequency response of a $LiFePO_4$ battery cell, representing its internal impedance, is acquired from an electrochemical impedance spectroscopy (EIS). This acquired variable has a non-linear relationship to SOC, thus, an adaptive methodology approach is taken. The result of the EIS measurement renders the input to a fuzzy logic system designed for the battery SOC estimation, through a comparative analysis between the current impedance measurement and previously observed ones, related to certain values of SOC. To attain this comparative analysis, the fuzzy inference model is previously constructed using an adaptive neuro-fuzzy inference system (ANFIS) technique, based on past EIS measurements, for pre-defined SOC values.

A device is developed, using the Arduino Due platform and an assembled printed circuit board (PCB), so that both processes mentioned above are implemented. The results proved that the implemented system is capable of correctly inferring the battery SOC, although being highly dependent on the amount of past information being acquired, modelling the fuzzy inference system.

**Keywords:** ANFIS; Arduino Due; EIS; Fuzzy Logic; Internal impedance; $LiFePO_4$ battery; SOC estimation.

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# List of abbreviations

**AC** Alternating Current

**ADC** Analog-to-Digital Converter

**ANFIS** Adaptive Neuro-Fuzzy Inference System

**ANN** Artificial Neural Network

**DAC** Digital-to-Analog Converter

**DC** Direct Current

**DDS** Direct Digital Synthesis

**DFT** Discrete Fourier Transform

**EIS** Electrochemical Impedance Spectroscopy

**EKF** Extended Kalman Filter

**EMF** Electromotive Force

**FIS** Fuzzy Inference System

**FL** Fuzzy Logic

**HP** High-Pass

**I2C** Inter-Integrated Circuit

**KF** Kalman Filter

**LCO** Lithium Cobalt Oxide

**LFP** Lithium Iron Phosphate

**LMO** Lithium Manganese Oxide

**LP** Low-Pass

**LSB** Less Significant Bit

**NCA** Nickel Cobalt Aluminum

**NMC** Nickel Manganese Cobalt

**OCV** Open Circuit Voltage

**PCB** Printed Circuit Board

**SCL** System Clock Line

**SDA** Serial Data Line

**SOC** State of Charge

**SRAM** Static Random Access Memory

**RMS** Root-Mean-Square

**VCCS** Voltage Controlled Current Source

# Chapter 1

# Introduction

## 1.1 Motivation

With the rise of autonomous applications in the past years and its predicable growth in the forthcoming ones, comes the ascent of energy storage systems demand. The progress in energy efficiency and the decline of non-renewable sources of energy dictates the advancement in battery monitoring systems. With this in mind, an accurate and reliable measurement of a battery state-of-charge (SOC) is of the most priority to its active management. The SOC value describes the available stored energy in the battery in relation to its full capacity. This indicator is not only relevant from the remaining capacity point of view but also of extreme importance to the lifetime of the monitorized battery seeing that these systems are sensitive to deep discharges or overcharges related to high or too low SOC values, states capable of irreversible damaging the battery. A battery system, depending on the application, is usually composed of more than one cell. With this rises another problem, related to the different usage times for each cell, seeing that in these cases the SOC value is measured for the entire set of cells. This uneven usage leads to rapid ageing of some cells resulting in its destruction, thereby decreasing the lifetime of the entire pack. Therefore, battery SOC estimation methods are of great importance.

This work aims the implementation of a reliable and automatic SOC measurement system. The ultimate goal is to this in a compact and low-cost way.

## 1.2 Objectives

Lithium iron phosphate ($LiFePO_4$ or LFP) battery cells are emerging as a choice when a long cycle life and safety supersedes energy density, such as in electric vehicles. This work addresses the development of a system capable of measuring the SOC value of $LiFePO_4$ cells. In that context, the proposed sytem will be able to measure the impedance profile of a given cell, through the development of an EIS measurement system, later inferring its SOC value using an adaptive neuro-fuzzy methodology. The implemented system will automatically estimate this variable based on previous acquired cell impedance profile measurements.

## 1.3 Thesis Outline

This work is structured as follows:

Chapter 2 introduces the basic concepts of a battery as well as a brief description of $LiFePO_4$ cells characteristics with a comparison between the $LiFePO_4$ and other batteries available on the market.

Chapter 3 reviews usual SOC estimation methods and introduces the proposed inference mechanism.

Chapter 4 describes Fuzzy logic models and Adaptive Neuro-Fuzzy inference systems, later applied in this work.

Chapter 5 details the proposed implemented system, while addressing the working principles of each main block composing the system.

Chapter 6 aims to validate the developed system, described in Chapter 5, based on a proposed case study and its results.

Lastly, the main conclusions of this work are summarized and some considerations about future work are given.

## 1.4 Contribution of this thesis

The main contributions of this work are:

- Development of a novel monitoring system that measures the internal impedance of the battery cell to infer its SOC value, employing adaptive neuro-fuzzy inference techniques.
- Test and validation of the proposed system applied to a $LiFePO_4$ cell.

# Chapter 2

# Batteries

## 2.1 Basic principles

A battery is a device consisting of one or more electrochemical cells that converts the chemical energy stored in its active materials into electric energy through an electrochemical oxidation-reduction (redox) reaction. The battery cell is composed of a positive terminal or cathode, with its composition differing among the types of Li-ion batteries; a negative terminal or anode, usually composed of carbon or graphite on account of its low electrical resistivity; an electrolyte, providing the medium for transfer of charge inside the cell and a separator between the anode and cathode and a separator, preventing physical contact of the electrodes.

During discharge, the cathode, where lithium ions are reduced, accepts electrons flowing from the anode(oxidized), through the electrical load. For rechargeable batteries, this procedure is reverted, resulting in the oxidation of the positive electrode (cathode) and the reduction at the negative electrode (anode). Both processes are represented in Figure 2.1.

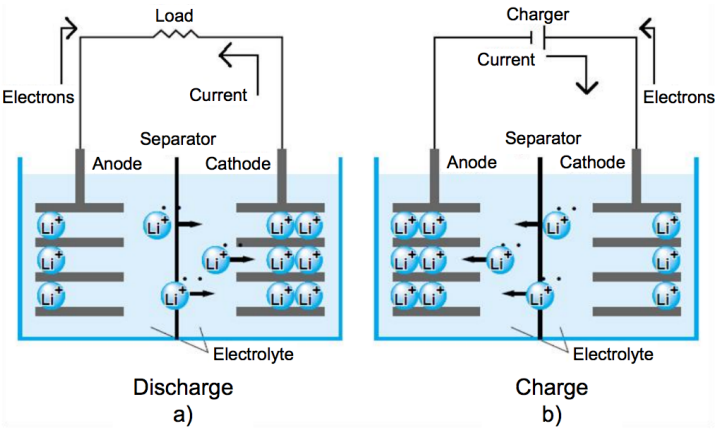



Figure 2.1: Discharge a) and Charge b) mechanisms of lithium ion rechargeable batteries [1].

## 2.2 $LiFePO_4$ batteries

Lithium iron phosphate ($LiFePO_4$ or LFP) cells were first described in [2] by John Goodenough's research group at the University of Texas in 1996 and are emerging as a choice when a long cycle life and safety supersedes energy density, such as in electric vehicles.

The following characteristics of $LiFePO_4$ (LFP) can be summarised: LFP shows an acceptable cell voltage of 3.2 V, depending on the active materials, and it shows exceedingly good safety features. $LiFePO_4$ is chemically stable, non-toxic and shows no thermal runaway. It shows a long cycle life ($>$3000 cycles) and reasonable energy density, (110 to 140) Wh/kg. The rate of self-discharge of a LFP battery is extremely low and it can be stored fully charged.

$LiFePO_4$'s stability comes from its decomposition reaction when exposed to high temperature. Oxygen is not released, at least for temperatures up to 350 °C as it can be seen in Figure 2.2. This happens due to the strong P-O bond in the $LiFePO_4$, therefore, there is a low risk of fire, giving it great safety features when exposed to overcharge or short circuit conditions, when compared to other cathodes, such as: Lithium Nickel Cobalt Aluminium Oxide ($LiNiCoAlO_2$ or NCA), Lithium Cobalt Oxide ($LiCoO_2$ or LCO), Lithium Manganese Oxide ($LiMn_2O_4$ or LMO) .

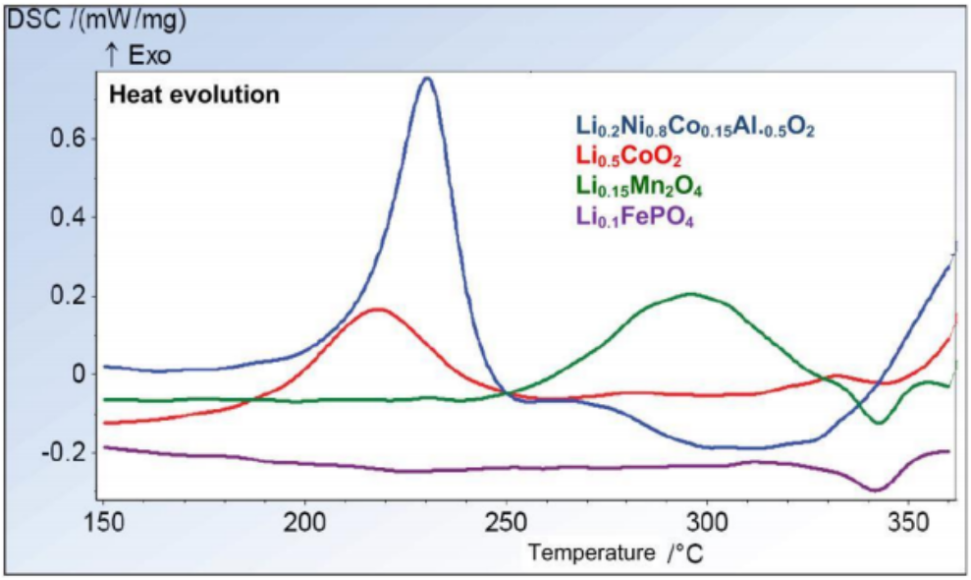



Figure 2.2: Exothermic reaction evolution with temperature [3].

A possible disadvantage of these batteries cells is their voltage level, which is lower than those of the other batteries available on the market. However, as stated previously, this issue is counterbalanced by its enhanced safety, crucial in many applications.

A comparison between $LiFePO_4$ and other positive electrode materials available on the market is presented in Table 1, differing in specific energy density, specific capacity density, cycle life, charging/discharging voltages and peak current, operating temperature and cost.

| Specifications | Lithium cobalt oxide (LCO) | Nickel cobalt aluminium (NCA) | Nickel manganese cobalt (NMC) | Lithium manganese oxide (LMO) | Lithium iron phosphate (LFP) |
|---|---|---|---|---|---|
| Specific energy [Wh/Kg] | 170 - 185 [4] | 145 - 165 [4] | 155 - 185 [4] | 90 - 120 [4] | 100 - 140 [4] |
| Specific capacity [Ah/Kg] | 140 [5] | 180 [5] | 145 [5] | 146 [5] | 170 [5] |
| Cycle life [Number of cycles] | 500 - 1000 [5] | 2000 - 3000 [5] | 2000 - 3000 [5] | 1000 [5] | >3000 [5] |
| Cell Voltage [V] | 3.65 [4] | 3.65 [4] | 3.7 [4] | 3.8 [4] | 3.2 [4] |
| Charge cut-off voltage [V] | 4.2 [6] | 4.2 [6] | 4.2 [6] | 4.2 [6] | 3.65 [6] |
| Discharge cut-off voltage [V] | 2.5 [6] | 3.0 [6] | 2.5 [6] | 2.5 [6] | 2.5 [6] |
| Charge current peak [C] | 0.7–1 C [6] | 0.7 C [6] | 0.7–1 C [6] | 0.7–1 C [6] | 1 C [6] |
| Discharge current peak [C] | 1 C [6] | 1 C [6] | 1 C [6] | 1 C [6] | 1 C [6] |
| Operating temperature [ºC] | (-20) - (60) [7] | (-20) - (60) [7] | (-20) - (60) [7] | (-20) - (60) [7] | (-20) - (60) [7] |
| Safety | Poor [6] | Poor [6] | Moderate [6] | Moderate [6] | Very Good [6] |
| Price ($/kWh) | [1] | 318 [8] | 307 [8] | 375 [8] | 402 [8] |

Table 2.1: Characteristics of the batteries available on the market.

[1] The price ($/kWh) of Lithium cobalt oxide (LCO) was not indicated in [8].

# Chapter 3

# The State of Charge (SOC) Estimating Methods

## 3.1 SOC Definition analysis and it's estimation methods

The ratio of the amount of electrical energy stored in a cell ($Q(t)$) to its maximum capacity ($Q_n$) is usually referred to as the state-of-charge (SOC) of the cell. It can be defined as follows:

$$SOC(t) = \frac{Q(t)}{Q_n} \tag{3.1}$$

State-of-charge determination is an increasingly important issue in energy storage systems in terms of both extending the life of the battery and also knowing the remaining capacity of the battery, crucial for its management. Hence, it is necessary to have methods capable of accurately estimating battery SOC. Its prediction can be performed trough invasive and non-invasive methods. The need for non-invasive and instantaneous methods for the determination of SOC became dominant with remote and or sealed battery technology.

The SOC of the battery is a non-linear function depending on various parameters. Some variables affecting the SOC are temperature, charge-discharge rates, hysteresis, self-discharge, and cell age [9]. Several approaches have been proposed for the SOC estimation and some [10–13] allow a division into three main estimator categories: the direct, the indirect or book-keeping methods, and finally adaptive systems for SOC estimation.

### 3.1.1 Direct methods

Direct measurement methods concern the measurement of battery variables and later relating them to SOC. These include the battery voltage (V), battery impedance (Z) and voltage relaxation time ($\tau$) when a current step is applied. The great advantage of a direct measurement system is that it does not have to be continuously coupled to the battery. The main problem resides in the relation between the measured

battery variable and the SOC under all applicable conditions, including the discharge current values that may suffer a great variation depending on the application, temperatures, storage times, among others [13]. Some direct methods are reviewed, such as the open circuit voltage method, the EMF method and the impedance measurement method.

#### 3.1.1.1 The open circuit voltage method

Voltage measurement is a popular method but it does not produce the most accurate results. The open circuit voltage (OCV) of a battery drops with the decrease of SOC. Thus, its value can be used as an estimate of the battery SOC. To illustrate this relationship, the OCV of a standard $LiFePO_4$ cell as a function of SOC is presented in Figure 3.1.

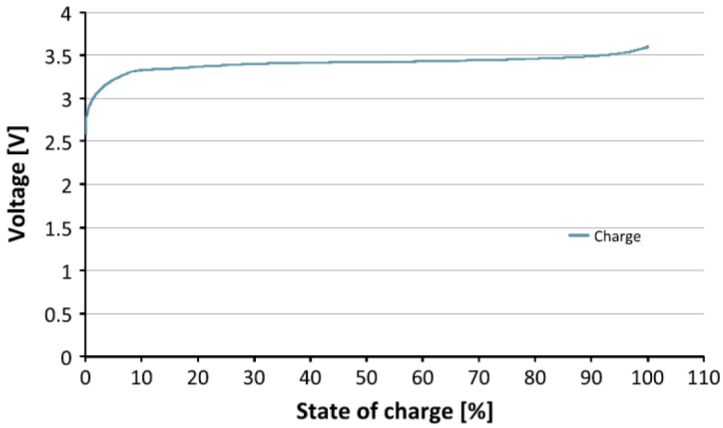



Figure 3.1: Plot of OCV in function of SOC for a $LiFePO_4$ cell [14].

The SOC value can be inferred using one of the following methods: a look-up table, where the values of the measured voltages can be stored and used to indicate the value of SOC or a piecewise linear function, dividing the OCV in intervals corresponding to predefined values of SOC. However, some factors can change the value of OCV for each defined battery SOC, consequently changing the initial OCV-SOC relation. The most significant factors are temperature and the number of cycles (charge/discharge) of the battery. When these parameters change, a small variation of OCV is observed, thus changing the OCV-SOC relation, this way providing an inaccurate value for the battery SOC.

#### 3.1.1.2 The EMF method

EMF denotes electromotive force. The EMF of a cell is equal to the cell terminal voltage when no current flows and the voltage has relaxed to its equilibrium value. Otherwise, the EMF is proportional to the cell terminal voltage and its relation to SOC does not change throughout the charging/discharging cycling of the battery, with minimum dependency on the battery's age and temperature, if the SOC is expressed as a function of the cell capacity [13].

There are three methods of measuring the EMF: voltage relaxation, linear interpolation and linear extrapolation. The first method is based on the relaxation of the battery terminal voltage to the EMF value after interrupting the current flow. This is a slow process, particularly when the battery capacity

is at a low level. In addition to this, there is an impreciseness in defining when the battery voltage has fully relaxed. The second method, *linear interpolation*, is graphically represented for a lithium ion battery in Figure 3.2, showing that the battery terminal voltage, $V_{ch}$, during charging, is higher than the EMF , and lower than the terminal voltage ,$V_d$, during discharging. With this method, the EMF is given by the average voltage obtained between $V_{ch}$ and $V_d$, when the absolute value of the charging current is equal to the absolute value of the discharging current.

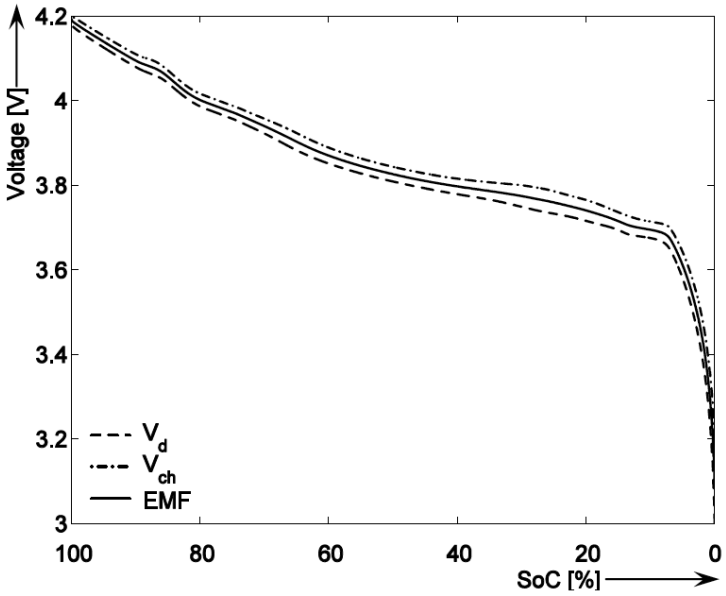



Figure 3.2: EMF curve obtained through linear interpolation [15].

The third and final method, *linear extrapolation*, is based on the measurement of different terminal voltages obtained with different charging or discharging currents at the same SOC. With the measured values, a polynomial fit relating the terminal voltages as function of the flowing current is established. This polynomial is used to extrapolate the voltage value associated to a zero current value of flowing current, illustrated in Figure 3.3, corresponding to the relaxation of the voltage to its equilibrium value, the EMF.

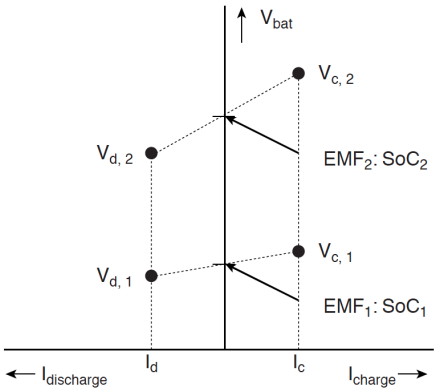



Figure 3.3: EMF curve obtained through linear extrapolation[13].

The SOC of the battery is later estimated using the same methods previously described in 3.1.1.1,

through a look-up table or a piecewise linear function.

#### 3.1.1.3 Impedance measurements method

Electrochemical impedance spectroscopy (EIS) is an experimental technique with the purpose of characterizing electrochemical systems as a function of frequency. This method measures the impedance of a system over a defined range of frequencies, hence the frequency response of the system. The impedance data obtained by EIS is usually represented graphically in a Nyquist plot or a Bode plot. Bode plots express the impedance magnitude and phase angle in relation to frequency. A Nyquist plot, or complex plane, expresses the imaginary impedance versus the real impedance of the system.

Impedance is measured in potentiostatic mode or galvanostatic mode. In potentiostatic mode, an AC potential is imposed to a cell and its response current is measured. In galvanostatic mode, impedance is measured imposing an excitation current to the cell, thereby measuring its response potential. In galvanostatic mode, the excitation current, as a function of time, is stated as:

$$i(t) = I_0 \sin(\omega t) \tag{3.2}$$

where $i(t)$ is the current at the time instant $t$, $I_0$ is the amplitude of the signal, and $\omega$ is the angular frequency.

The response signal, $u(t)$, is shifted in phase ($\phi$) and has an amplitude $U_0$:

$$u(t) = U_0 \sin(\omega t + \phi) \tag{3.3}$$

Through Ohm's Law, the impedance is calculated:

$$Z(t) = \frac{u(t)}{i(t)} = \frac{U_0 \sin(\omega t + \phi)}{I_0 \sin(\omega t)} = Z_0 \frac{\sin(\omega t + \phi)}{\sin(\omega t)} \tag{3.4}$$

With Eulers relationship, the impedance is represented in the polar form of its complex number. With this relationship, the excitation current is given by:

$$\mathbf{I} = I_0 \exp(j\omega t) \tag{3.5}$$

and the response voltage:

$$\mathbf{U} = U_0 \exp(j(\omega t + \phi)) \tag{3.6}$$

Accordingly, the impedance is represented in the complex plane as:

$$\mathbf{Z} = \frac{\mathbf{U}}{\mathbf{I}} = Z_0 \exp(j\phi) \tag{3.7}$$

The SOC of the battery is later estimated by measuring the current battery impedance spectra and correlating it to known impedances at different SOC levels.

### 3.1.2 Indirect methods

Indirect SOC measurement methods, or book-keeping methods, are based on coulometric systems, measuring and integrating the battery charging/discharging current. When applying these methods, additional variables are measured, such as voltage and temperature, resulting in a more precise system in contrast to the previously described direct methods.

#### 3.1.2.1 Coulomb counting method

The Coulomb counting method is based on the integration of the battery charging/discharging current according to:

$$SOC(t) = SOC(0) + \int_0^t \frac{\eta \cdot i(t)}{Q_n} dt \tag{3.8}$$

where $SOC(0)$ is the initial SOC, $\eta$ being the coulombic efficiency, $Q_n$ the battery maximum capacity and $i(t)$ the discharge current. Thus, the accuracy of the coulomb counting method resorts primarily to a precise measurement of the battery current and accurate estimation of the initial SOC [16]. The inaccuracy of these parameters brings disadvantages, specific to a book-keeping system, due to the accumulation of errors over time, seeing that the inaccuracy of the SOC value estimation at a given moment will result in the incorrect initial SOC value for a future measurement. Therefore, these methods often require re-calibration. With this in mind, the coulomb counting method is usually combined with other battery parameters, such as its open circuit terminal voltage, directly related to the SOC value, as described in section 3.1.1.1, thereby compensating the inaccuracy of the method. Furthermore, this technique is unable to accurately match the non-linear behaviour of the battery over its entire lifetime, not taking into account the ageing of the cell, corresponding to a decrease in the battery's maximum capacity, $Q_n$.

### 3.1.3 Adaptive systems

The uncertainty of the battery and its management system behaviour, due to the influence of previously mentioned parameters, is the main problem to an accurate SOC estimation. For this reason, adaptive systems based on Fuzzy Logic [17], Artificial Neural Network (ANN) [18] and Kalman Filter (KF) [19] combined with direct measurements, indirect measurements or both, offer a better solution for on-line SOC estimation. These systems self-design themselves, conceding an automatic adjust to a change in the system.

#### 3.1.3.1 Fuzzy Logic based method

Fuzzy-Logic (FL) is a learning-based adaptive method capable of inferring information about the dynamic behaviour of the system while modelling it through a set of rules that make up a "linguistic" model. This type of method allows to generalize, add or even change the information composing the model when necessary. In a fuzzy system, data may be categorized by 'crisp' and/or 'fuzzy' sets. Crisp sets

categorize data with certainty, for instance, a set of voltages between 60kV and 400kV. With fuzzy sets, a set in which data can be categorized, is uncertain, for example, the voltage is 'high'. This linguistic descriptor 'high' is a subset contained in the set of voltages ('low', 'medium' and 'high') and is defined by its membership function. The degree to which an element of the set 'voltage' belongs to the fuzzy subset 'high' is indicated by a quantity referred to as its 'degree of membership' or fit fuzzy unit value [20]. Hence, the membership function is the basic idea in fuzzy set theory. Its value measures degrees to which objects satisfy certain properties.

The fuzzy system has four conceptual components: a rule base describing the relationship between input and output variables; a data base that defines the membership functions for the input and output variables; a reasoning mechanism that performs the inference procedure and a defuzzification block which transforms the fuzzy output sets to a real-valued crisp [10].

Applying Fuzzy theory to SOC estimation, impedance spectra values from Electrochemical Impedance Spectroscopy (EIS) [21] or Coulomb counting methods [22] give the input parameters for the fuzzy logic model construction and then, through the membership functions and rule set, a value for the SOC of the cell is obtained as output.

#### 3.1.3.2 Artificial Neural Network based method

The Artificial Neural Network (ANN) is a data based system with a working principle based on the mechanism of communication between the neurons present in the human brain. In ANN, data is received in different parts of our body. Proceeding this, each bit of data is crossed with other input data to see if there is any relation between them. If effectively there is a relation, a certain response is given by the system. This method estimates the actual SOC using the recent history of current, voltage, and temperature of the battery.

An architecture of a SOC estimating neural network is shown in Figure 3.4, taken from [23]. The ANN contains an input layer with three neurons for terminal voltage, discharge current, and temperature; an output layer with one neuron for SOC , and one hidden layer with $g$ neurons. In the input layer, data is introduced as it is in the network, without any kind of calculation. The hidden layer is where the input variables are weighted in different combinations, with each node getting a certain output ($w_{io}^{k}$ in Figure 3.4, where *i* is the starting node, *o* is the end node and *k* is index of the layer) . In the output layer, the previous hidden layer outputs are gathered and evaluated in order to bring a solution to the problem.

A learning process is required so that the knowledge of the Neural Network is achieved. This consists in a process where weights connection between nodes are regulated by a specific method to obtain desired values. This is accomplished using a back propagation learning algorithm in order to guarantee the error between the desired output (weight target) and the output of the network according to an "error goal". The solution of the learning program is attained when the combination of weights which minimizes the "error goal", is found. After the neural network is trained, it is ready to be validated and employed in SOC estimation [22].

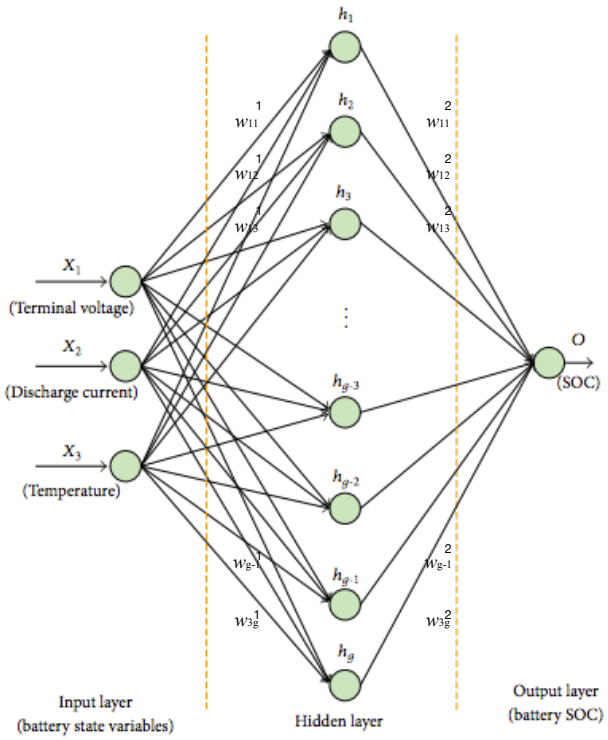



Figure 3.4: The architecture of the SOC estimating neural network [23].

#### 3.1.3.3 Kalman Filter based method

The Kalman filter (KF) is an algorithm capable of estimating the current value of the time-varying state of a dynamic system through filtered measurements observed over time. The KF is a state estimator for a linear system with the assumptions that the process noise and sensor noise are independent, zero-mean, Gaussian noise processes. If the system is non-linear, a linearisation process is used at each time step to approximate the non-linear system to a linear time varying one. This linearisation process associated with the Kalman filter algorithm results in the extended Kalman filter (EKF) [24].

Figure 3.5 shows a block diagram of the Kalman Filter algorithm.

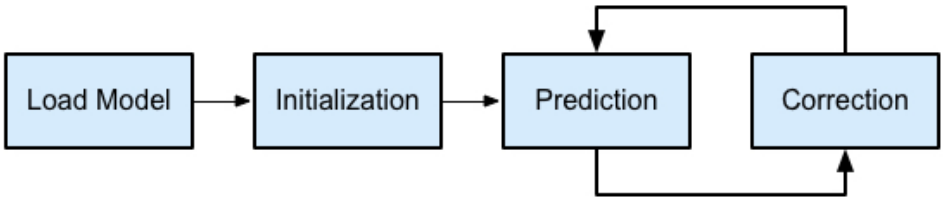



Figure 3.5: Block diagram of the Kalman Filter algorithm.

The algorithm is divided in four steps. The first step is expressing the model in a state-space representation (Load Model); after this, the filter is initialized (Initialization). The third step, the prediction

one, is where the KF estimates the present state variables and their uncertainties (Prediction). Finally, when the following measurement is observed, the new estimates are corrected and updated trough a weighted average, giving more weight to estimated variables with higher certainty (Correction).

In addition, to correctly estimate the SOC value using the EKF, the linearisation of the battery is required. Thus, some models, such as the Shepherd Model; Unnewehr Universal Model; Nernst Model; Linear Model and RC Model are presented in [25].

## 3.2 Proposed Method

In this project, a solution based on an impedance spectra database combined with fuzzy logic is developed in order to correctly estimate the battery SOC. In a first step, for pre-defined values of battery SOCs, measured through a coulometric approach, described in section 3.1.2.1, an EIS measurement is performed to the battery cell and this data is stored in a impedance spectra database. Later, the calculation of SOC is performed through the comparison of the current battery impedance characteristic with the impedance characteristic curves previously stored in the database. This inference between the performed EIS and the stored database of impedances is accomplished using fuzzy logic, explained in the next chapter. On this account, the developed system will be capable of automatically estimate the battery SOC, through the combined implementation of two processes:

- The EIS technique, explained in 3.1.1.3.
- A fuzzy inference system, based on the previously acquired impedance spectras database and the performed EIS.

The construction of the database of impedance spectras with their respective capacity begins with the battery fully charged. Afterwards, the battery is discharged and through a coulomb count technique described in 3.1.2.1, an EIS measurement is executed for specific SOC values (100%; 90%; 80%; 70%; 60%; 50%; 40%; 30%; 20%; 15%) resulting in an initial database of impedance spectras over the entire range of SOC's.

Seeing that the battery impedance is dependant of its age and number of cycles, this database needs to be updated periodically, in order to correctly estimate the battery cell SOC. In this project, this process will not be performed, leaving the update of the database with the increase number of charge/discharge cycles for future work.

# Chapter 4

# Fuzzy Logic and Adaptive Neuro Fuzzy Inference Systems

In section 3.1.3.1, Fuzzy logic was introduced as an adaptive system that finds information on dynamic behaviour of a system expressing data through a set of rules that make up a linguistic model. In this chapter, the characteristics of a basic fuzzy model are presented and described, as an introduction to the adaptive neuro fuzzy inference system(ANFIS) method, later applying this inference mechanism to the project so that an accurate estimation of the battery SOC is achieved.

## 4.1 Characteristics of a fuzzy model

The structure of a fuzzy inference revolves around a model that maps input data to input membership functions, input membership function to fuzzy rules, fuzzy rules to a set of output characteristics, output characteristics to output membership functions and finally output membership functions to a single output value. As an example, a simple functional relation is presented, taken from [26], in order to help the reader understand the working principles of the model. Consider the function $y = x^2$ , relating the input (variable $x$) with the output (variable $y$), graphically represented in Figure 4.1.

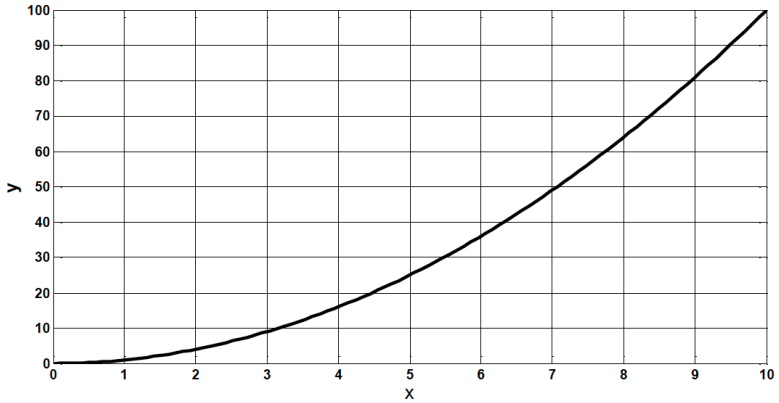



Figure 4.1: Plot of the given function $y = x^2$ [26].

The function can be discretized for the values $x$ = 1, 3, 5, 7 and 9, as shown in Figure 4.2, imposing a set of relations, referred as crisp relations, since data is represented trough crisp values, expressed as follows:

$$\begin{aligned} &\text{If } x \in [0,2] \text{ Then } y = 1^2 \\ &\text{If } x \in ]2,4] \text{ Then } y = 3^2 \\ &\text{If } x \in ]4,6] \text{ Then } y = 5^2 \\ &\text{If } x \in ]6,8] \text{ Then } y = 7^2 \\ &\text{If } x \in ]8,10] \text{ Then } y = 9^2 \end{aligned} \tag{4.1}$$

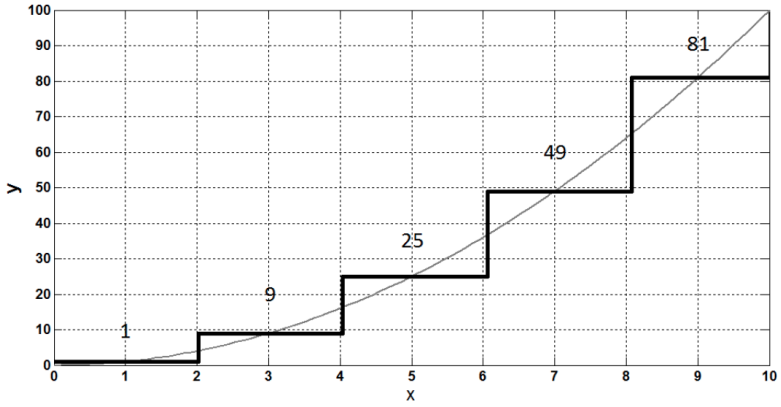



Figure 4.2: Plot of the discretized function $y = x^2$ [26].

### 4.1.1 Fuzzy sets and Membership functions

After the proposed discretization, the relation between the input and the output, $x$ and $y$, respectively, can't be defined in a precise mathematical way, as before ($y = x^2$), but can treated through a set of linguistic rules such as:

- Rule 1: If $x$ is low, then $y$ is low.
- Rule 2: If $x$ is moderate, then $y$ is high.
- Rule 3: If $x$ is high, then $y$ is very high.

Now, a set of linguistic values is used to represent the output as a function of the input. A set for the input variable $x$ is composed of three subsets: low, moderate, high; whereas the set for the output variable $y$ is characterized by the subsets low, high and very high. The degree to which an input $x$ belongs to a specific subset is indicated by its 'degree of membership' to a membership function. A membership function can be described as a mapping curve that 'translates' how each point in the input space is mapped to a membership value (or degree of membership) between 0 and 1. Applying this idea

the given example, using triangular membership functions, one can say that a value of 1 for the subset low of the input variable $x$ would correspond to a crisp value of 0 and a value of 0.5 for the same subset would correspond to a crisp value of 1. The linguistic rules describing the system are represented in Figure 4.3.

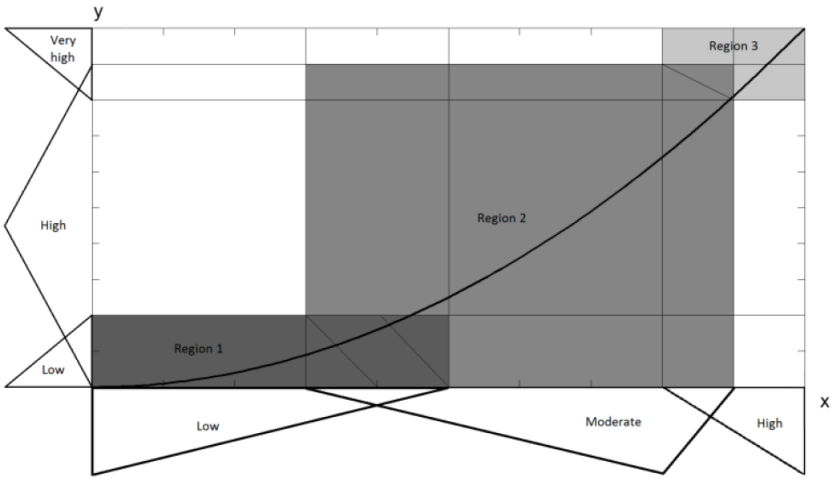



Figure 4.3: Set of rules and membership functions describing the fuzzy system applied to the given example [26].

Hence, it can be said that each linguistic term or subset of rules can be represented by its own membership function ($\mu_f(x)$), in this case, a triangular membership function:

- Rule 1: If $x$ is $\underbrace{low}_{\mu_{A_1}^{(1)}(x)}$ , then $y$ is $\underbrace{low}_{\mu_B^{(1)}(y)}$ .
- Rule 2: If $x$ is $\underbrace{moderate}_{\mu_{A_2}^{(2)}(x)}$, then $y$ is $\underbrace{high}_{\mu_B^{(2)}(y)}$ .
- Rule 3: If $x$ is $\underbrace{high}_{\mu_{A_3}^{(3)}(x)}$ , then $y$ is $\underbrace{very\ high}_{\mu_B^{(3)}(y)}$.

Each membership function is defined as (for a triangular membership function):

$$\mu_f(x) = \begin{cases} 0, & x \leq a \\ \frac{x-a}{b-a}, & a < x \leq b \\ \frac{c-x}{c-b}, & b < x \leq c \\ 0, & x > c \end{cases}$$

where the parameters $a$, $b$, $c$ (with $a < b < c$) determine the $x$ coordinates of the three corners of the underlying triangular membership functions.

An example for the fuzzy output of the linguistic fuzzy logic system presented is shown in Figure 4.4.

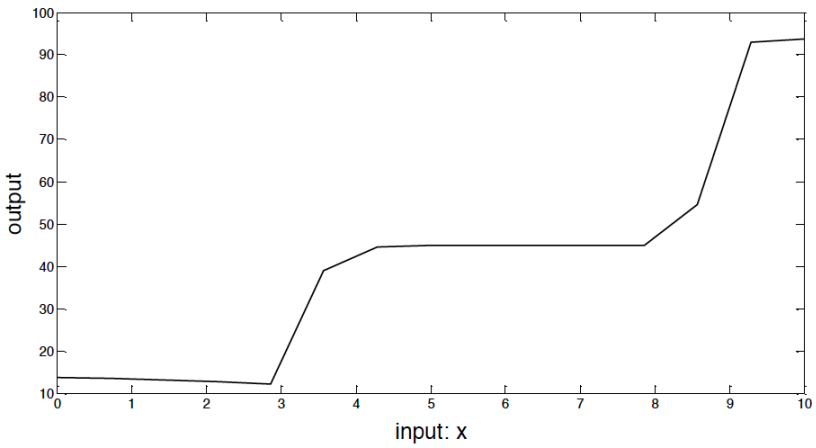



Figure 4.4: Ouput of the linguistic fuzzy logic system of the given example [26].

### 4.1.2 Fuzzy inference system

In this project it is discussed the so-called Sugeno, or Takagi-Sugeno-Kang, method of fuzzy inference, mapped over a neural network structure. This methodology uses a linear or constant level as the output membership function rather than a distributed fuzzy set. This is known as a singleton output membership function, $\omega$. A typical rule for a system with two inputs in a Sugeno fuzzy model has following form:

$$\text{If Input 1 = } x \text{ and Input 2 = } y\text{, then Output is } \omega = g(x, y)$$

When $g(x, y)$ is a first-order polynomial, the fuzzy inference method is a first-order Sugeno fuzzy model:

$$\omega = mx + ny + k \tag{4.2}$$

where the parameters $m$, $n$ and $k$ are the parameters describing the polynomial linear relation between the inputs and the single value crisp output.

When $g(x, y)$ is constant, the Sugeno fuzzy model is given by a zero-order polynomial ($m = n = 0$):

$$\omega = k \tag{4.3}$$

Changing the output subsets of the rules for the given example to singletons, the rules for the fuzzy model of the functional relation ($y = x^2$) are now represented as follows and observed in Figure 4.5:

- Rule 1: If $x$ is low, then $y$ is $\omega^{(1)}$.
- Rule 2: If $x$ is moderate, then $y$ is $\omega^{(2)}$.
- Rule 3: If $x$ is high, then $y$ is $\omega^{(3)}$.

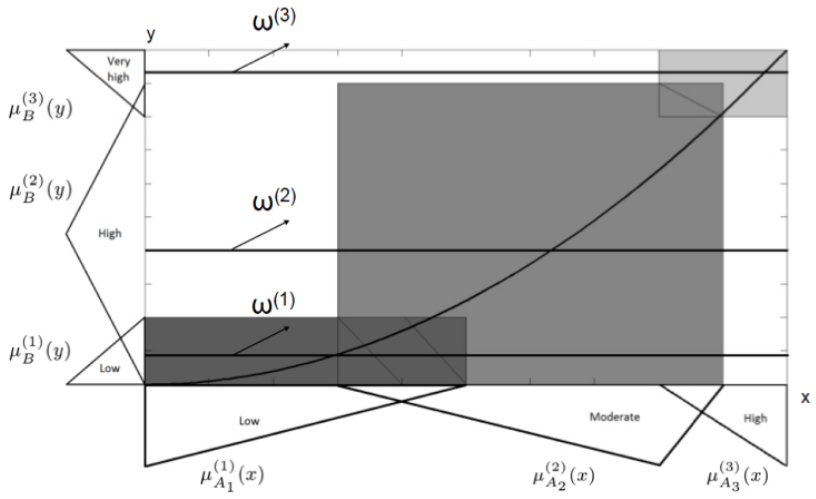



Figure 4.5: Representation of the fuzzy model rules using triangular membership functions and respective singletons [26].

### 4.1.3 Defuzzification

Since each rule has a crisp output, the overall output is obtained via weighted average of all rule outputs, calculated as:

$$Y(x) = \frac{\sum_{l=1}^{c} \mu_{A_l}^{(l)}(x)\omega^{(l)}}{\sum_{l=1}^{c} \mu_{A_l}^{(l)}(x)} \tag{4.4}$$

In the previous expression, the variable $x$ is the single crisp input; $c$ represents the total number of rules used in the inference, $l$ is the number of the rule and $Y(x)$ is the numerical value inferred through the model.

#### 4.1.3.1 Defuzzification for a system with two inputs

In the previous example, only one input was considered. If the system has two inputs, the fuzzy reasoning methodology changes. In this case, the singleton output of each rule, $\omega^{(i)}$, is weighted by the firing strength of the rule, $f^{(l)}(X1, X2)$ for both inputs, $X1$ and $X2$.

The firing strength gives the compatibility degree of the pattern with each rule. In order to calculate the compatibility degree of the pattern with each rule, a T-norm operator is used, therefore, the degrees of membership of the linguistics terms of the rule $l$ ($l$ = 1,...,Total number of rules) for each input are multiplied as a function of the inputs values. For example, if Input $X1 = a$ and Input $X2 = b$, then the firing strength for the rule $l$ is calculated as:

$$f^{(l)}(a, b) = \mu_{X1}^{(l)}(a) \cdot \mu_{X2}^{(l)}(b) \tag{4.5}$$

where $\mu_{X1}^{(l)}(a)$ and $\mu_{X2}^{(l)}(b)$ are the values of degrees of membership for the rule $l$ relative to Inputs 1 and

2, considering the array of membership degree for each membership function according to:

$$\mu_{X1}(k) = [\mu_{X1}^{(1)}(k) \quad \mu_{X1}^{(2)}(k) \quad \mu_{X1}^{(3)}(k) \quad \cdots \quad \mu_{X1}^{(l)}(k)] \tag{4.6}$$

$$\mu_{X2}(k) = [\mu_{X2}^{(1)}(k) \quad \mu_{X2}^{(2)}(k) \quad \mu_{X2}^{(3)}(k) \quad \cdots \quad \mu_{X2}^{(l)}(k)] \tag{4.7}$$

The next process is calculating the ratio of the $l$th rule firing strength, $f^{(l)}(X1, X2)$, to the sum of all rules firing strengths:

$$\overline{f^{(l)}(a,b)} = \frac{f^{(l)}(a,b)}{\sum_{i=1}^{c} f^{(i)}(a,b)} \tag{4.8}$$

where $c$ represents the total number of rules used in the inference; $l$ is the number of the rule.

After the normalization of each firing rule, this value is multiplied by the first-order polynomial that describes the linear relation between the inputs and the single value output:

$$\overline{f^{(l)}(a,b)} \cdot \omega^{(l)} = \overline{f^{(l)}(a,b)} \cdot (m_l X1 + n_l X2 + k_l) \tag{4.9}$$

where the parameters $m_l$, $n_l$ and $k_l$ are the modifiable parameters describing the output singleton to each rule $l$.

The overall output $Y$is finally given by the sum of all the multiplied polynomial by their firing strengths, representing the centre of gravity or the weighted average of all rule outputs:

$$Y = \sum_{i=1}^{c} (\overline{f^{(i)}(a,b)} \cdot \omega^{(i)}) = \frac{\sum_{i=1}^{c} (f^{(l)}(a,b) \cdot \omega^{(i)})}{\sum_{i=1}^{c} f^{(i)}(a,b)} \tag{4.10}$$

This process is exemplified through a basic example using two input variables, each one mapped into five membership functions, represented in Figure 4.7. The combination of membership functions for each variable results in different rules of the system:

Rule 1: If $X1$ is $\mu_{X1}^{(1)}$ and $X2$ is $\mu_{X2}^{(1)}$ , then $\omega^{(1)} = m_1 X1 + n_1 X2 + k_1$
Rule 2: If $X1$ is $\mu_{X1}^{(2)}$ and $X2$ is $\mu_{X2}^{(2)}$ , then $\omega^{(2)} = m_2 X1 + n_2 X2 + k_2$
Rule 3: If $X1$ is $\mu_{X1}^{(3)}$ and $X2$ is $\mu_{X2}^{(3)}$ , then $\omega^{(3)} = m_3 X1 + n_3 X2 + k_1$
Rule 4: If $X1$ is $\mu_{X1}^{(4)}$ and $X2$ is $\mu_{X2}^{(4)}$ , then $\omega^{(4)} = m_4 X1 + n_4 X2 + k_4$
Rule 5: If $X1$ is $\mu_{X1}^{(5)}$ and $X2$ is $\mu_{X2}^{(5)}$ , then $\omega^{(5)} = m_5 X1 + n_5 X2 + k_5$

Figure 4.6 illustrates the reasoning mechanism for the Sugeno model applied to the given example. In layer 1, every node is an adaptive node, for which the parameters can be changed, with a node function equal to the membership function associated to each subset of each of the five rules. In layer 2, each node is fixed, having no parameters, and represents the firing strength associated to each rule. In layer 3 each node is fixed and the incoming firing strength is normalized. In layer 4 each node is adaptive and the firing rules are multiplied by their correspondent singletons. Layer 5 is composed by a single node, computing the output as the sum of all incoming signals.

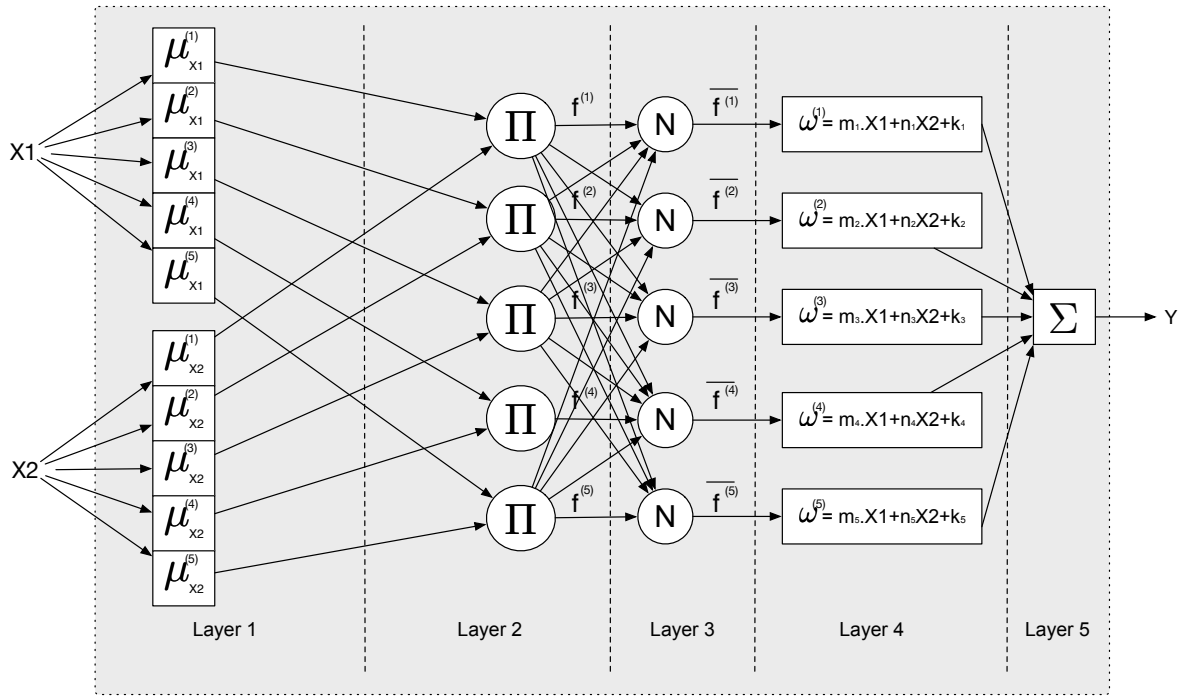



Figure 4.6: Structure of the five-layer adaptive neuro-fuzzy system for the Sugeno model for the given example.

The fuzzy singleton or ”centre of gravity” of each rule is obtained using qualitative observations as displayed in Figure 4.8. This is achieved for the rule in Figure 4.7 using the set of elements which are in the intersection of the domain of the two membership functions as shown in Figure 4.8, represented by black dots.

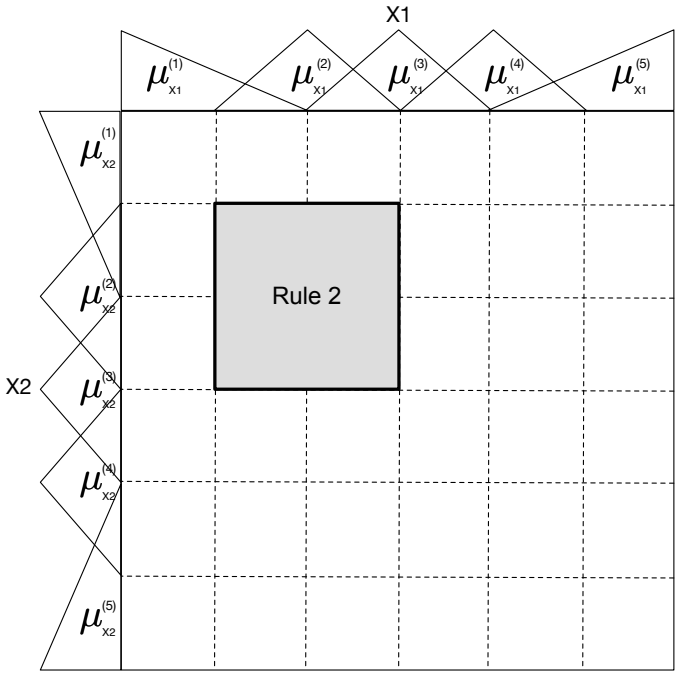



Figure 4.7: Graphical representation of rule 2.

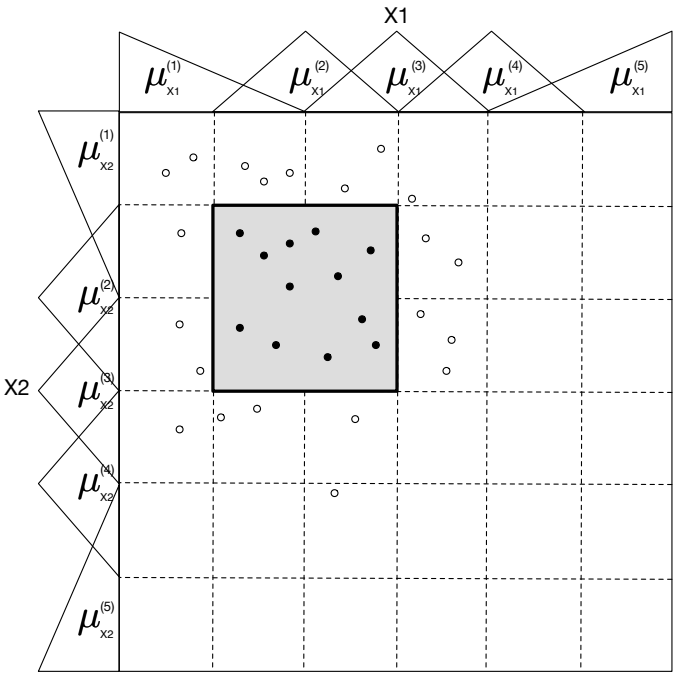



Figure 4.8: Set of examples relating to the rule defined by the membership function 2 [X1] and membership function 2 [X2].

## 4.2 Fuzzy logic applied to a system with two inputs using learning examples

Sometimes, it is not the best practice to establish the IF-THEN rules of a fuzzy system using a human operator. Frequently, one cannot discern what the membership functions should look like simply from observing the data. In other cases, the option of inferring the fuzzy output through a comparative analysis between the current inputs and previous ones, representing the behaviour of the system, is preferred. In these cases, the output of a given system is accomplished using a technique that provides a method for the fuzzy modelling procedure to learn information about a previously acquired data set, rather than choosing randomly the membership function parameters. Hence, for systems to which already exists a collection of input/output data, neuro-adaptive techniques incorporated with fuzzy logic are used in order to compute the membership function parameters that best allow the associated fuzzy inference system to track the current input/output data. This is the idea behind ANFIS or adaptive neuro-fuzzy inference systems, so that a membership function parameter adjustment is attained [27].

The parameter identification in the adaptive nodes in adaptive neuro-fuzzy inference systems is achieved using a backpropagation learning algorithm. This algorithm searches for the minimum of error function in weight space through a method of gradient descent. The solution of the learning program is achieved when the combination of weights which minimizes the error function is found [28]. This error is defined by the sum of the squared difference between actual and desired outputs. While this difference

is propagated back through the five layers such as in Figure 4.6, the parameters $m$, $n$ and $k$ (from the singleton's) and the parameters describing each input membership function associated to each rule, are adjusted.

In this project, this learning technique associated to the neuro-fuzzy inference system is applied to the input/output data, resulting from the EIS implemented system presented in the next chapter, through the Fuzzy Logic Toolbox function existent in MATLAB. This function works by introducing as an argument an input/output data set so that the toolbox function named anfis constructs a fuzzy inference system (FIS) output file in which the membership function and singleton parameters associated with each rule are adjusted automatically. This way, a model describing the impedance spectra database is created, containing the mentioned parameters, so that an IF-THEN rule based fuzzy inference system is later implemented.

# Chapter 5

# Implementation of the EIS measurement and SOC estimation systems

In this chapter the implementation of the proposed EIS measurement system is described. In addition, the adopted solution applied to the $LiFePO_4$ battery cell SOC estimation, describing the use of ANFIS methodology previously introduced in chapter 4, is delineated.

The proposed system combines signal generation, acquisition, processing and SOC estimation. It is composed by three main blocks, displayed in Figure 5.1. In Figure 5.2, these blocks are represented in the developed device:

- An Arduino Due, providing a variable frequency voltage source (DDS and DAC in Figure 5.1).
- A customized PCB (Printed Circuit Board):
  - First filtering the input signal from the voltage source Arduino (LP and HP filter in Figure 5.1).
  - Afterwards, amplifying the signal using a linear voltage-controlled current source (VCCS), producing a sinusoidal excitation current applied to the cell (Enhanced Howland current source in Figure 5.1).
  - Finally, acquiring both voltage and current signals, using a hall sensor and two external analog-to-digital converters (Hall sensor and ADCs in Figure 5.1).
- Another Arduino Due microcontroller, responsible for the signals processing and SOC estimation:
  - Firstly, imposing the sampling frequency to the external ADCs located in the PCB.
  - Simultaneously, storing the acquired samples resulting from the ADC conversion, while applying oversampling and moving average filtering techniques (Oversampling and Averaging; Moving Average Filter in Figure 5.1).

– Proceeding this, applying the Discrete Fourier transform to both voltage and current in order to obtain the impedance spectra of the cell (DFT blocks in Figure 5.1).

– Finally, inferring the SOC value, employing the ANFIS methodology, introduced in section 4.2 (ANFIS block in Figure 5.1).

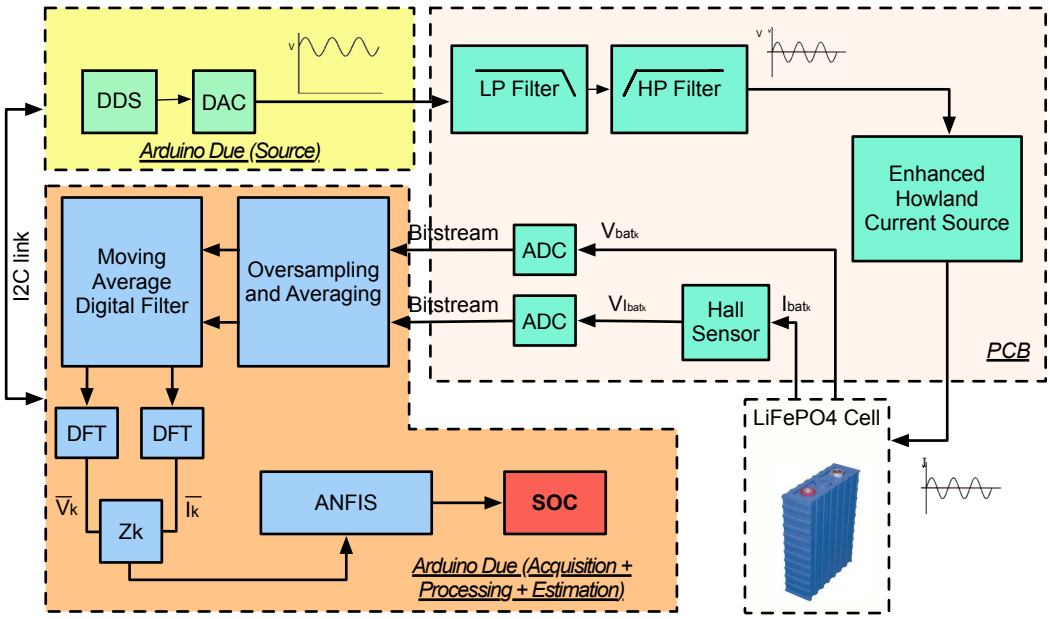



Figure 5.1: Block diagram of the proposed EIS measurement and SOC estimation systems.

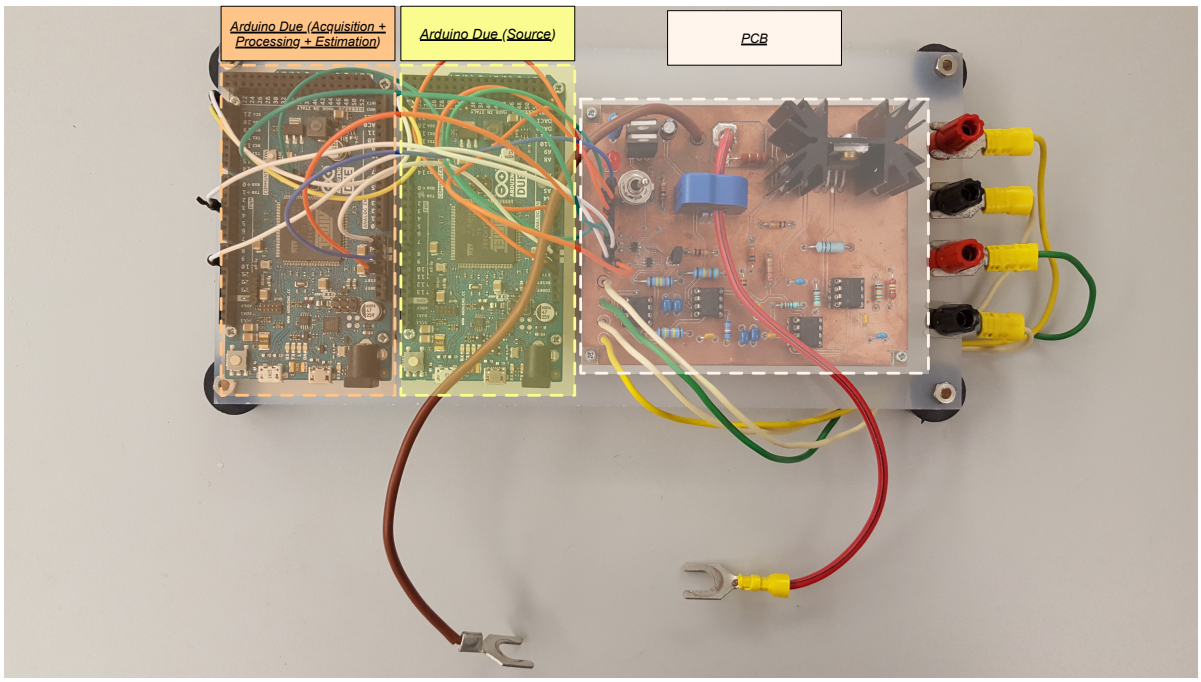



Figure 5.2: Developed device composed by three main bocks: Arduino Due (source), PCB and Arduino Due (responsible for the signal acquisition, processing and SOC estimation).

## 5.1 Arduino Due

Both signal generation and signal acquisition were executed using a commercial Arduino Due platform. The Arduino Due is a microcontroller board embedding a 32-bit ARM core microcontroller (Atmel SAM3X8E), clocked at 84 MHz. It embeds a dual channel 12-bit digital to analog converter (DAC) output, 16 12-bit analog to digital converter (ADC) inputs, 54 digital pins that can be used as an input or output. Each pin is able to provide a current of 3 mA or 15 mA, depending on the pin, or receive a current of 6 mA or 9 mA, depending on the pin. The Due has 512 KB of flash memory, where the Arduino sketch is stored, and 96 KB of SRAM, where the sketch creates and manipulates variables while it runs.

In this project, two Arduino Due, displayed in Figure 5.3, were employed and a firmware has been developed for each, one for the variable frequency voltage source and another one for the cell impedance measurement system in addition to the SOC inference system based on the measured impedance data.

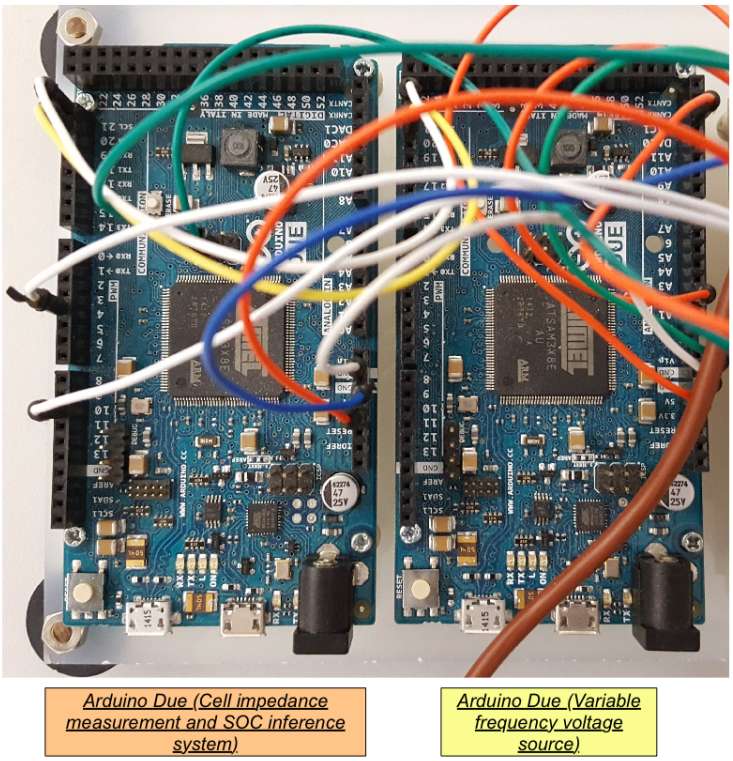



Figure 5.3: Arduino Dues used in the developed device.

## 5.2 Variable frequency voltage source

In order to polarize the cell and acquire its impedance over a wide range of frequencies, a variable frequency voltage source is necessary.

An Arduino Due microcontroller board was used to implement the Digital Direct Synthesis (DDS) technique. This converts digital numbers stored in an array into analogue signals through conversions

executed by a Digital-to-Analogue Converter (DAC). The DDS technique processes data blocks read from a look-up table in a Static Random-Access Memory (SRAM) to generate a form of frequency-tunable and phase-tunable output signal with reference to a fixed frequency precision clock source [29]. The address counter steps through and accesses each of the SRAM's memory locations and the contents (the equivalent sine amplitude words) are presented to a DAC converter. The output frequency of this DDS implemented technique is dependent on the frequency of the reference clock in addition to the sine wave step size, previously programmed into the SRAM Arduino sketch.

With the introduction of a phase accumulator function into the digital signal chain, illustrated by the "phase wheel" in Figure 5.4, this architecture becomes a numerically-controlled oscillator, now being able to alter the frequency of the output sinwave. A counter and phase register are implemented in the microcontroller before the sine lookup table.

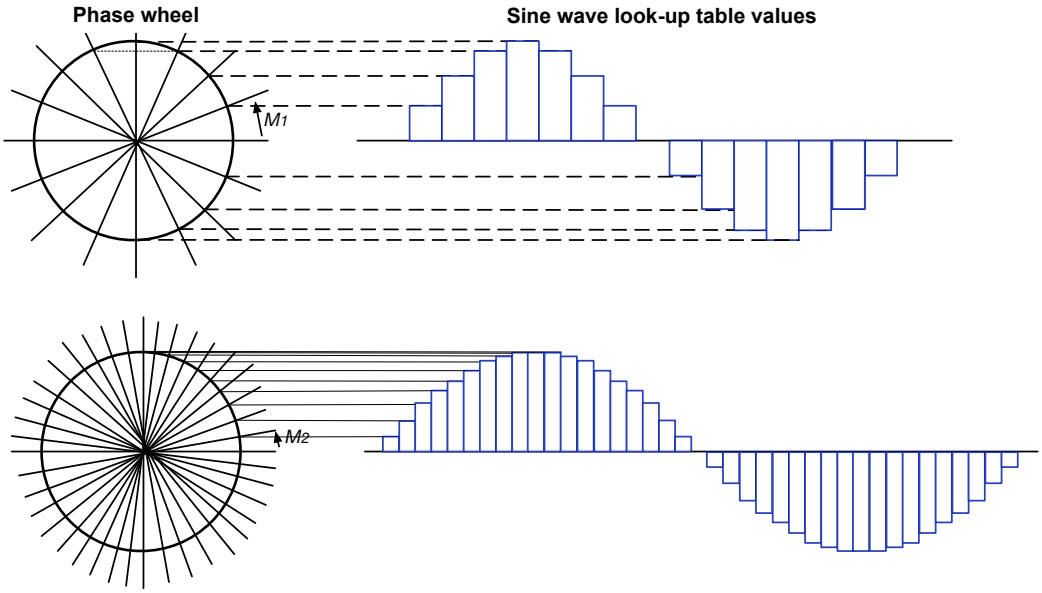



Figure 5.4: Digital Phase Wheel for two increment ammounts, $M_1$ and $M_2$.

One revolution of the vector around the phase wheel ($2\pi$ rad) is divided into 2000 data points, representing a period of the sine wave stored in the look-up table [30]. Accordingly, an interruption sub-routine is programmed in the microcontroller, summed at a specific rate, the frequency reference. Each time the sub-routine is summed, an "increment amount" is added to a *Phase accumulator* variable. When the *Phase accumulator* overflows, a complete cycle of the sinewave is covered.

The magnitude of the "increment ammount", represented by the variable *M* in Figure 5.4, is determined by a digital word contained in the *nPhaseIncrement* array. Each position in the *nPhaseIncrement* array contains the phase jump value equivalent in the phase wheel to a change in the frequency in the variable voltage frequency source. Thus, this "increment ammount", *M* in Figure 5.4, effectively sets how many points to skip around the phase wheel. The larger the jump size, the faster the phase accumulator overflows and completes its equivalent of a sinewave cycle. This is how a change in frequency is accomplished, changing the "increment ammount" added to the accumulator, thus changing the speed

at which the Phase accumulator overflows. In sum, the specific range of frequencies set in the voltage source is defined through the *nPhaseIncrement* pre-stored array.

## 5.3 Band-pass Filter

An active band-pass filter is required to exclusively select frequencies inside the 0.01Hz-10kHz spectrum, as this range fully describes the battery cell behaviour. A lower cut-off frequency of 0.01Hz is essential, this way filtering the DC offset included in the signal generated by the Arduino Due DAC.

There are some filter specifications: it requires a Butterworth response due to its nearly flat pass band with unity gain and no ripple, this way obtaining a uniform frequency response for all the wanted frequencies. The architecture that will be used is the Sallen-Key owing to its ability to operate under unity amplifier gain. The Sallen-Key topology has a low-pass or high-pass roll off 20dB/dec for every pole. Thus, an eight order Butterworth Band-pass filter will have an attenuation rate of -80dB/dec and 80 dB/dec. Such solution is recommended for this application, forming an eight-order Butterworth Band-pass filter after cascading two stages of second-order low-pass filters with two stages of second-order high-pass filters [31], illustrated in Figure 5.5.

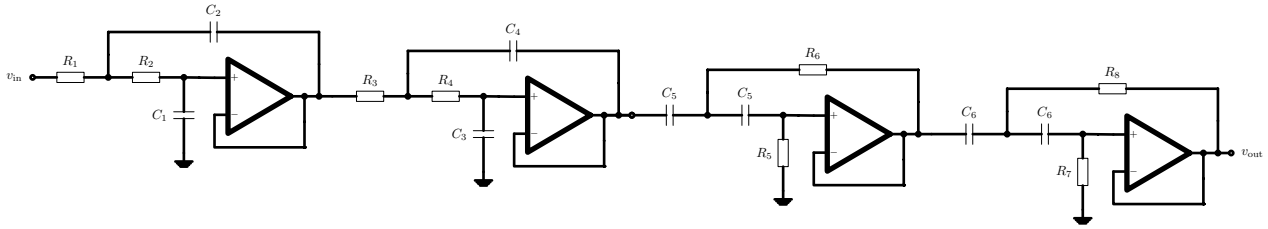



Figure 5.5: 8th Order Unity-Gain Sallen-Key Band-Pass Filter.

Table 5.1 lists the specifications for the desired Band-pass filter. Setting the following parameters, the required filter characteristic is later obtained using PSpice A/D simulator from OrCAD Capture CIS CIS 16.6 (2012 version) software.

| | |
|---|---|
| Lower Cut-Off Frequency | 10mHz |
| Higher Cut-Off Frequency | 10kHz |
| Centre Frequency | 10Hz |
| Band-pass Gain | 1 |

Table 5.1: Filter Specifications.

### 5.3.1 Low-Pass Filter

The general transfer function of a low-pass filter is [32]:

$$A(s) = \frac{A_0}{\prod_i (1 + a_i s + b_i s^2)} \tag{5.1}$$

with $A_0$ being the passband gain, $a_i$ and $b_i$ being the filter coefficients.

The equation represents a cascade of low-pass second order filters. Hence, for a single stage second order filter:

$$A(s) = \frac{A_0}{1 + a_i s + b_i s^2} \tag{5.2}$$

The filter coefficients $a_i$ and $b_i$ distinguish Butterworth, Tschebyscheff, and Bessel filters, therefore determining the gain behavior in the passband. The unity-gain for the proposed topology is analysed in the following sections.

#### 5.3.1.1 2nd order Unity-Gain Sallen-Key Low-Pass Filter

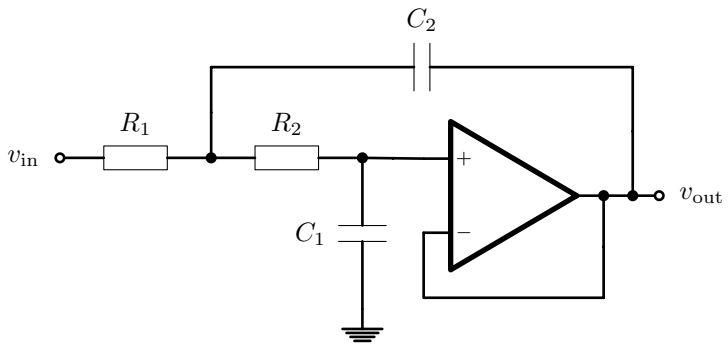



Figure 5.6: Unity-Gain Sallen-Key Low-Pass Filter.

The transfer function of the low-pass unity-gain Sallen-key filter, displayed in Figure 5.6 is:

$$A(s) = \frac{1}{1 + [\omega_c C_1 (R_1 + R_2)]s + (\omega_c^2 R_1 R_2 C_1 C_2)s^2} \tag{5.3}$$

Comparing this transfer function to equation (5.2) outcomes:

$$\begin{aligned} A_0 &= 1\,, \\ a_1 &= \omega_c C_1 (R_1 + R_2)\,, \\ b_1 &= \omega_c^2 R_1 R_2 C_1 C_2\,, \end{aligned} \tag{5.4}$$

where $\omega_c$ is the angular frequency associated to the higher cut-off frequency.

For a given $C_1$ and $C_2$, the resistor values for $R_1$ and $R_2$ are determined by:

$$R_{1,2} = \frac{a_1 C_2 \mp \sqrt{a_1^2 C_2^2 - 4 b_1 C_1 C_2}}{4\pi f_c C_1 C_2} \tag{5.5}$$

Following equation (5.5), $C_2$ must satisfy the following condition, so that real values for $R_1$ and $R_2$

are obtained:

$$C_2 \geq C_1 \frac{4b_1}{a_1^2} \tag{5.6}$$

#### 5.3.1.2 4th Order Unity-Gain Sallen-Key Low-Pass Filter

In order to obtain a fourth-order low-pass filter, two second-order filters are connected in series, as illustrated in Figure 5.8, so that the product of the individual frequency responses results in the optimized frequency response of the overall filter.

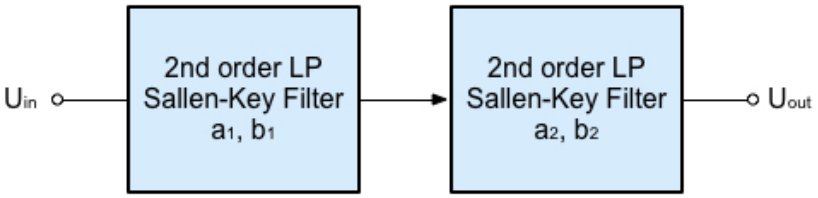



Figure 5.7: Cascading Filter Stages for a fourth-order Low-Pass filter.

For a fourth-order Butterworth filter type, the coefficients associated with each second order polynomial in equation (5.2) are [32]:

- $a_1 = 1.85$
- $b_1 = 1$
- $a_2 = 0.77$
- $b_2 = 1$

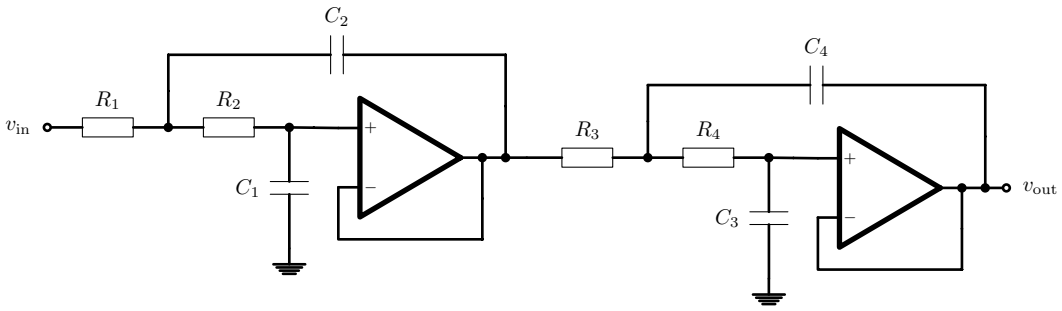



Figure 5.8: 4th Order Unity-Gain Sallen-Key Low-Pass Filter.

• **First stage** :

Specifying $C_1 = 100$ pF, so that acceptable values for $R_1$ and $R_2$ are obtained, and invoking equation (5.6), $C_2$ results in:

$$C_2 \geq C_1 \frac{4b_1}{a_1^2} = 100 \cdot 10^{-12} \cdot \frac{4 \cdot 1}{1.8478^2} = 117 \text{ pF} \rightarrow C_2 = 220 \text{ pF} \tag{5.7}$$

With $C_1$ =100 pF and $C_2$ = 220 pF , $R_1$ and $R_2$ are calculated for a high cut-off frequency, $f_c$, of 10 kHz, using equation (5.5):

$$R_1 = \frac{a_1 C_2 - \sqrt{a_1^2 C_2^2 - 4 b_1 C_1 C_2}}{4\pi f_c C_1 C_2} = 46.505 \text{ k}\Omega \rightarrow R_1 = 47.4 \text{ k}\Omega \tag{5.8}$$

$$R_2 = \frac{a_1 C_2 + \sqrt{a_1^2 C_2^2 - 4 b_1 C_1 C_2}}{4\pi f_c C_1 C_2} = 247.582 \text{ k}\Omega \rightarrow R_2 = 240 \text{ k}\Omega \tag{5.9}$$

• **Second stage** :

The process is repeated for this stage. For a value of $C_3 = 100$ pF, $C_4$ results in:

$$C_4 \geq C_3 \frac{4 b_2}{a_2^2} = 100 \cdot 10^{-12} \cdot \frac{4 \cdot 1}{0.7654^2} = 683 \text{ pF} \rightarrow C_4 = 820 \text{ pF} \tag{5.10}$$

With $C_3 = 100$ pF and $C_4 = 820$ pF, $R_1$ and $R_2$ are calculated as follows:

$$R_3 = \frac{a_2 C_4 - \sqrt{a_2^2 C_4^2 - 4 b_2 C_3 C_4}}{4\pi f_c C_3 C_4} = 36.992 \text{ k}\Omega \rightarrow R_3 = 35.7 \text{ k}\Omega \tag{5.11}$$

$$R_4 = \frac{a_2 C_4 + \sqrt{a_2^2 C_4^2 - 4 b_2 C_3 C_4}}{4\pi f_c C_3 C_4} = 85.824 \text{ k}\Omega \rightarrow R_4 = 86.6 \text{ k}\Omega \tag{5.12}$$

### 5.3.2 High-Pass Filter

The general transfer function of a high-pass filter is given by:

$$A(s) = \frac{A_\infty}{\prod_i (1 + \frac{a_i}{s} + \frac{b_i}{s^2})} \tag{5.13}$$

with $A_\infty$ being the passband gain.

The equation stands for a cascade of High-pass second order filters, being the transfer function of a single stage second order filter given by (5.14):

$$A(s) = \frac{A_\infty}{(1 + \frac{a_i}{s} + \frac{b_i}{s^2})} \tag{5.14}$$

Likewise, as with the low-pass filter, coefficients $a_i$ and $b_i$ distinguish Butterworth, Tschebyscheff, and Bessel filters.

#### 5.3.2.1 2nd Order Unity-Gain Sallen-Key High-Pass Filter

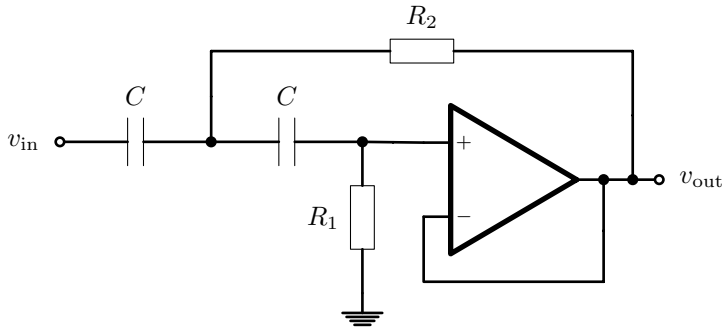



Figure 5.9: Unity-Gain Sallen-Key High-Pass Filter.

The transfer function of the second order unity-gain high-pass filter shown in Figure 5.9 is given by:

$$A(s) = \frac{1}{1 + \frac{2}{\omega_c R_1 C} \cdot \frac{1}{s} + \frac{1}{\omega_c^2 R_1 R_2 C^2} \cdot \frac{1}{s^2}} \tag{5.15}$$

Comparing the previous transfer function to equation (5.14) results:

$$\begin{aligned} A_\infty &= 1\,, \\ a_1 &= \frac{2}{\omega_c R_1 C}\,, \\ b_1 &= \frac{1}{\omega_c^2 R_1 R_2 C^2}\,, \end{aligned} \tag{5.16}$$

where $\omega_c$ is the angular frequency associated to the lower cut-off frequency.

For a certain value of $C$, the resistor values $R_1$ and $R_2$ are calculated over (5.17) and (5.18), respectively:

$$R_1 = \frac{1}{\pi f_c C a_1} \tag{5.17}$$

$$R_2 = \frac{a_1}{4\pi f_c C b_1} \tag{5.18}$$

The derivations and equations above were summarized from [32].

#### 5.3.2.2 4th Order Unity-Gain Sallen-Key High-Pass Filter

Two high-pass second-order filters are cascaded (Figure 5.10) similarly to the low-pass filter, in order to get a fourth-order filter. The cascade is presented in Figure 5.11.

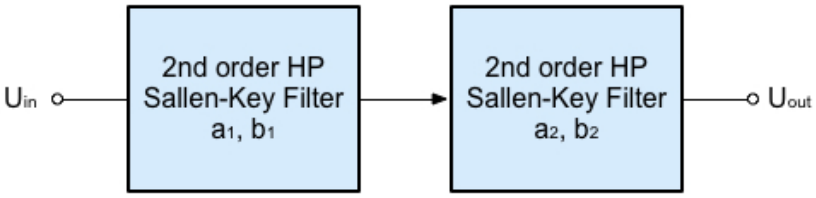



Figure 5.10: Cascading Filter Stages for a fourth-order High-Pass filter.

Again, for a fourth-order Butterworth filter type, the coefficients associated with each second order polynomial in equation (5.15) are [32]:

- $a_1 = 1.85$
- $b_1 = 1$
- $a_2 = 0.77$
- $b_2 = 1$

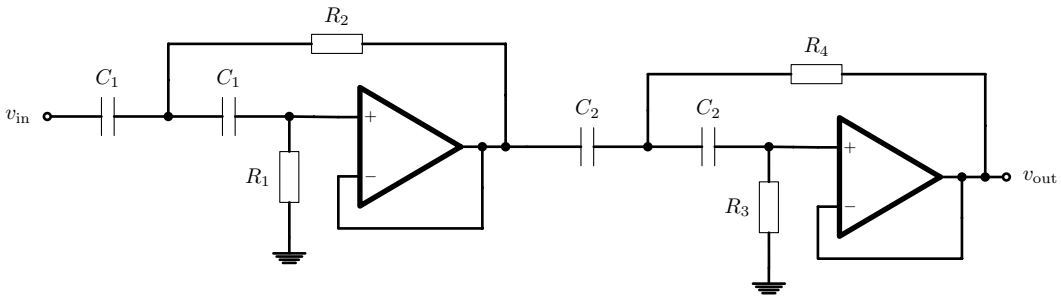



Figure 5.11: 4th Order Unity-Gain Sallen-Key High-Pass Filter.

• **First stage** :

Imposing $C_1 = 10\mu$F, so that acceptable values for $R_1$ and $R_2$ are obtained, $R_1$ and $R_2$ are calculated for a low cut-off frequency, $f_c$, of 10 mHz, using (5.17) and (5.18), respectively:

$$R_1 = \frac{1}{\pi f_c C_1 a_1} = 1.723 \text{ M}\Omega \rightarrow R_1 = 1.74 \text{ M}\Omega \tag{5.19}$$

$$R_2 = \frac{a_1}{4\pi f_c C_1 b_1} = 1.470 \text{ M}\Omega \rightarrow R_2 = 1.47 \text{ M}\Omega \tag{5.20}$$

• **Second stage** :

Assigning $C_2 = 10\mu$F, follows:

$$R_3 = \frac{1}{\pi f_c C_2 a_2} = 4.159 \text{ M}\Omega \rightarrow R_3 = 4.53 \text{ M}\Omega \tag{5.21}$$

$$R_4 = \frac{a_2}{4\pi f_c C_2 b_2} = 609.086 \text{ k}\Omega \rightarrow R_4 = 619 \text{ k}\Omega \tag{5.22}$$

Using PSpice A/D simulator from OrCAD Capture CIS 16.6 (2012 version), a simulation was performed to the complete filter configuration, displayed in Figure 5.5, with the listed values in table A.1. The schematic diagram is shown in Figure 5.13. Figure 5.12 shows the gain-magnitude frequency response of the eight order Butterworth Band-pass filter.

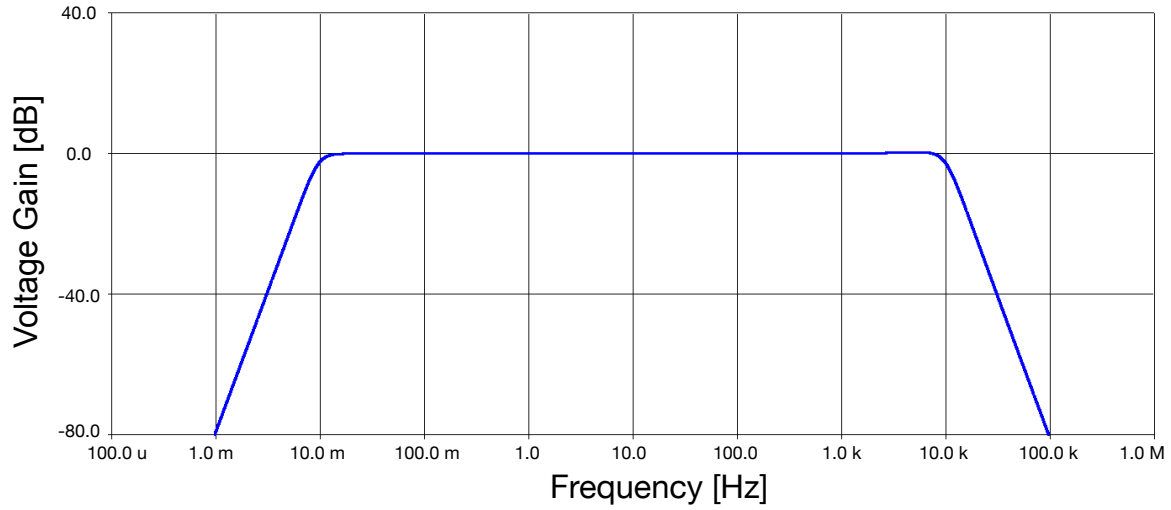



Figure 5.12: Band-Pass filter frequency response using PSpice A/D simulator.

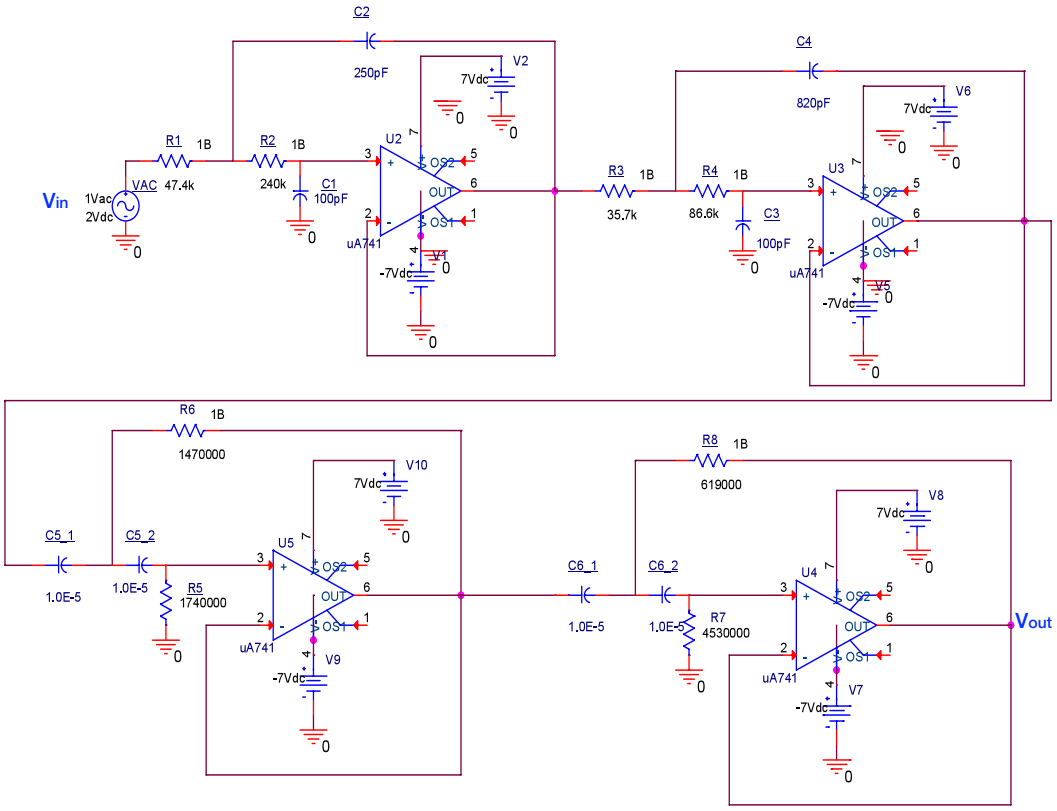



Figure 5.13: Schematic diagram of the Band-Pass filter in OrCAD Capture CIS.

| $R$ values [Ω] | | | | $C$ values [F] | | | |
|---|---|---|---|---|---|---|---|
| $R_1$ | 47.4k | $R_5$ | 1.74M | $C_1$ | 100p | $C_5$ | $10\mu$ |
| $R_2$ | 240k | $R_6$ | 1.47M | $C_2$ | 220p | $C_6$ | $10\mu$ |
| $R_3$ | 35.7k | $R_7$ | 4.53M | $C_3$ | 100p | | |
| $R_4$ | 86.6k | $R_8$ | 619k | $C_4$ | 820p | | |

Table 5.2: Values for the filter components.

## 5.4 Enhanced Howland Current Source

EIS measurements are performed in potentiostatic or galvanostatic mode. In potentiostatic mode, a sinusoidal potential perturbation is applied to the cell. The resulting current is measured to determine the impedance of the system. In galvanostatic mode, a sinusoidal current is applied to the cell instead. The resulting potential is now measured, to determine the impedance of the system.

A galvanostat device, such as the GAMRY Reference 3000 displayed in Figure 5.14, can easily control ampere currents to an accuracy of a few milliamperes.


Figure 5.14: GAMRY Reference 3000 galvanostat.

As the voltage signal in a galvanostatic EIS experiment is proportional to the applied current, a current source based excitation system is proposed due to the low impedance value of the tested $LiFePO_4$ cell (internal impedance is specified as less than 1 m$\Omega$ at 1 kHz in the $LiFePO_4$ datasheet). The maximum output current from an Arduino Due DAC is 15 mA. Therefore, a current amplifier is required in order to generate a greater voltage response from the cell. An enhanced Howland current source is chosen since it can be constructed using a single operational amplifier and five resistors.

The Howland circuit is modelled as a linear voltage-controlled current source (VCCS). The model is driven by an external and independent voltage source that drives the VCCS input, in this case, the variable frequency voltage source at the output of the filter [33].

The operation of the VCCS in Figure 5.15 is based on the fact that the output current, $I_L$, is measured as a voltage drop across $R_1$ [34]. Considering an infinite open-loop voltage gain, $A_d$, of the operational amplifier, the following equations can be written, by current analysis:

$$\frac{U_o - U_{-in}}{R_2} - \frac{U_{-in}}{R_3} = 0 \rightarrow U_{-in} = \frac{R_3}{R_2 + R_3} U_o \tag{5.23}$$

$$\frac{U_i - U_{+in}}{R_2} - \frac{U_{+in} - U_{Z_L}}{R_3} = 0 \rightarrow U_{+in} = \frac{U_{Z_L} \cdot R_2 + U_i \cdot R_3}{R_2 + R_3} \tag{5.24}$$

$$\frac{U_o - U_{Z_L}}{R_1} + \frac{U_{+in} - U_{Z_L}}{R_3} - I_L = 0 \tag{5.25}$$

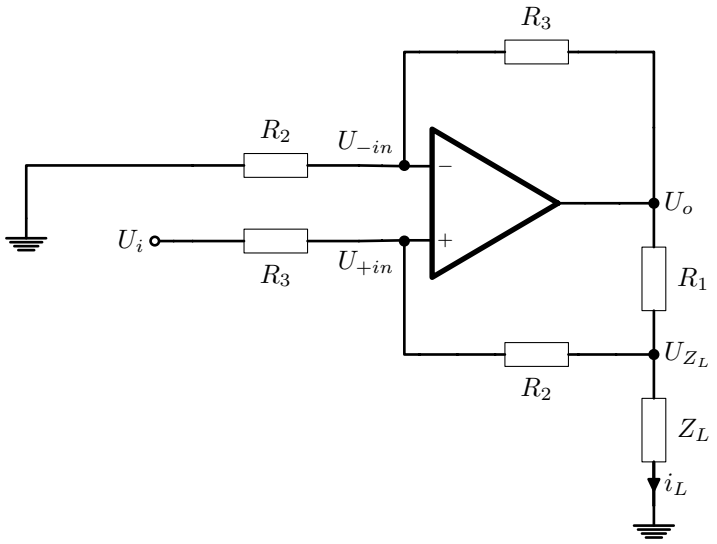



Figure 5.15: Enhanced Howland Current Source.

Assuming $U_{+in} = U_{-in}$, gives:

$$\frac{R_3}{R_2 + R_3} U_o = \frac{U_{Z_L} \cdot R_2 + U_i \cdot R_3}{R_2 + R_3} \rightarrow U_o = \frac{R_2}{R_3} U_{Z_L} + U_i \tag{5.26}$$

Replacing equations (5.24) and (5.26) in equation (5.25), yields:

$$\frac{(\frac{R_2}{R_3} U_{Z_L} + U_i) - U_{Z_L}}{R_1} + \frac{\frac{U_{Z_L} \cdot R_2 + U_i \cdot R_3}{R_2 + R_3} - U_{Z_L}}{R_3} - I_L = 0 \rightarrow I_L = \frac{U_i}{R_1} + (\frac{R_2 - R_3}{R_1 R_3} - \frac{1}{R_2 + R_3}) U_{Z_L} \tag{5.27}$$

According to (5.27), one can conclude that for a high value of both $R_2$ and $R_3$, while imposing $R_2 = R_3$, the output current is very close to be independent from the load impedance. Therefore, the equation (5.27) for the output current, simplifies to:

$$I_L \approx \frac{U_i}{R_1} \tag{5.28}$$

An enhanced Howland current source was designed to generate a 2 $A_{p-p}$ sinusoidal current. A 2 $V_{p-p}$

voltage signal was applied to the circuit as input, with $R_2$ = $R_3$ = 10 k$\Omega$ and $R_1$ = 1 $\Omega$. Hence, in order to apply to the terminals of the cell a 2 $A_{p-p}$ sinusoidal current, a high-current operational amplifier is required. An OPA548 from Texas Instruments was the choice considering that it allows the output current limit to be adjusted from 0 A to 5 A.

Using PSpice A/D simulator from OrCAD Capture CIS CIS 16.6 (2012 version), a simulation was performed to the Howland current source. The circuit model is shown in Figure 5.16. Figure 5.17 shows both input voltage $U_i$, and output current $I_L$, respectively, according to equation (5.28).

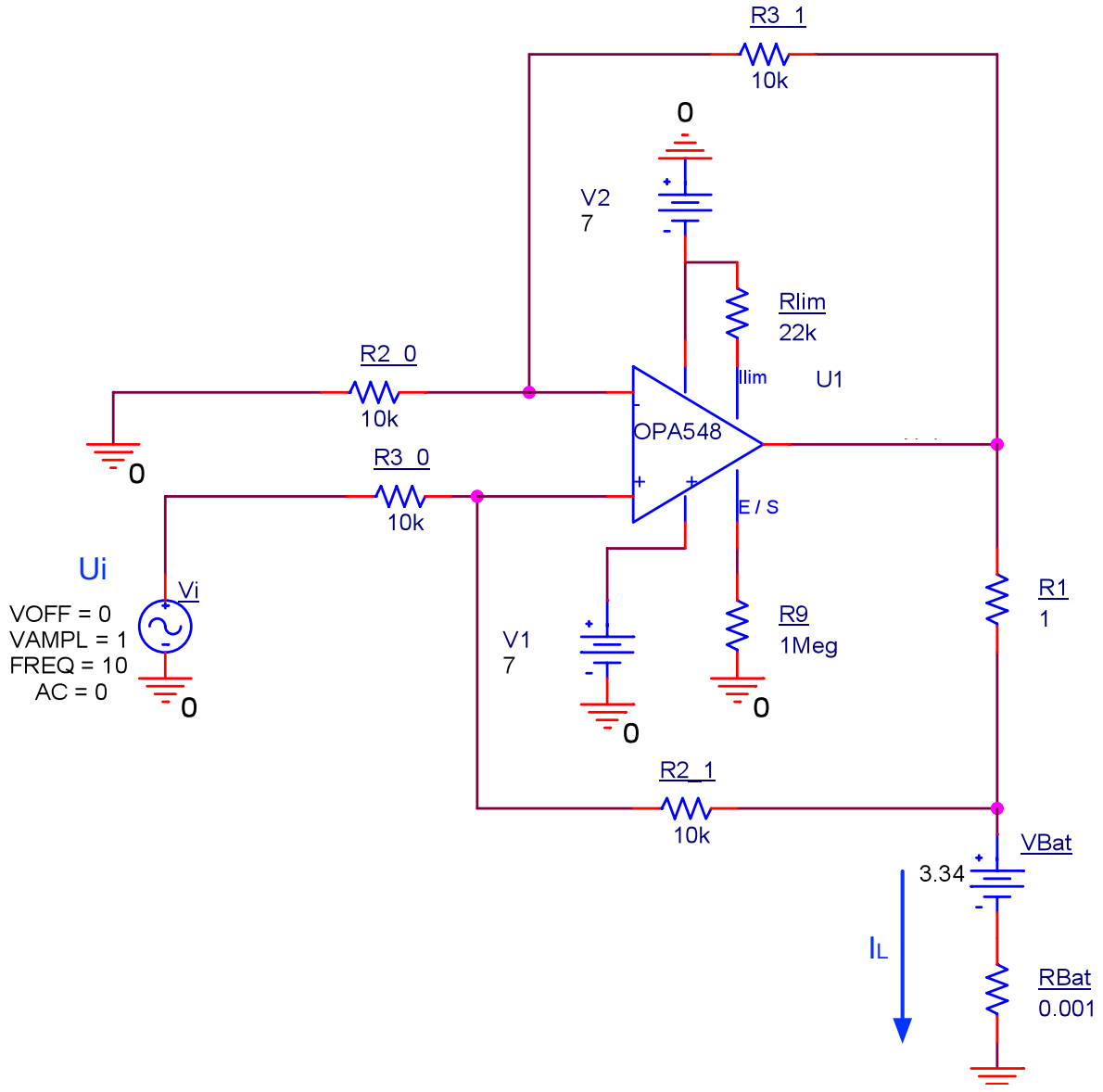



Figure 5.16: Enhanced Howland Current Source Schematic in PSpice A/D simulator.

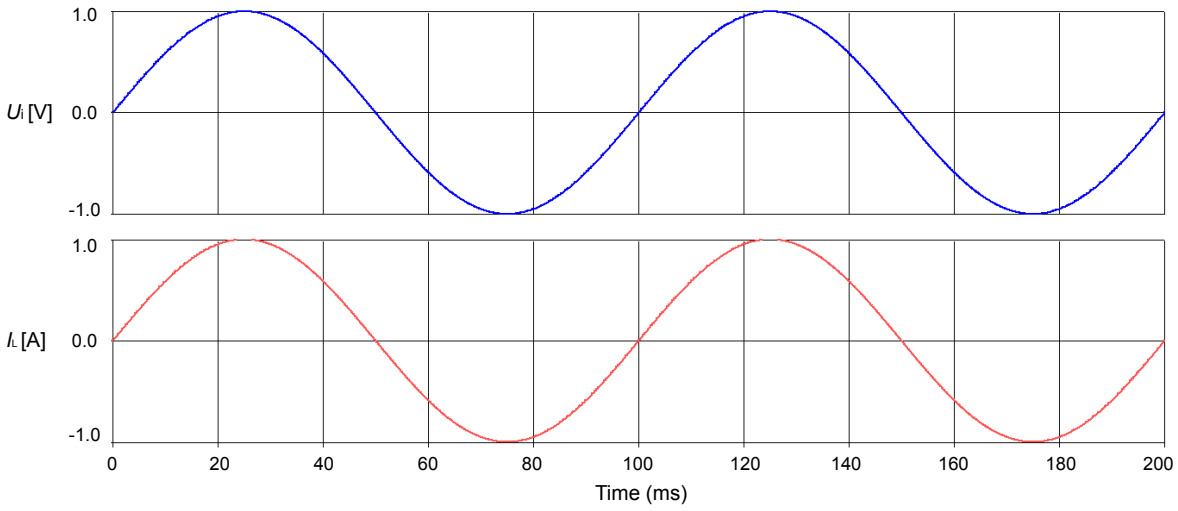



Figure 5.17: Input voltage, $U_i$, and output current, $I_L$ simulations using PSpice A/D simulator.

## 5.5 Data Acquisition

A second Arduino device was used to read the sinusoidal current imposed to the cell and its voltage response. The Arduino Due integrated ADC input has a 12 bit resolution. So, the smallest change in the analog signal that will result in a change in the digital output, called least significant bit (LSB) voltage, will be:

$$N_{LSB} = \frac{U_R}{2^N} = \frac{3.3}{2^{12}} = 0.81 \text{ mV}\,, \tag{5.29}$$

where $U_R$ is the Arduino reference voltage (the operating voltage of the board) and $N$ is the number of bits in the digital output given by the ADC resolution. In order to precisely acquire lower voltage and current increments, particularly relevant in this project due to the low impedance of the cell, a higher resolution is required. Hence, the approach of using external ADCs having a 16 bit resolution was taken. With this solution, the value of each digital word in the digital output of the ADC will now be:

$$N_{LSB} = \frac{U_R}{2^N} = \frac{3.3}{2^{16}} = 0.05 \text{ mV} \tag{5.30}$$

The current is measured by a LEM hall effect transducer current sensor (LTSR 6-NP). It measures bi-directional currents up to 6 A RMS from DC to 200 kHz.

### 5.5.1 Sampling

Analog-to-digital converters (ADCs) translate analog quantities to digital language, used in information processing, computing, data transmission and control systems [35]. Two AD7680 (by Analog Devices) 16-bit successive approximation analog to digital converters were employed, one for the voltage at the

cell terminals, the other for the voltage output of the current transducer. The AD7680 operates from a single 2.5 V to 5.5 V power supply and features throughput rates up to 100 kSPS.

Both voltage and current are sampled and, after the analog to digital conversion, the sequence of digital words according to the AD7680 transfer characteristic in Figure 5.18 and associated to the acquired signals are obtained as:

$$N_{LSB_v}(k_s\Delta t) = \frac{v_{cell}(k_s\Delta t)}{V_{DD}} \cdot 2^N \tag{5.31}$$

$$N_{LSB_i}(k_s\Delta t) = \frac{v_{HS_{cell}}(k_s\Delta t)}{V_{DD}} \cdot 2^N \tag{5.32}$$

where $V_{DD}$ is the supply voltage of each ADC, $k_s$ is the number of the sample and $\Delta t$ being the time interval between acquired samples.

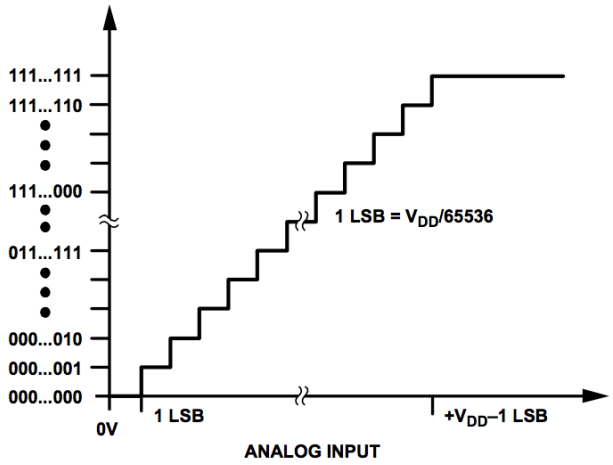



Figure 5.18: AD7680 Transfer Characteristic [36].

The sequence of digital words is later stored in the Arduino Due 96 KBytes SRAM. These words are stored as float data-type, a 4 byte (32 bit) binary number, yielding a range of -3.40$\times$ $10^{38}$ to +3.40$\times$ $10^{38}$.

Due to memory limitation, one can only afford to store a finite number of digital words when sampling the variable frequency signals. Given this limitation, it was chosen to store 320 samples for each of the frequencies, taking into account that there are 22 different frequencies resulting in two stored matrix's of 22 by 320 digital words, each one occupying 4 bytes, taking 56 KBytes of the 96 KBytes. Hence, the control of the sampling frequency is mandatory.

To attain the control of the sampling frequency, so that 320 samples are stored per frequency, the Arduino that is responsible for acquiring both signals requires the value of the frequency of the sinusoidal current being imposed to the cell during the acquisition interval. This is achieved by creating a communication channel via I2C protocol between the Arduino in charge of generating the variable-frequency AC voltage signal and the Arduino responsible for the data acquisition, as illustrated by Figure 5.19.

#### 5.5.1.1 I2C Communication

Using the I2C communication protocol, each time the frequency variation sub-routine is summed in the source Arduino (resulting in a change in the voltage frequency at the output of the source Arduino DAC), the value of the new frequency is transmitted to the slave Arduino. The I2C protocol involves using two lines to send and receive data: a serial clock pin (SCL) that the Arduino Master board pulses at a regular interval, and a serial data pin (SDA) over which data is sent between the two devices. As the clock line changes from low to high, a single bit of information is transferred from the I2C master board (voltage source Arduino) to the I2C slave (acquisition Arduino) device over the SDA line. After 32 clock pulses (eight bits, four bytes, for each frequency float) the transmission is concluded and the slave Arduino stores the frequency value. Follow, the sampling frequency is calculated so that only 320 samples during each acquisition time window (five complete cycles of the generated signal) are acquired.

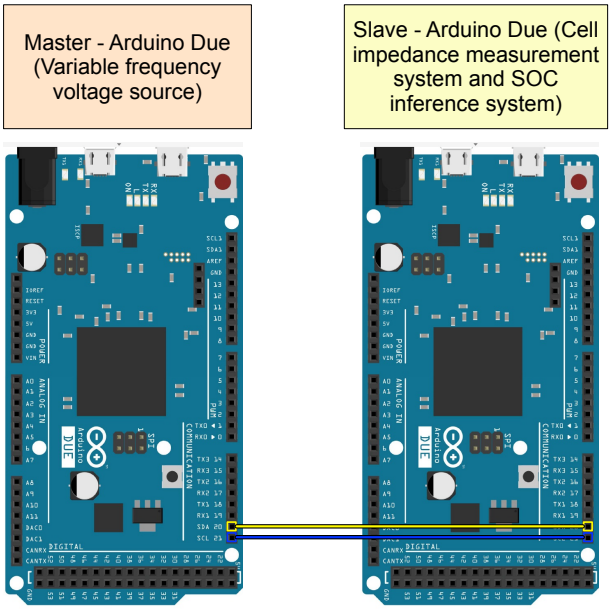



Figure 5.19: Master and slave devices I2C connections.

#### 5.5.1.2 Oversampling and averaging

The process of signal acquisition in this project requires a fine resolution due to the small fluctuations in the sampled voltage and current signals. One way to increase the resolution of the ADC output is by oversampling and averaging functions. When oversampling, the ADC samples both voltage signals (voltage at the terminals of the cell and output of the hall current sensor) at a higher rate than the system's required sampling rate, accumulating enough samples in the specific sampling period, later averaging them. This method is comparable to a low-pass filter, attenuating the signal fluctuation and noise [37].

The $m$ extra samples acquired during the sampling interval and obtained by oversampling the signal, are added and the result is right shifted by $n$ positions, where $n$ represents the extra bit of resolution. A right shift in a binary number is the same as dividing the binary number by 2. In this project, each

sample is oversampled 80 times and later the accumulated value is divided by this value (80), giving the ADC resolution an increment of 6 bits

$$\text{Extra resolution } = \log_2(80) = 6.321 \text{ bit} \tag{5.33}$$

So, instead of 16 bits as previously, both ADCs now have 22 bits of resolution.

#### 5.5.1.3 Moving average digital filter

In order to further improve the random noise reduction achieved by the oversampling and averaging process, described in the previous section, a moving average filter was implemented, this way reducing random white noise while maintaining a sharp step response. The moving average filter works by averaging a number of points from the sampled signal to produce each point in the output stored signal [38]. Each point in the output of the filter is given by:

$$y(i) = \frac{1}{M} \sum_{j=0}^{M-1} x(i-j) \tag{5.34}$$

where $x(i-j)$ is the input signal, $y(i)$ the output signal and $M$ is the total number of points used in the moving average. For instance, in a 4 points moving average filter, point 60 in the output signal is obtained as follows:

$$y(60) = \frac{x(60) + x(59) + x(58) + x(57)}{4} \tag{5.35}$$

Figures 5.20 (a) and (b) illustrate the attenuation effect of the moving average filter in a signal with random noise. The amount of noise reduction in each point in the output of the filter is equal to the square-root of the number of points in the average ($M$, in equation (5.34)) [38]. In this project, a 22 point moving average filter was applied to both voltage and current acquired signals, reducing the random noise by a factor of 4.7.

### 5.5.2 Discrete Fourier Transform

In this project, the Discrete Fourier transform (DFT) is the chosen method to estimate both voltage and current phasors. After sampling, stored data at discrete time step is available for processing. Hence, the Fourier-transform calculation has been performed in discrete environment and is named as Discrete Fourier Transform or DFT [39]. The discrete Fourier transform of a general sequence $x[n]$ of finite duration is determined as follows [40]:

$$X(m) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi nm/N} \tag{5.36}$$

In (5.36), the term $x(n)$ is a discrete sequence of time-domain sampled values of the continuous variable $x(t)$; $n$ is the time-domain index of the input samples; $N$ is the number of samples of the input sequence

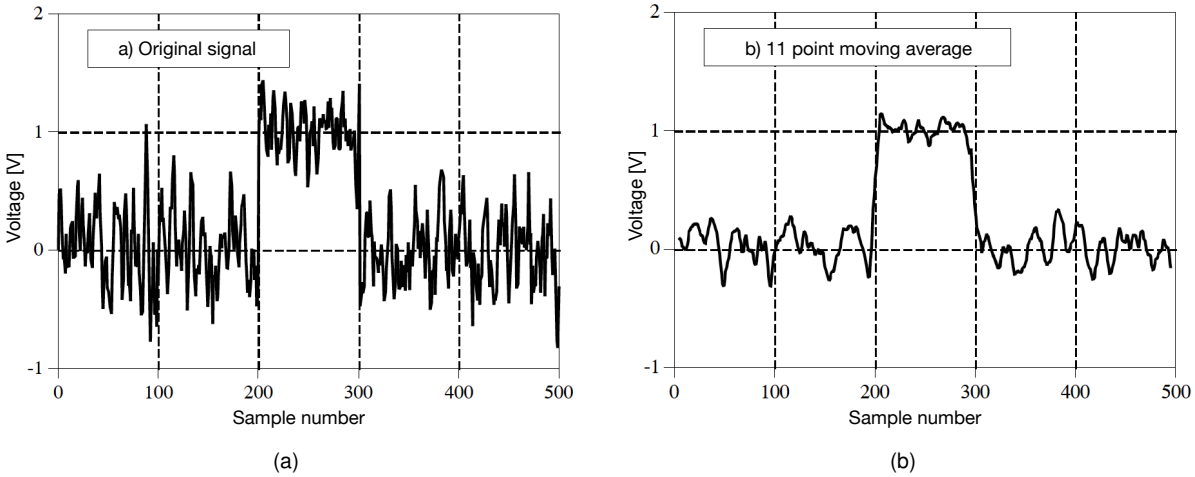



Figure 5.20: Example of a moving average filter applied to a voltage pulse [38]. In (a) the signal is filled with random noise and in (b) a moving average filter with 11 points is applied.

and the number of frequency points in the DFT output; $m$ is the index of the DFT output in the frequency domain, being equivalent to the number of complete cycles that occur over the $N$ points of the signal.

A sinusoid $x(t)$ with frequency $mf_0$ with a Fourier series [39]:

$$x(t) = a_m \cos(2\pi m f_0 t) + b_m \sin(2\pi m f_0 t) = \tag{5.37}$$

$$= \sqrt{a_m^2 + b_m^2}\ \cos(2\pi m f_0 t + \phi) \tag{5.38}$$

has a phasor representation as follows:

$$\overline{X(m)} = \sqrt{a_m^2 + b_m^2}\, e^{j\phi}, \tag{5.39}$$

$$\phi = \arctan(-\frac{b_m}{a_m}) \tag{5.40}$$

The phasor in its complex form becomes:

$$\overline{X(m)} = a_m - jb_m \tag{5.41}$$

Likewise, when applying Euler's formula to equation (5.36), the phasor representation of the $m$th harmonic component is equivalent to:

$$\overline{X(m)} = \sum_{n=0}^{N-1} x(n)[\cos(2\pi nm/N) - j\sin(2\pi nm/N)] \tag{5.42}$$

Defining both cosine and sine sums as follows:

$$\overline{X_c(m)} = \sum_{n=0}^{N-1} x(n)\cos(2\pi nm/N), \tag{5.43}$$

$$\overline{X_s(m)} = \sum_{n=0}^{N-1} x(n)\sin(2\pi nm/N), \tag{5.44}$$

results in a phasor, $X(m)$, given by:

$$\overline{X(m)} = \overline{X_c(m)} - j\overline{X_s(m)} \tag{5.45}$$

#### 5.5.2.1 4-Cycles Based Discrete Fourier Transform (DFT) Algorithm

A 4-cycle DFT considers a window size of:

$$N = 4\frac{fs}{fn} \tag{5.46}$$

Which is four times greater that considering only one cycle. This yields to an attenuation of high and low frequency harmonics, significantly improving the output results of both voltage and current phasor estimation, for each frequency. The reason behind a better resolution when acquiring more cycles is that it decreases the effect of spectral leakage, a phenomena associated with the non-cyclical input of the Fourier-transform.

To understand the significance of this problem, the following example, taken from [41] , is given: A 64-point DFT of a given sequence is indicated by the dots in Figure 5.21 (a). Figure 5.21 (a) also shows the $m = 4$ sinewave analysis frequency, superimposed over the input sequence, to remind the reader that the analytical frequencies always have integer number of cycles over the total interval of 64 points. The sequence is a sinewave with exactly three cycles in the $N$ = 64 samples. Figure 5.21 (b) shows the first half of the DFT of the input sequence and indicates that the sequence has an zero average value ($X(0) = 0$) as well as no signal components in other frequencies besides the $m = 3$ frequency. The sum of the products of the input sequence and the $m = 4$ analysis frequency is zero, showing that the correlation of the input sequence with the $m = 4$ analysis frequency is zero, just like all the other analysis frequencies, not represented in Figure 5.21 (a).

Representing the spectral leakage problem, the dots in Figure 5.21 (c) show an input sequence having 3.4 cycles over the $N = 64$ samples. Due to a non-integer number of cycles over the 64-sample interval, input energy has leaked into all other DFT analysis frequencies, as shown in Figure 5.21 (d). Now, the m = 4 analysis frequency, as an example, is different than zero because the sum of the products of the input sequence and the m = 4 analysis frequency is no longer zero.

Processing more than one cycle is a good practice since it increases the number of complete cycles in the sampled interval, reducing the effect of leakage but still does not fully solves the leakage problem. In this project, with the purpose of reducing the spectral leakage effect in both voltage and current phasor estimation, a technique known as windowing was applied.

Windowing works by selecting the DFT input data in order to reduce the non-integer number of cycles over the N samples interval. This was achieved with a rectangular window, leading to a grater attenuation of high and low frequency harmonics in the DFT output. To illustrate this idea, in the case previously presented, the input sequence with 3.4 cycles was windowed in order to select 3.0 cycles, as shown in Figure 5.22.

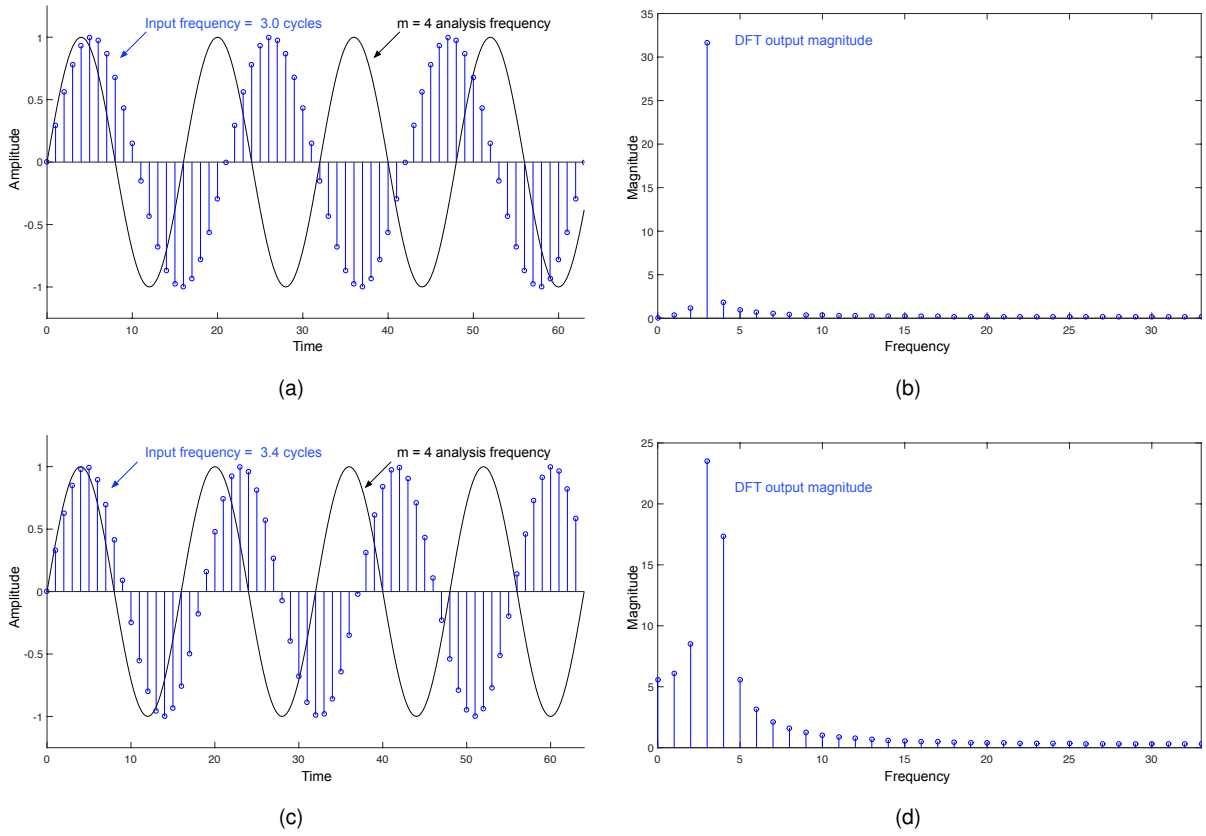



Figure 5.21: 64 samples sequence DFT: (a) 3.0 cycles sequence and m = 4 analysis frequency; (b) DFT output magnitude of the 3.0 cycles sequence; (c) 3.4 cycles sequence and m = 4 analysis frequency; (d) DFT output magnitude of the 3.4 cycles sequence, adapted from [41].

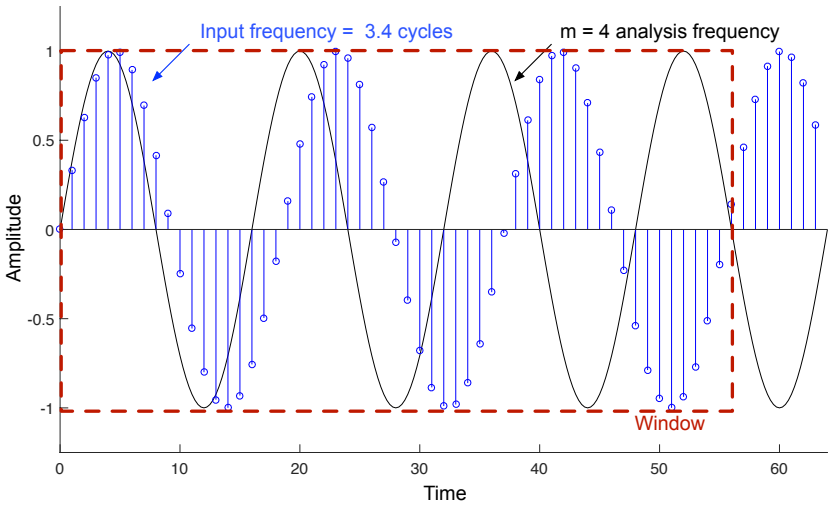



Figure 5.22: 64 samples sequence: application of the windowing process to the 3.4 cycles sequence, and m = 4 analysis frequency.

#### 5.5.2.2 Impedance phasor calculation

Employing the DFT algorithm to both voltage and current samples, the impedance for each frequency $k$ is obtained:

$$\overline{Z_k(m)} = |Z_k(m)|e^{j\phi_{Z_k}} \tag{5.47}$$

where the impedance magnitude of the $m$th harmonic, $|Z_k(m)|$ and phase angle of the impedance, $\phi_{Z_k}(m)$ are obtained as follows:

$$|Z_k(m)| = |\frac{U_k(m)}{I_k(m)}| = |\frac{U_{k_c}(m) - jU_{k_s}(m)}{I_{k_c}(m) - jI_{k_s}(m)}| = \frac{\sqrt{U_{k_c}(m)^2 + U_{k_s}(m)^2}}{\sqrt{I_{k_c}(m)^2 + I_{k_c}(m)^2}} \tag{5.48}$$

$$\phi_{Z_k}(m) = \phi_{U_k}(m) - \phi_{I_k}(m) = \arctan(-\frac{U_{k_s}(m)}{U_{k_c}(m)}) - \arctan(-\frac{I_{k_s}(m)}{I_{k_c}(m)}) \tag{5.49}$$

The final setup of the proposed EIS measurement method is displayed in Figure 5.23, presenting the three main blocks composing the system, first enumerated in the beginning of this chapter, in Figure 5.1, both Arduino Dues as well as the assembled PCB.

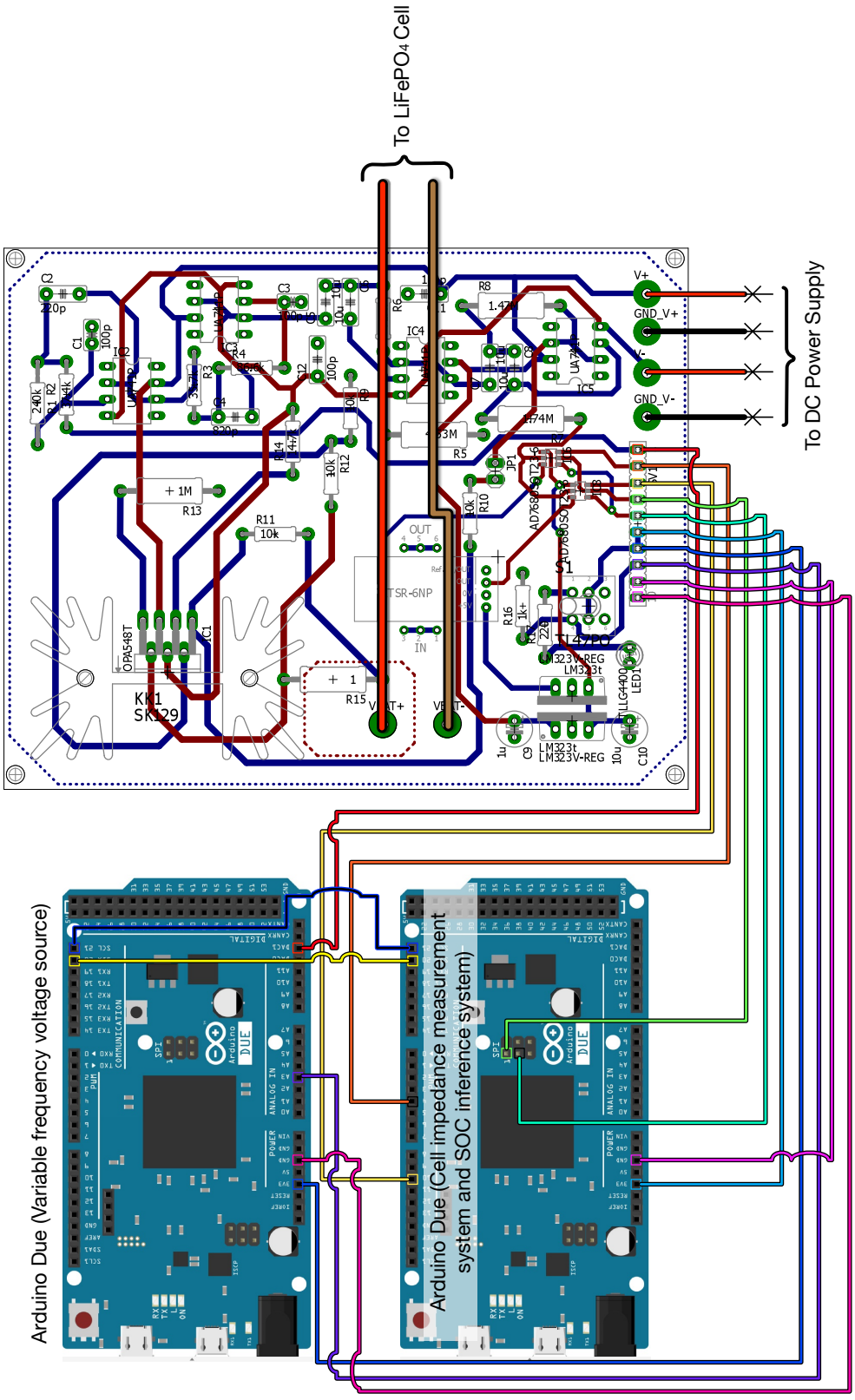



Figure 5.23: Implemented system setup, presenting both source and acquisition Arduino Dues in addition to the designed PCB.

## 5.6 Adaptive Neuro Fuzzy Inference Systems applied to SOC estimation

The impedance spectra for each SOC is obtained through the previous EIS measurement system. This way, an adaptive neuro-fuzzy inference system that uses two input variables, introduced in section 4.2, has been implemented. The input variables are the real part of the measured complex impedance and its imaginary part. The output of the ANFIS system will be the battery cell inferred SOC. The estimation of the battery SOC will be achieved through a comparative analysis of its actual impedance spectra with the impedance spectra database previously built from past EIS measurements for pre-defined SOC values, as it was previously explained in section 3.2.

Both inputs, real and imaginary impedance parts, are mapped to their own membership functions using the Fuzzy Logic Toolbox function existent in MATLAB. Instead of triangular membership functions, as presented in the previous example in section 4.1, Gaussian ones will be used. The Gaussian function, represented in Figure , expressed in equation 5.1, is specified with two parameters, $m$ and $\sigma$, as follows [42]:

$$f(x, m, \sigma) = e^{-\frac{(x-m)^2}{\sigma^2}} \tag{5.50}$$

where $m$ denote the mean value, corresponding to the centre of the function, and $\sigma$, the standard deviation, giving its width.

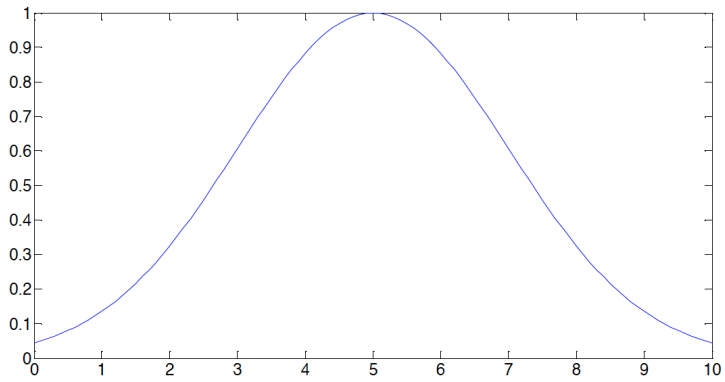



Figure 5.24: Gaussian curve membership function (m = 5 and $\sigma$ = 2) [26].

To properly distinguish the different SOC EIS measurements, each one having $N$ different points, $N$ representing the number of different frequencies in the frequency sweep, the model requires a certain number of IF-THEN rules in order to differentiate the precessed data. The necessary number of rules providing an accurate system is approximately half the total number of impedance data points stored in the database. The database will be composed by $M$ impedance spectras, one for each pre-defined SOC. Each impedance spectra contains $N$ points, one for each frequency, and each of these points is

defined by its real value and imaginary value. Hence, the total number of rules comes:

$$N_{rules} = \frac{M_{SOCs} \cdot N_{frequencies} \cdot N_{inputs}}{2} \tag{5.51}$$

After running the Fuzzy Logic Toolbox function, a FIS file is given as output, modelling the Sugeno fuzzy inference model, described in section 4.2, containing the membership function parameters for both real and imaginary impedance parts inputs and the first-order polynomial parameters, describing the output singleton membership functions.

Following the modelling process, the fuzzy inference system is implemented in the acquisition Arduino Due, setting the IF-THEN rules, where the subsets of each rule are described by their membership functions, characterized by the tailored parameters computed by the neuro-adaptive technique and displayed in the FIS file. The combination of input membership functions and singleton outputs for each input variable results in different rules of the system:

Rule 1: If $Re(Z)$ is $\mu^{(1)}_{Re(Z)}$ and $-Im(Z)$ is $\mu^{(1)}_{-Im(Z)}$ , then $\omega^{(1)} = m_1 Re(Z) + n_1(-Im(Z)) + k_1$

Rule 2: If $Re(Z)$ is $\mu^{(2)}_{Re(Z)}$ and $-Im(Z)$ is $\mu^{(2)}_{-Im(Z)}$ , then $\omega^{(2)} = m_2 Re(Z) + n_2(-Im(Z)) + k_2$

Rule 3: If $Re(Z)$ is $\mu^{(3)}_{Re(Z)}$ and $-Im(Z)$ is $\mu^{(3)}_{-Im(Z)}$ , then $\omega^{(3)} = m_3 Re(Z) + n_3(-Im(Z)) + k_3$

$$\vdots$$

Rule N: If $Re(Z)$ is $\mu^{(N)}_{Re(Z)}$ and $-Im(Z)$ is $\mu^{(N)}_{-Im(Z)}$ , then $\omega^{(N)} = m_N Re(Z) + n_N(-Im(Z)) + k_N$

Figure 5.25 shows the reasoning mechanism for the Sugeno model, described in section 4.1.3.1, applied to the SOC estimation.

This process is implemented in the acquisition Arduino, automatically inferring the SOC for each of the $N$ frequency points in the EIS current measured impedance spectra.

In layer 1, every node is an adaptive node with a node function equal to the membership function, for which the parameters $m^{(i)}$ and $\sigma^{(i)}$, characterizing each gaussian membership function, have been estimated by means of the Fuzzy Logic Toolbox function.

In layer 2, each node is fixed and represents the firing strength associated to each rule $i$:

$$f^{(i)}(Re(Z), -Im(Z)) = \mu^{(i)}_{Re(Z)}(Re(Z)) \cdot \mu^{(i)}_{-Im(Z)}(-Im(Z)) \tag{5.52}$$

In layer 3 each node is fixed. Now the incoming firing strength is normalized to the sum of all rules firing strengths:

$$\overline{f^{(i)}(Re(Z), -Im(Z))} = \frac{f^{(i)}(Re(Z), -Im(Z))}{\sum_{k=1}^{N} f^{(k)}(Re(Z), -Im(Z))} \tag{5.53}$$

where $N$ represents the total number of rules, given by expression (5.51).

In layer 4 each node is adaptive. At this point, the firing rules are multiplied by their correspondent singletons, for which the parameters $m_i$, $n_i$ and $k_i$ , characterizing each output singleton, have been

estimated through the Fuzzy Logic Toolbox function.

$$\overline{f^{(i)}(Re(Z),-Im(Z))}\cdot\omega^{(i)}=\overline{f^{(i)}(Re(Z),-Im(Z))}\cdot(m_iRe(Z)+n_i(-Im(Z))+k_i) \tag{5.54}$$

Layer 5 is composed by a single fixed node, computing the SOC value output as the sum of all incoming signals, representing the centre of gravity or the weighted average of all rule outputs:

$$SOC=\sum_{k=1}^{N}(\overline{f^{(i)}(Re(Z),-Im(Z))}\cdot\omega^{(i)})=\frac{\sum_{k=1}^{N}(f^{(l)}(Re(Z),-Im(Z))\cdot\omega^{(i)})}{\sum_{k=1}^{N}f^{(i)}(Re(Z),-Im(Z))} \tag{5.55}$$

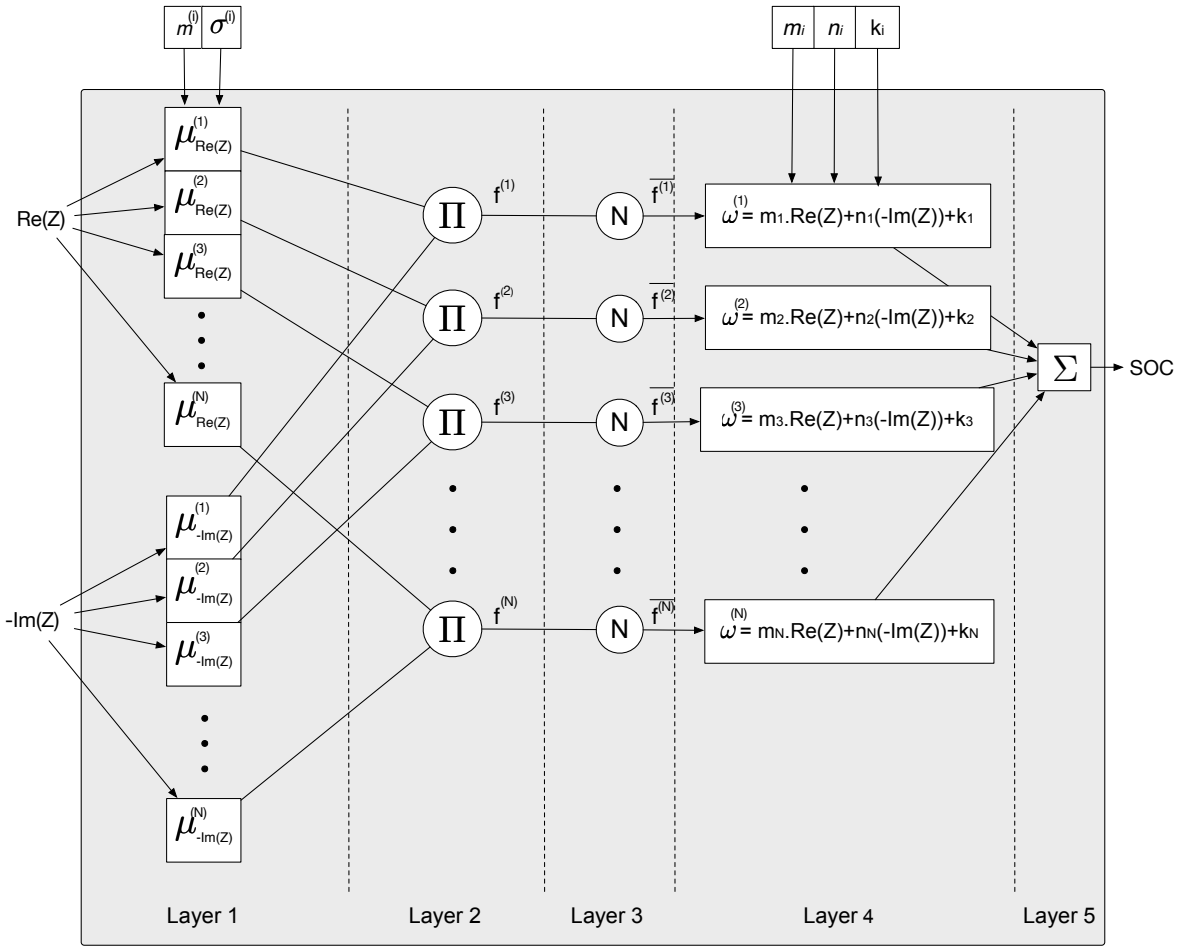



Figure 5.25: Structure of the five-layer adaptive neuro-fuzzy system for the Sugeno model implemented in the acquisition Arduino Due.

# Chapter 6

# Results

This chapter aims to verify the functioning of the implemented EIS measurement system together with Fuzzy logic SOC inference method. It presents information and results about both processes with the aid of a case study considering a 160 Ah capacity $LiFePO_4$ cell having a 70% SOC.

## 6.1 Assumptions

In order to run the above mentioned and implemented techniques, the following listed premises were defined so that some of the variables affecting the battery cell impedance were controlled:

- Temperature: During the experiments, the battery cell was maintained at a room temperature of 17 ºC with a temperature fluctuation of $\pm$ 1ºC.
- Relaxation Time: After each battery cell discharge, the resting time of the cell was established as 10 minutes.
- Charge/Discharge rates: The cell was charged at a rate of 7.4 Ah and discharged at a rate of 16 Ah.
- Operating Voltages: The impedance spectra of the cell was measured galvanostatically in a voltage range between 2.8 and 3.6 V, corresponding to 15% and 100% SOC, respectively.
- Impedance database: Generated during one full discharge cycle (100% - 15%). The battery cell was later fully charged again and discharged to certain SOC's to present the reader the proposed case studies.

Figure 6.1 displays the experimental test scenario of the developed system.

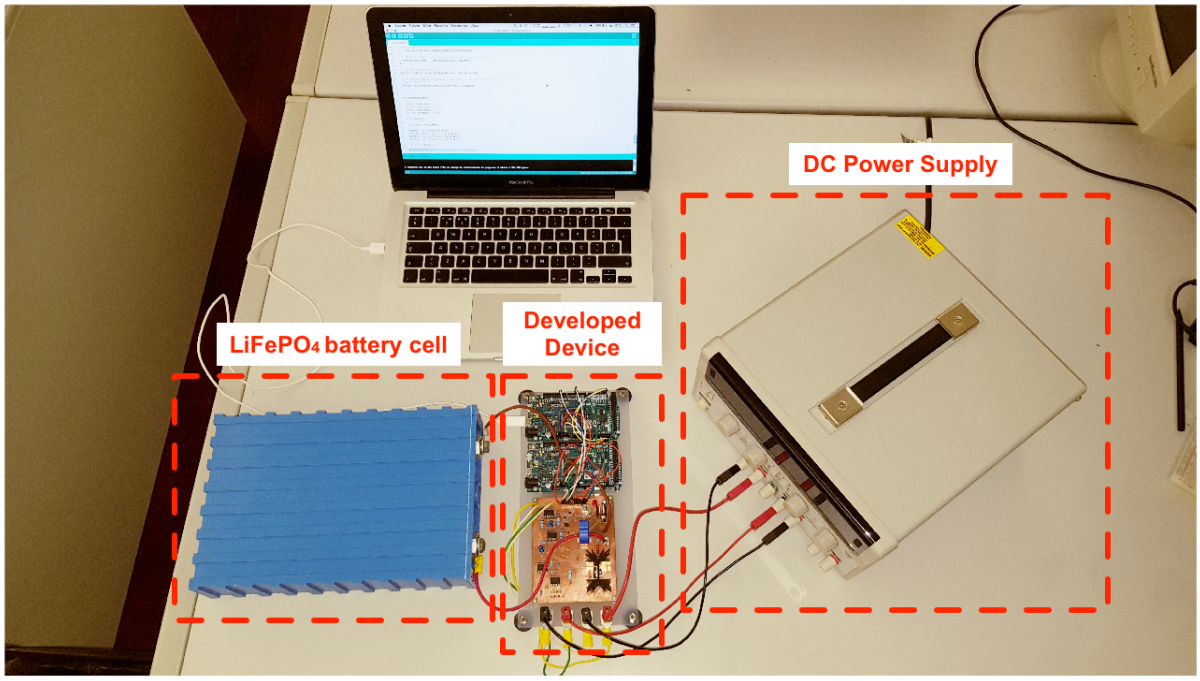



Figure 6.1: Experimental scenario.

## 6.2 Validation of the EIS measurement system implementation

The variable frequency voltage source provided by the Digital Direct Synthesis (DDS) technique in the source Arduino Due was programmed with a 2000 digital word look-up table, as described in section 5.2, supplying at the output of the Arduino DAC a voltage with a duration of six complete cycles, as follows:

$$U_{DAC}(t) = U_{o_{AC}} \sin(2\pi f_i t + \varphi) + U_{o_{DC}} \text{ [V]} \tag{6.1}$$

where $U_{o_{AC}} = U_{o_{DC}} = 1.6114\ V$; $\varphi = \frac{\pi}{6}\ rad$ and a variable frequency value $f_i$, a variable frequency value, so that the frequency sweep is carried, for each of the listed values in table 6.2.

After the filtering stage, the voltage in equation (6.1), as explain in section 5.3, results in:

$$U_{out_{Filter}}(t) = U_{o_{AC}} \sin(2\pi f_i t + \varphi) = 1.6114 \sin(2\pi f_i t + \frac{\pi}{6}) \text{ [V]} \tag{6.2}$$

This voltage is then presented to the dimensioned Enhanced Howland Current Source, as in section 5.4, so that accordingly to equation (5.28), an excitation current is imposed to the battery cell:

$$I_L(t) \approx \frac{U_{out_{Filter}}(t)}{R_1} = \frac{1.6114 \sin(2\pi f_i t + \frac{\pi}{6})}{1} = 1.6114 \sin(2\pi f_i t + \frac{\pi}{6}) \text{ [A]} \tag{6.3}$$

Both voltage and current are sampled at a sampling frequency dependent on that transmitted from the source Arduino, listed in table 6.2, to the acquisition one, via I2C communication, detailed in section 5.5.1.1.

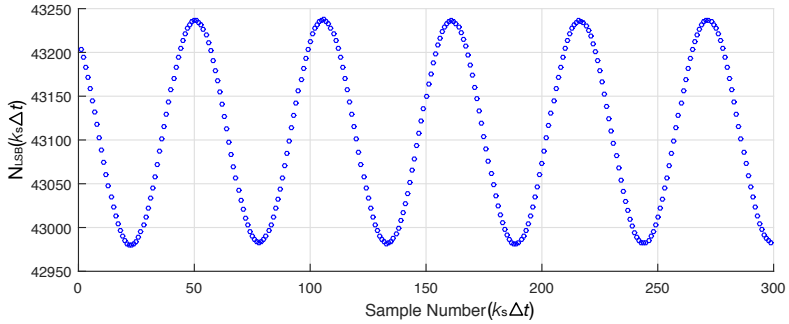
| Frequency (Hz) | | | |
|---|---|---|---|
| $f_1$ | 0.0130 | $f_{12}$ | 0.3160 |
| $f_2$ | 0.0180 | $f_{13}$ | 0.4220 |
| $f_3$ | 0.0237 | $f_{14}$ | 0.5630 |
| $f_4$ | 0.0316 | $f_{15}$ | 0.7500 |
| $f_5$ | 0.0422 | $f_{16}$ | 1.0000 |
| $f_6$ | 0.0563 | $f_{17}$ | 1.3390 |
| $f_7$ | 0.0750 | $f_{18}$ | 1.7680 |
| $f_8$ | 0.1000 | $f_{19}$ | 2.3720 |
| $f_9$ | 0.1330 | $f_{20}$ | 3.1590 |
| $f_{10}$ | 0.1800 | $f_{21}$ | 4.1780 |
| $f_{11}$ | 0.2370 | $f_{22}$ | 5.6340 |

Table 6.1: Programmed frequencies in the variable frequency voltage source Arduino Due, for which the EIS measurement system was realized.

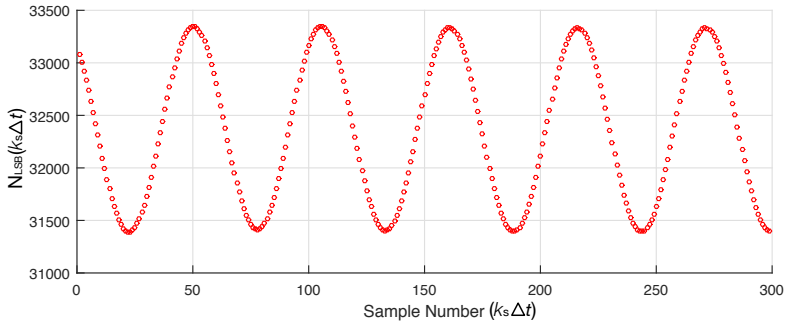
The acquisition Arduino is programmed in order to store 320 samples for each one of the 22 frequencies in table 6.2 so that approximately 280 samples are correctly acquired during 5 complete cycles, while oversampling and digital filtering, as descibed in section 5.5.1.2.

In order to graphically represent the data acquisition process, a 160 Ah capacity $LiFePO_4$ cell having a 70% SOC value, following the conditions described in section 6.1, is used as a test subject. As an example, the acquired voltage at the terminals of the cell and excitation current signals for a frequency of 0.0422Hz are presented in Figure 6.2 (a) and 6.2 (b), respectively.

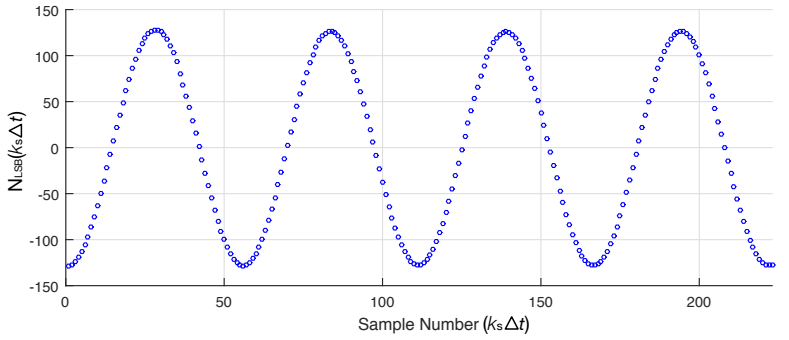
As it can be observed in Figures 6.2 (a) and (b), for a frequency of 0.0422 Hz, 280 samples during five complete cycles are stored, this process being performed 22 times, the number of pre-defined frequencies. The next step is applying a rectangular window to each of the stored arrays so that only the samples referring to 4 cycles of signal are processed by the discrete Fourier transform algorithm, this way minimizing spectral leakage, previously explained in 5.5.2.1. The result of the windowing process to both voltage and current sequences can be observed in Figure 6.2 (c) and 6.2 (d).



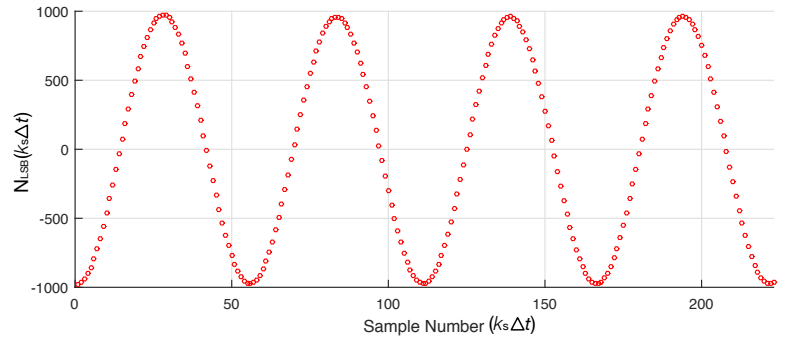

(a)




(b)




(c)




(d)

Figure 6.2: Acquired voltage at the terminals of the cell and excitation current signals for a frequency of 0.0422Hz: (a) Voltage sequence before windowing; (b) Current sequence before windowing; (c) Voltage sequence after windowing; (d) Current sequence after windowing

Now, the DFT algorithm to both windowed voltage and current samples, for each of the frequencies in table 6.2, is applied, so that the phasors for each of the variables, accordingly to section 5.5.2, are obtained. Afterwards, each digital word contained in the stored voltage and current arrays is converted back to its units following the inverse expressions of (5.31) and (5.32):

$$v_{cell}(k_s\Delta t) = \frac{V_{DD}}{N_{LSB_v}(k_s\Delta t)) \cdot 2^N} = \frac{5}{N_{LSB_v}(k_s\Delta t)) \cdot 65535} = \frac{0.0000762939}{N_{LSB_v}(k_s\Delta t))} \text{ [V/level]} \tag{6.4}$$

$$I_{cell}(k_s\Delta t) = C_{HS} \cdot v_{HS_{cell}}(k_s\Delta t) = C_{HS} \cdot \frac{V_{DD}}{N_{LSB_i}(k_s\Delta t)) \cdot 2^N} = \tag{6.5}$$

$$= 9.546 \cdot \frac{0.0000762939}{N_{LSB_v}(k_s\Delta t))} = \frac{0.0007283}{N_{LSB_i}(k_s\Delta t))} \text{ [A/level]} \tag{6.6}$$

where $C_{HS}$ is the hall effect transducer current sensor voltage-to-current conversion constant.

The impedance data assessed through the acquired voltage and current phasors, as described in section 5.5.2.2, is represented graphically in a Bode plot expressing the impedance magnitude and phase angle in relation to frequency in Figure 6.3 and 6.4, respectively. In Figure 6.5 the same measured impedance data , related to a 70% SOC, is represented through a Nyquist plot, expressing the imaginary impedance versus the real impedance of the system.

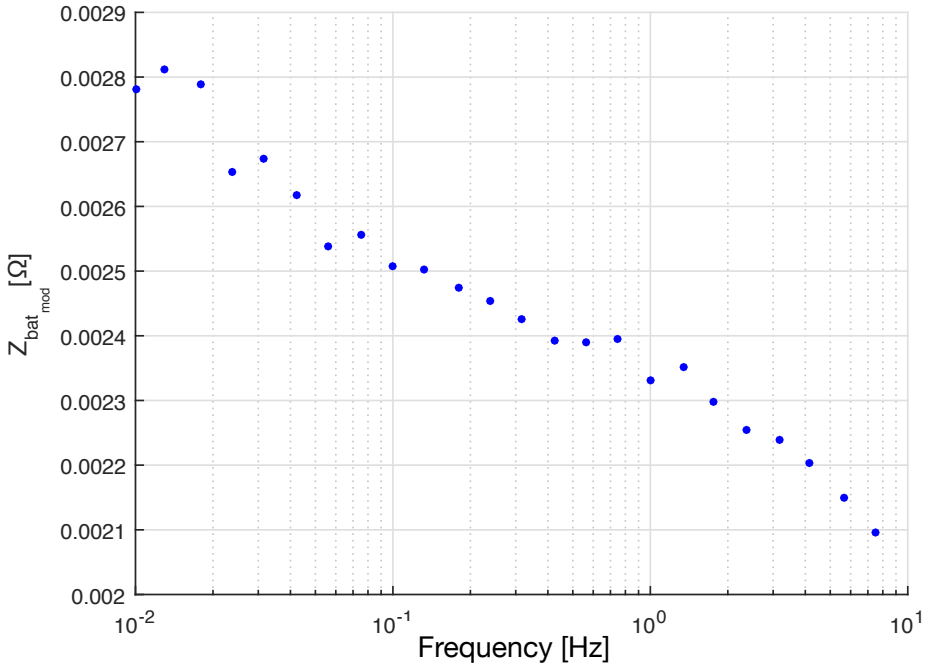



Figure 6.3: Bode plots of the impedance magnitude data assessed through the acquired voltage and current phasors for a 160 Ah battery cell with 70% SOC.

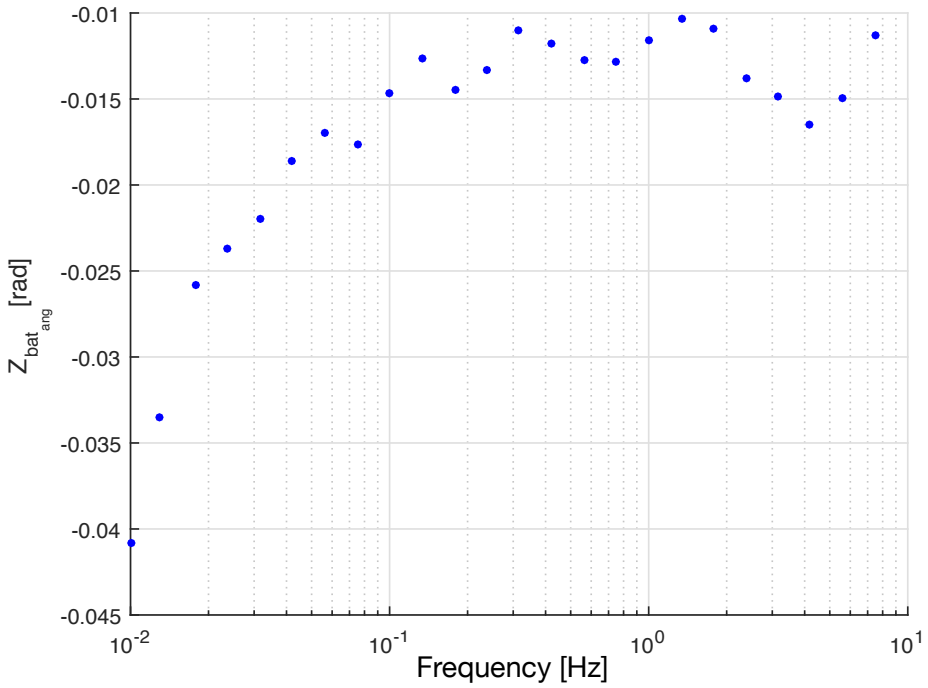



Figure 6.4: Bode plots of the impedance phase data assessed through the acquired voltage and current phasors for a 160 Ah battery cell with 70% SOC.

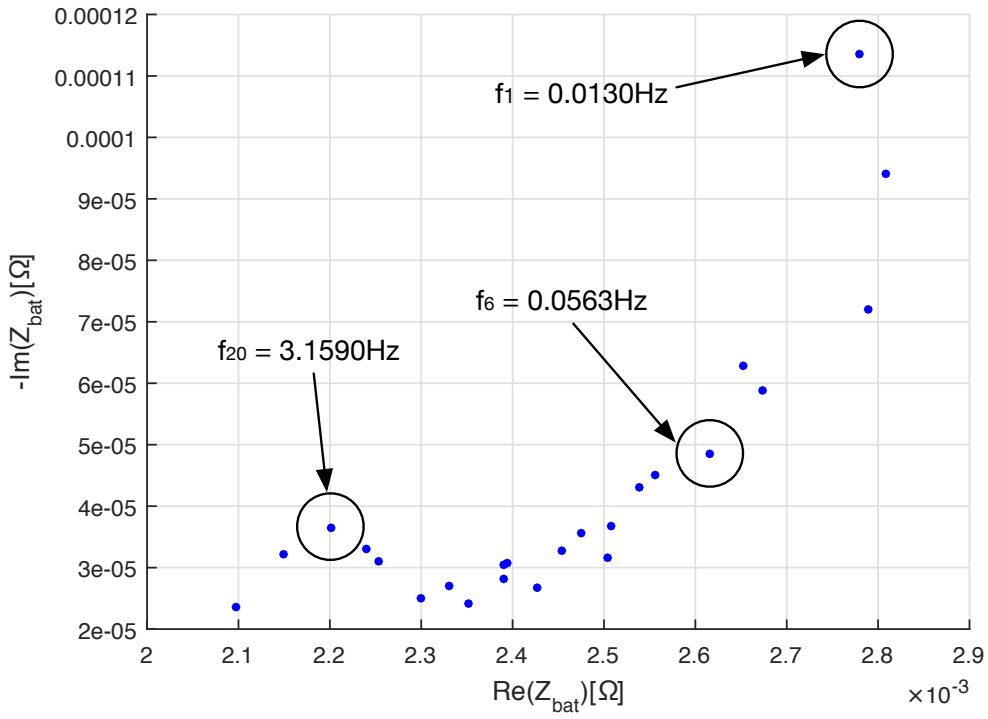



Figure 6.5: Nyquist plot of the impedance data assessed through the acquired voltage and current phasors for a 160 Ah battery cell with 70% SOC.

### 6.2.1 Impedance Spectra Database

The previous case study was presented as an example of the implemented EIS measurement system. The same process is executed to the following values of SOC during a discharge cycle so that a database to the fuzzy inference system is constructed:

| SOC(%) | 100 | 90 | 80 | 70 | 60 | 50 | 40 | 30 | 20 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|

Table 6.2: Pre-defined SOC's for which the impedance spectra database has been composed.

The obtained impedance spectra database is graphically presented in Figure 6.6 and Figure 6.7.

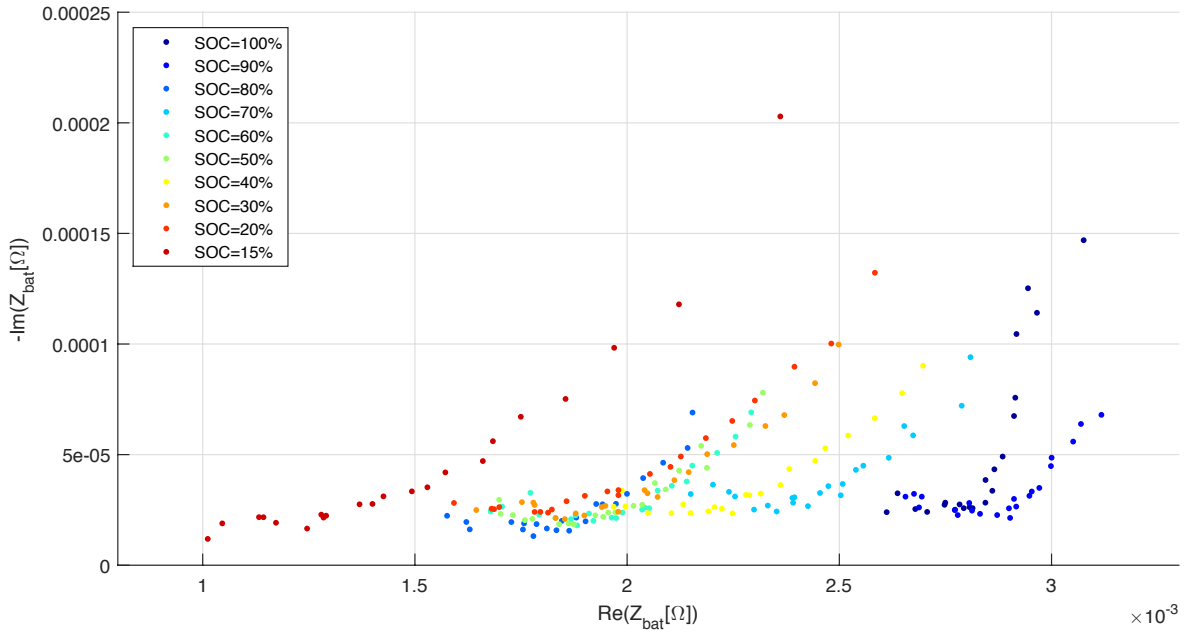



Figure 6.6: Nyquist plot of the impedance spectra database for the referred SOC's in table 6.2.

Observing the acquired impedance spectra's of the battery cell in Figure 6.6, one can say that only 20% to 30% of the referential space (-Img (Z) vs Re (Z)) is occupied by the stored data. A fuzzy system that accurately distinguishes the different SOC EIS measurements, each with 22 points, requires a certain number of rules in order to differentiate, with enough precision, the precessed data. The necessary number of rules providing an accurate system is approximately half the total number of impedance data points stored in the database. The database is composed by 10 impedance spectras, one for each SOC. Each impedance spectra contains 22 points, one for each frequency, and each of these points is defined by its real value and imaginary value. Hence, the total number of rules comes:

$$N_{rules} = \frac{N_{SOC's} \cdot N_{frequencies} \cdot N_{inputs}}{2} = \frac{10 \cdot 22 \cdot 2}{2} = 220 \tag{6.7}$$

As it was stated in chapter 4, each subset of rules (i.e. both fuzzy inputs and output) can be represented by its own membership function, thus, there are 220 gaussian membership functions for each

input (Re(Z) and -Img (Z)) and 220 output membership functions (singleton output membership functions) modelling the database.

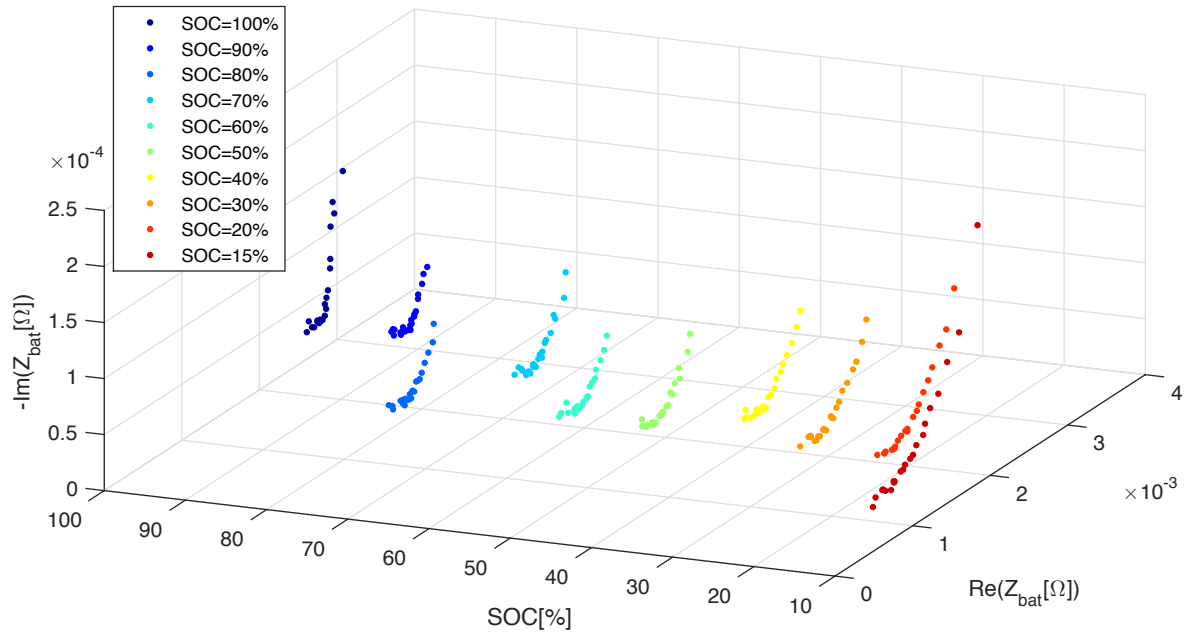



Figure 6.7: Nyquist plot of the impedance spectra database as function of the referred SOC's in table 6.2.

## 6.3 Validation of the Fuzzy Logic SOC inference system

The impedance spectra database is initially evaluated and the rule base is constructed. The fuzzy output for this pre-acquired data is plotted in Figure 6.8. The black points correspond to the estimated output of the fuzzy system, representing the inferred SOC's, whereas the blue circles represent the real SOC's of the input data, imposed to the fuzzy system, defining the respective SOC of each point introduced as training data.

After creating the database and consequent system rule base, in order to validate the fuzzy logic SOC inference system, four measurements were performed. The battery was fully recharged again, and later discharged so that the system could be tested to a SOC value of 90%, 70%, 74% and 64%. The obtained results from the EIS measurement system are presented in Figure 6.9, together with the pre-acquired database, where the impedance spectra points are marked as △ for 70%, ▽ for 90%, □ for 64% and ○ for a 74% SOC value.

The fuzzy system inferred SOC outputs for each of the four input profiles (marked by red asterisks), can be observed in Figures 6.10 (90%), 6.11 (70%), 6.12 (74%) and 6.13 (64%). The output average of the 22 estimated points is represented by a red marker (♢) in each plot.

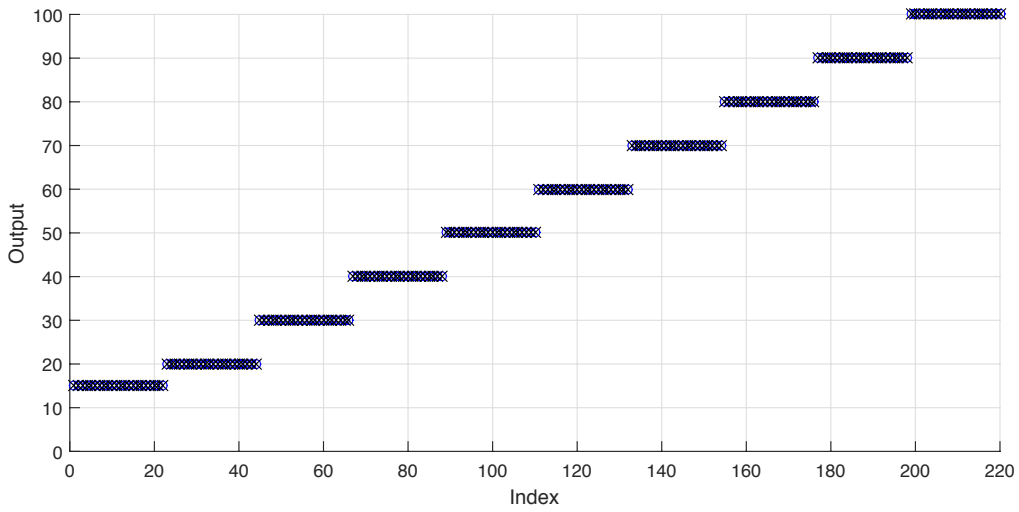



Figure 6.8: Fuzzy system output for the pre-defined SOC's. The defined output (blue dots) and the inferred output (black cyrcles).

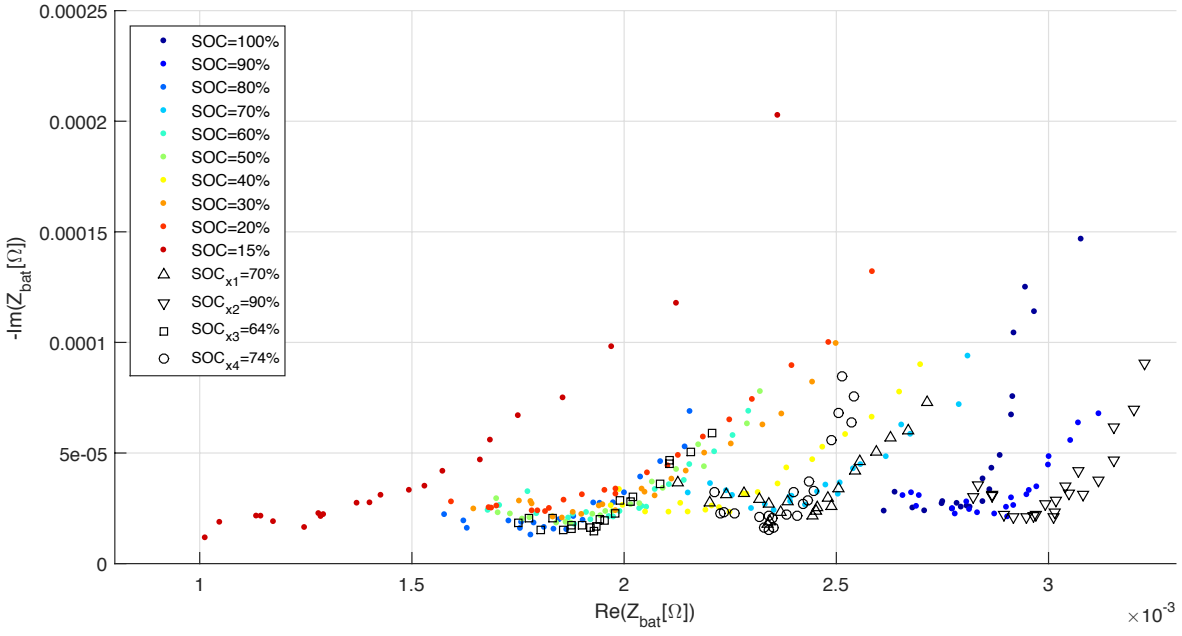



Figure 6.9: Nyquist plot of the impedance spectra database and the acquired impedance spectra for each of the presented case studies.

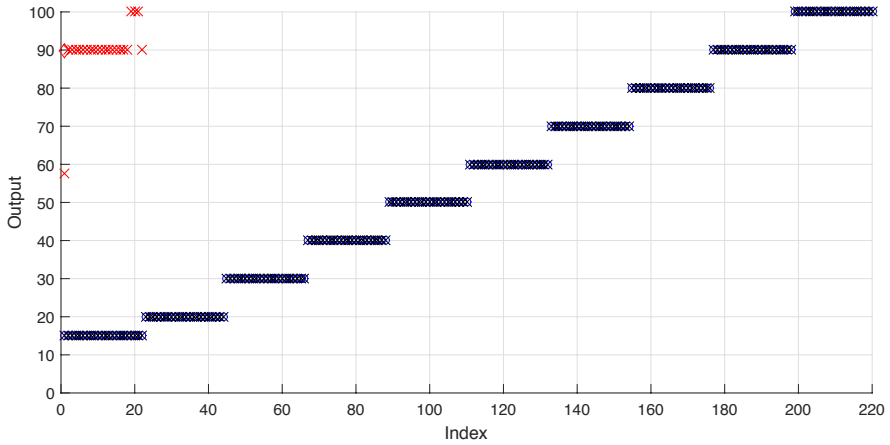



Figure 6.10: Fuzzy system output(marked by red asterisks) for the battery cell with a 90% SOC value. The output average of the inferred points is marked as ◊.

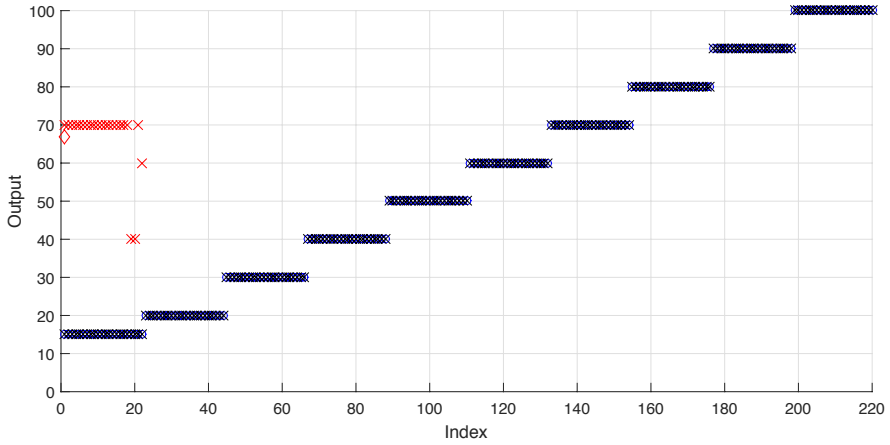



Figure 6.11: Fuzzy system output(marked by red asterisks) for the battery cell with a 70% SOC value. The output average of the inferred points is marked as ◊.

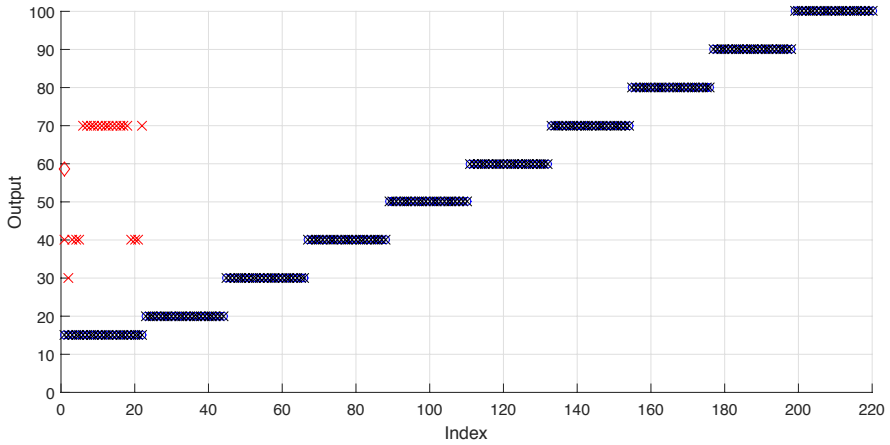



Figure 6.12: Fuzzy system output(marked by red asterisks) for the battery cell with a 74% SOC value. The output average of the inferred points is marked as ◊.

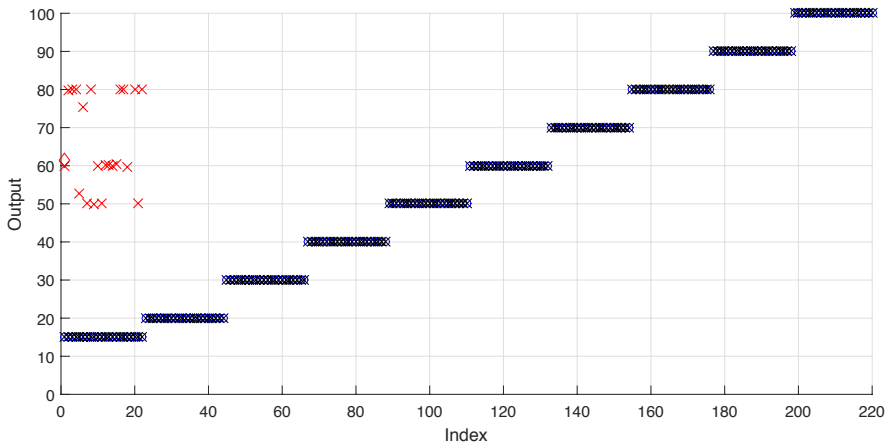



Figure 6.13: Fuzzy system output(marked by red asterisks) for the battery cell with a 64% SOC value. The output average of the inferred points is marked as ◊.

Table 6.3 displays the average and variance values of the four case studies output results. Analysing the table, it is evident that concerning input values with a SOC value not included in the modelling of the fuzzy system, in other words, for impedance spectras having a SOC value not included in the impedance spectra database, the average value of the output points is a random value and the corresponding variances are high, portraying the spread out between the inferred output points, observed in the respective plots, above presented. As for the input values with a SOC value residing in the database, the output average is close to the expected value, presenting a lower variance, thus concluding that the system is able to estimate the current SOC of the battery cell, if the measured impedance spectra has a SOC value predefined in the constructed database.

| Input | Output average | Output variance |
|---|---|---|
| Re(Z) and -Img (Z) of the cell with 90% SOC | 89.88 | 64.57 |
| Re(Z) and -Img (Z) of the cell with 70% SOC | 66.82 | 79.88 |
| Re(Z) and -Img (Z) of the cell with 74% SOC | 58.64 | 240.91 |
| Re(Z) and -Img (Z) of the cell with 64% SOC | 61.53 | 606.56 |

Table 6.3: Output average and variance of the Fuzzy system for the proposed case studies.

## 6.4 Discussion

Through the proposed case studies, one can conclude that the implemented system allows the inference of predefined SOCs, previously introduced in the constructed database. For intermediate values of predefined SOCs, the system presents an inaccuracy manifested through a high value of variance for the inferred output points, due to a mismatch between the current input and those present in the database. In order to have a more precise system, i.e., being able to correctly estimate the entire range of SOCs, a higher number of predefined SOCs are required at the moment of modelling the system, this way expanding the created database for the battery cell, used as test subject.

The database was created for the conditions presented in section 6.1, limiting the accurate SOC estimation to a fixed operating temperature and charge/discharge cycle, not taking in consideration the effects of these variables in the battery cell impedance. Although it was proven that the system is a viable SOC estimation tool, in order to get a viable built device for commercial purpose, the previous mentioned variables must be taken in account when the database is created. This means that the way the system is modelled defines the quality of the estimation method and consequent suitability of the system to different applications, depending on the application requirements. For example, for an electric vehicle application, where the battery cells are submitted to an elevated number of charge/discharge cycles and operating range temperature, the constructed database requires an wider set of information, based on the variables above mentioned.

The implemented EIS measurement system allows the measurement of low impedance $LiFePO_4$ battery cells, in a portable and compact way, this way creating a powerful tool to infer the SOC of the cell though a Fuzzy Logic inference system, proposed in this thesis, or any other of the inference methods mentioned in chapter 3, this way providing an alternative or improving the most common used SOC measuring estimation methods, the voltage measurement procedure and the coulomb counting technique. The major advantage of this method when compared to the most common ones, above mentioned, is its accuracy, depending on the database information. While these methods do not take in account the ageing and operating temperature of the cell, affecting its OCV-SOC curve and its capacity, the implemented system, if updated in regular periods of time, greatly reduces the influence of these variables, giving a more accurate value of batery cell SOC to the final user, or system, this way improving the lifetime of the cell.

# Chapter 7

# Conclusions

This chapter invokes the main conclusions that can be drawn from the performed work. In addition, it delineates some thoughts towards future work with the purpose of further develop some issues addressed throughout this thesis.

## 7.1 Achievements

This work aimed the development of a system capable of automatically measuring the SOC value of a $LiFePO_4$ battery cell. This is significantly important since $LiFePO_4$ battery cells are starting to appear as a better alternative in relation to other lithium ion batteries available on the energy storage systems market.

The developed device is capable of measuring the impedance profile of a given $LiFePO_4$ cell, performing an EIS measurement. The impedance profile assessed is afterwards used to infer its SOC value using an ANFIS based method. In order to implement this adaptive method, past impedance spectras, related to specific SOCs, constructed a database so that a valid fuzzy inference model is obtained. With this, a comparative analysis between the current cell's impedance and previous observed ones, using the considered fuzzy inference system (representing the non-linear behaviour of the internal impedance), yields the object of this thesis, the SOC value.

The device was validated for a 160 Ah $LiFePO_4$ cell, for the conditions listed in section 6.1, and the obtained results provided substantial information to access its performance. It was verified that that the way the inference system is modelled defines the accuracy of the SOC estimation method. The fuzzy inference system, modelling the cell's impedance as function of the SOC value, was obtained considering ten pre-defined SOC values: 100%; 90%; 80%; 70%; 60%; 50%; 40%; 30%; 20%; 15%. It was demonstrated that the developed device is capable of estimating future SOC values for inferred values matching those present in the database. For intermediate values it was concluded that the inferred results average was a random value and its corresponding variances were quite high due to large variations between impedance spectras, as expected, justified by the non-linear behaviour of the $LiFePO_4$ cell's impedance in relation to SOC. With this in mind, for this device to properly work for the

entire range of SOC values, including the intermediate ones, it is necessary to increase the number of acquired impedance spectras modelling the fuzzy inference system, i.e., increasing the number of pre-defined SOC values composing the database.

The conditions listed in section 6.1 concern a fixed operating temperature, only one charge/discharge cycle for the cell and a resting time of 10 minutes. Outside these conditions, the inferred SOC value is uncertain, seeing that the effects of each one of these variables in the cell's impedance were not taken in account in the course of this work.

In conclusion, it was proven that the device is capable of automatically estimate the SOC value of a $LiFePO_4$ battery cell, for a case study under certain conditions. The results may be further improved in the future, as described in the next section.

## 7.2 Future Work

Some further improvements may be attended in the future:

- The construction of an impedance spectra database considering a greater number of pre-defined SOC values while taking in account some variables affecting the internal impedance of a $LiFePO_4$ cell. The following variables may be considered: Operating temperature; Relaxation time after interrupting the current flow; Number of charge/discharge cycles; Charging/Discharging current rate.
- Introducing more input variables to the proposed ANFIS based method, such as the battery cell OCV.
- The development of an interpolating methodology in order to infer the intermediate impedance spectras already present in the database.
- The conjunction of the developed device with other SOC estimation methods, such as the indirect ones, described in section 3.1.2.

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# Appendix A

# Circuit Design

## A.1 PCB Components

PCB components

| Band-Pass Filter | Howland Current Source | Others |
|---|---|---|
| $R_1 = 47.4$ kΩ | $R_1 = 1\ \Omega$ | LTSR 6-NP Current transducer |
| $R_2 = 240$ kΩ | 2× $R_2 = 10$ kΩ | 2× LM323T Voltage regulator |
| $R_3 = 35.7$ kΩ | 2× $R_3 = 10$ kΩ | $C = 10\ \mu$F |
| $R_4 = 86.6$ kΩ | OPA548 Operational amplifier | $C = 1\ \mu$F |
| $R_5 = 1.74$ MΩ | SK129 Heatsink | 2× AD7680 ADC Converters |
| $R_6 = 1.47$ MΩ | $R_{lim} = 22$ kΩ | 6-leg toggle switch |
| $R_7 = 4.53M$ kΩ | $R_9 = 1$ MΩ | LED Basic red |
| $R_8 = 619.4$ kΩ | | |
| $C_1 = 100$ pF | | |
| $C_2 = 220$ pF | | |
| $C_3 = 100$ pF | | |
| $C_4 = 820$ pF | | |
| $C_5 = 10\ \mu$F | | |
| $C_6 = 10\ \mu$F | | |
| 4× $\mu$A741 Operational amplifier | | |

Table A.1: Components for the developed printed circuit board.

## A.2 Circuit PCB

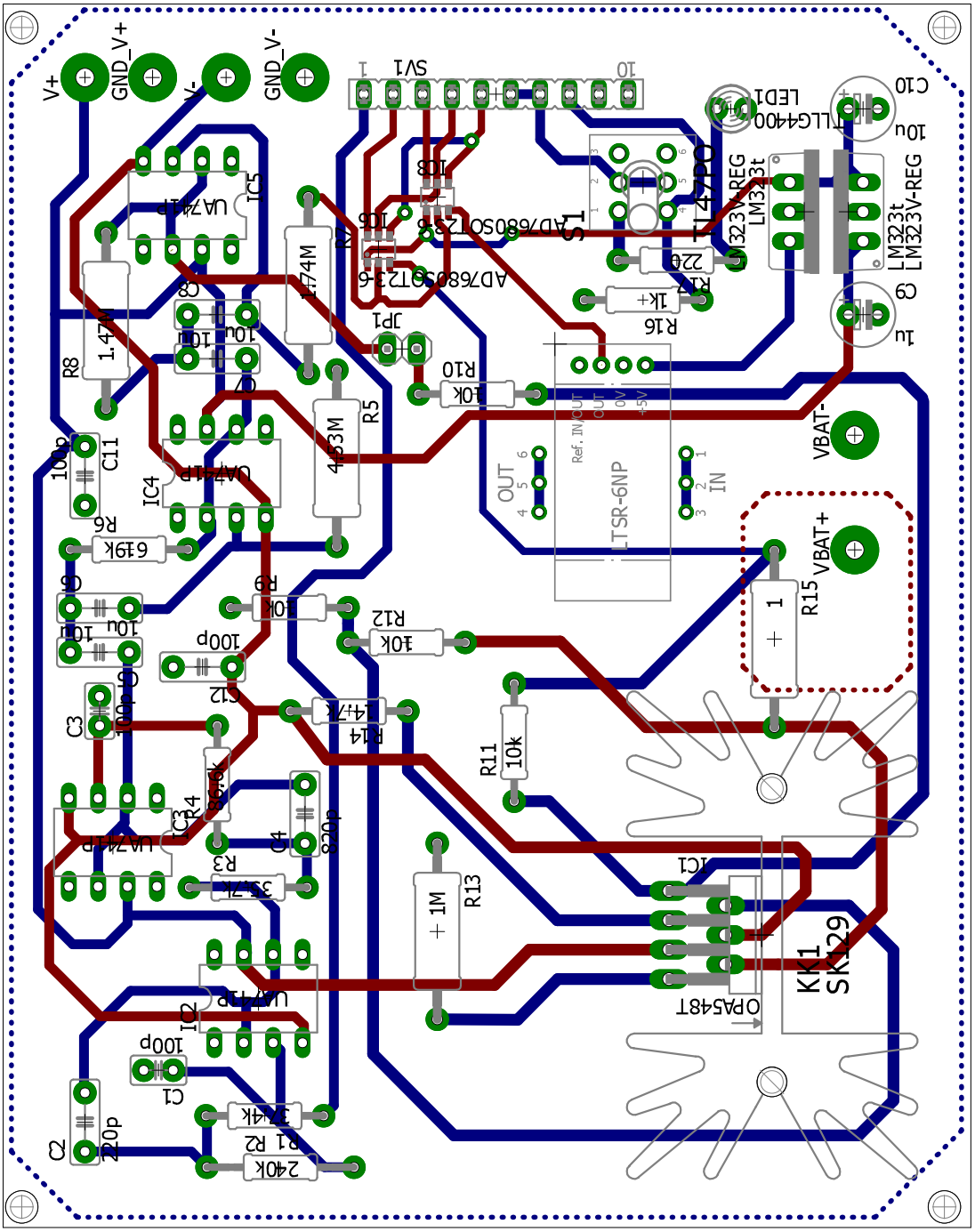



Figure A.1: PCB Board.

## A.3 Circuit Schematic

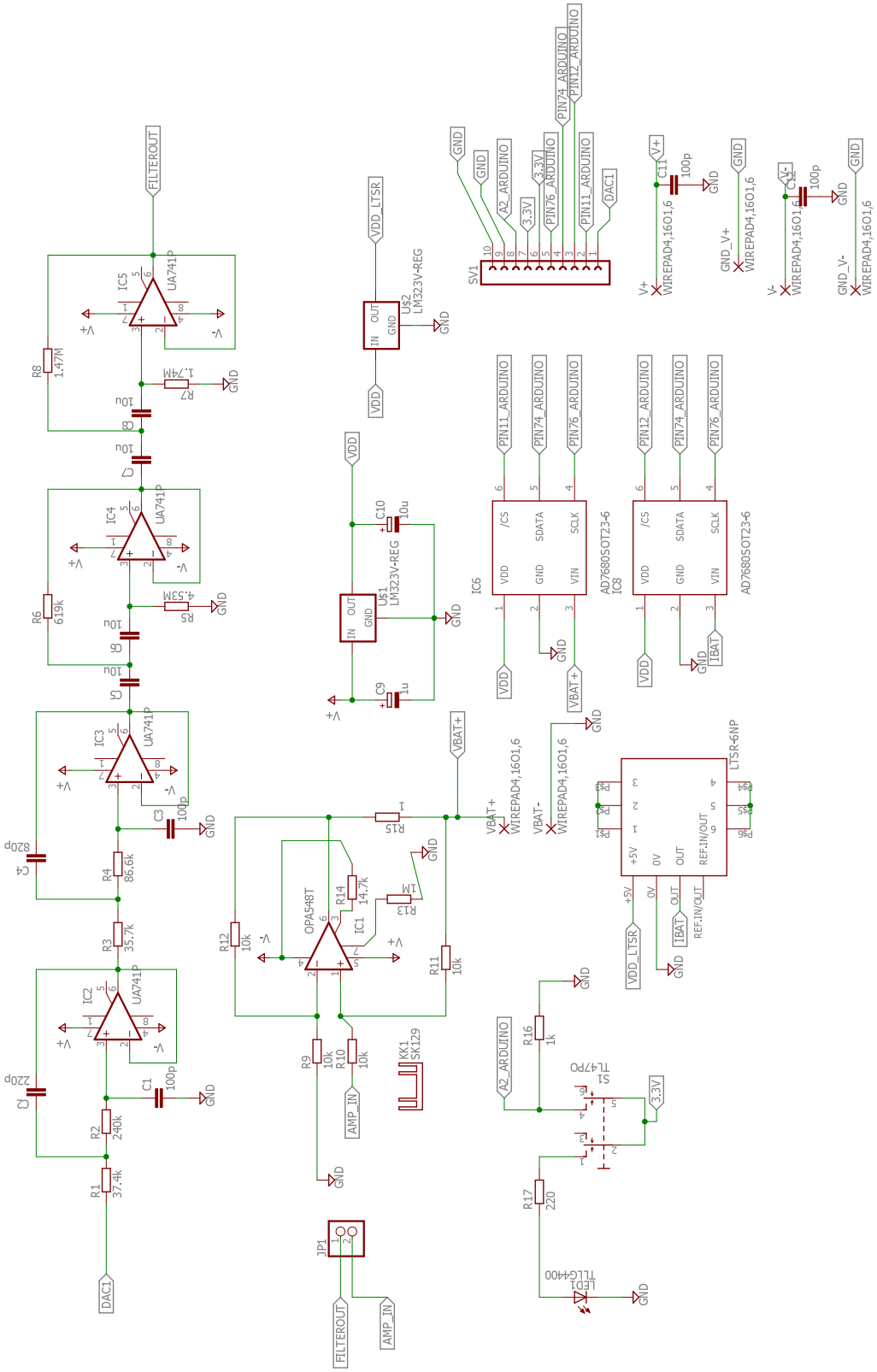



Figure A.2: Circuit Schematic.

# Appendix B

# Routines

## B.1 Variable Frequency Voltage Source routine

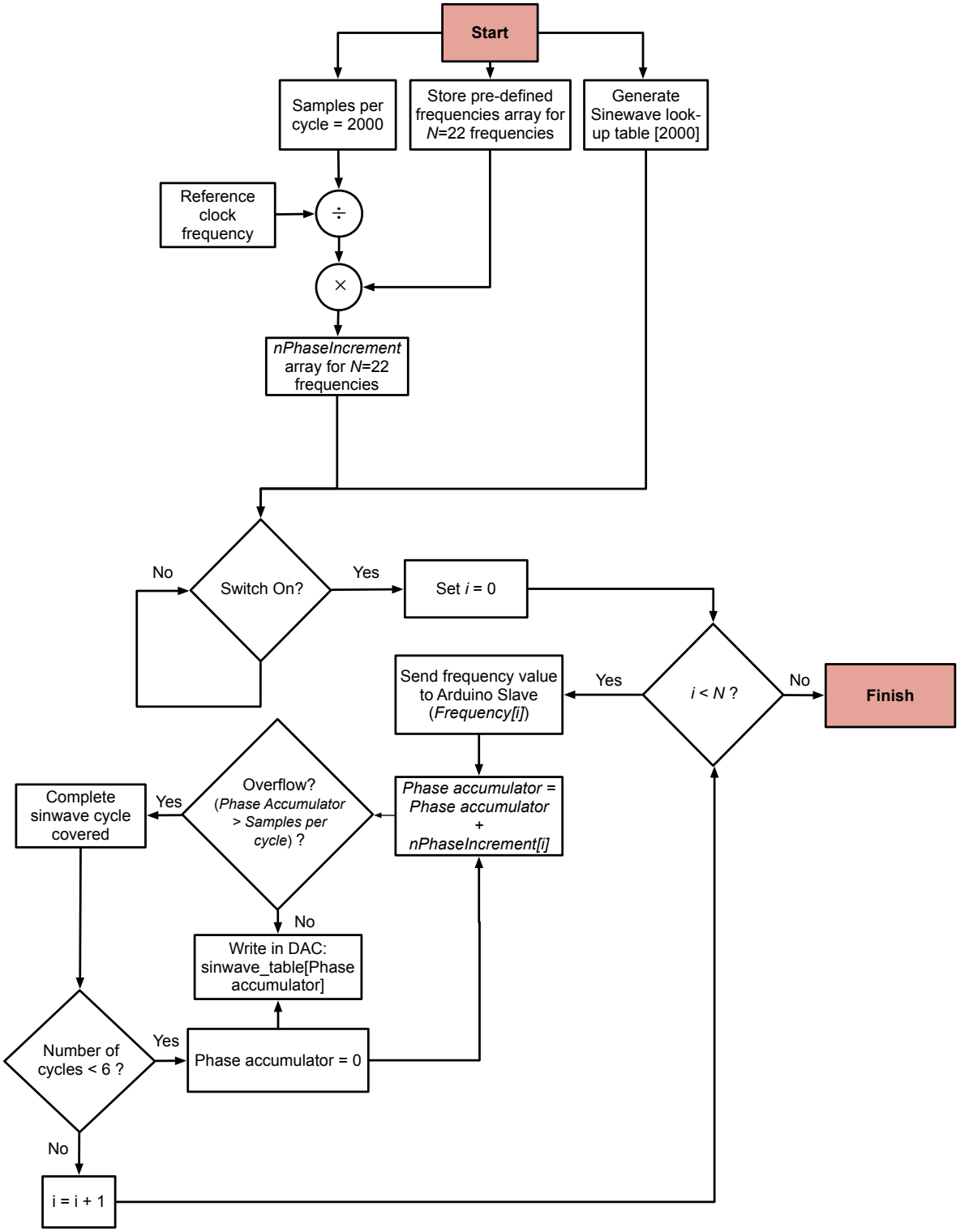



Figure B.1: Variable frequency voltage source routine.

## B.2 Oversampling with Averaging and Moving Average Digital Filter routines

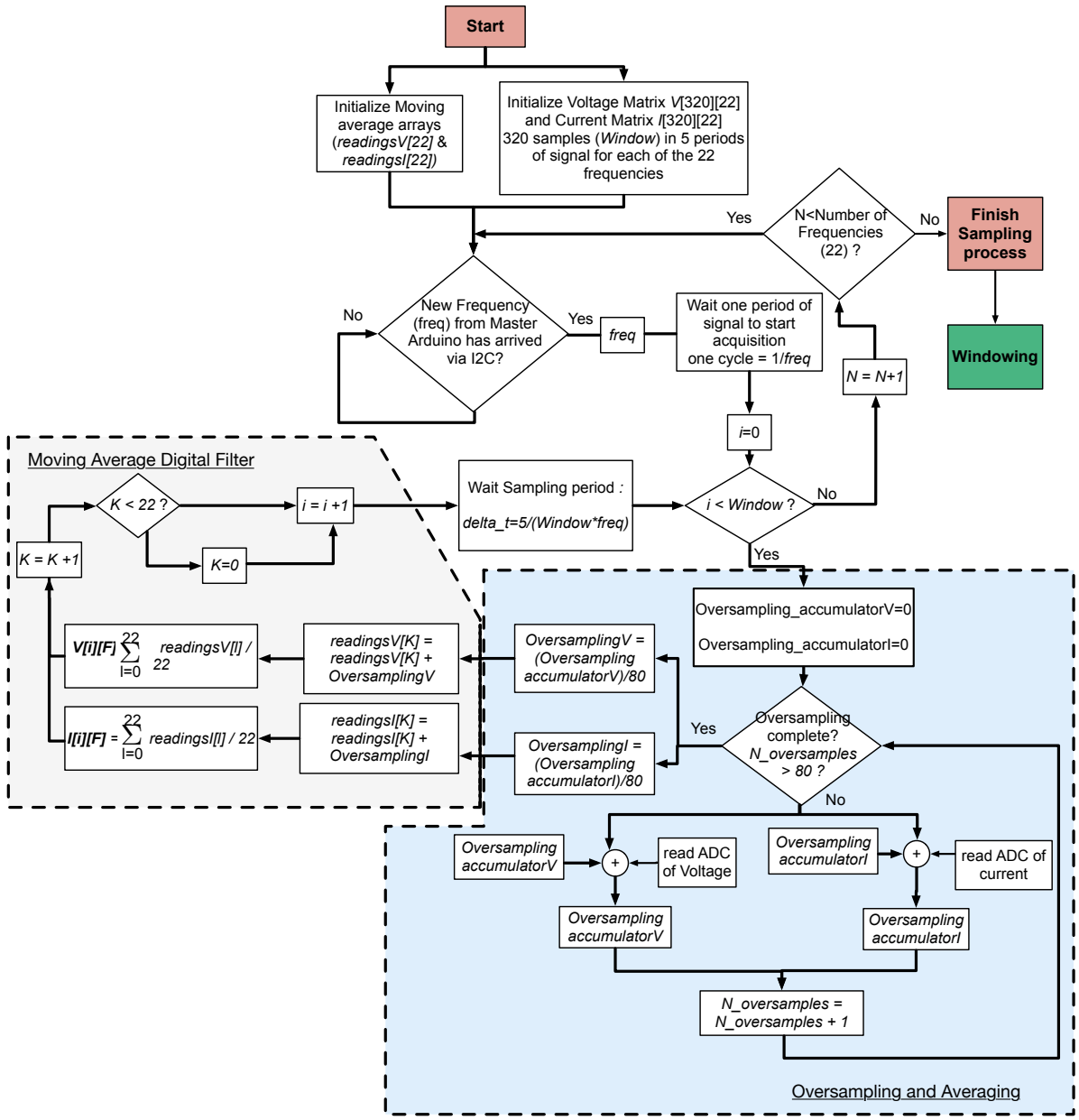



Figure B.2: Oversampling and averaging and Moving average digital filter routines.

## B.3 Windowing routine

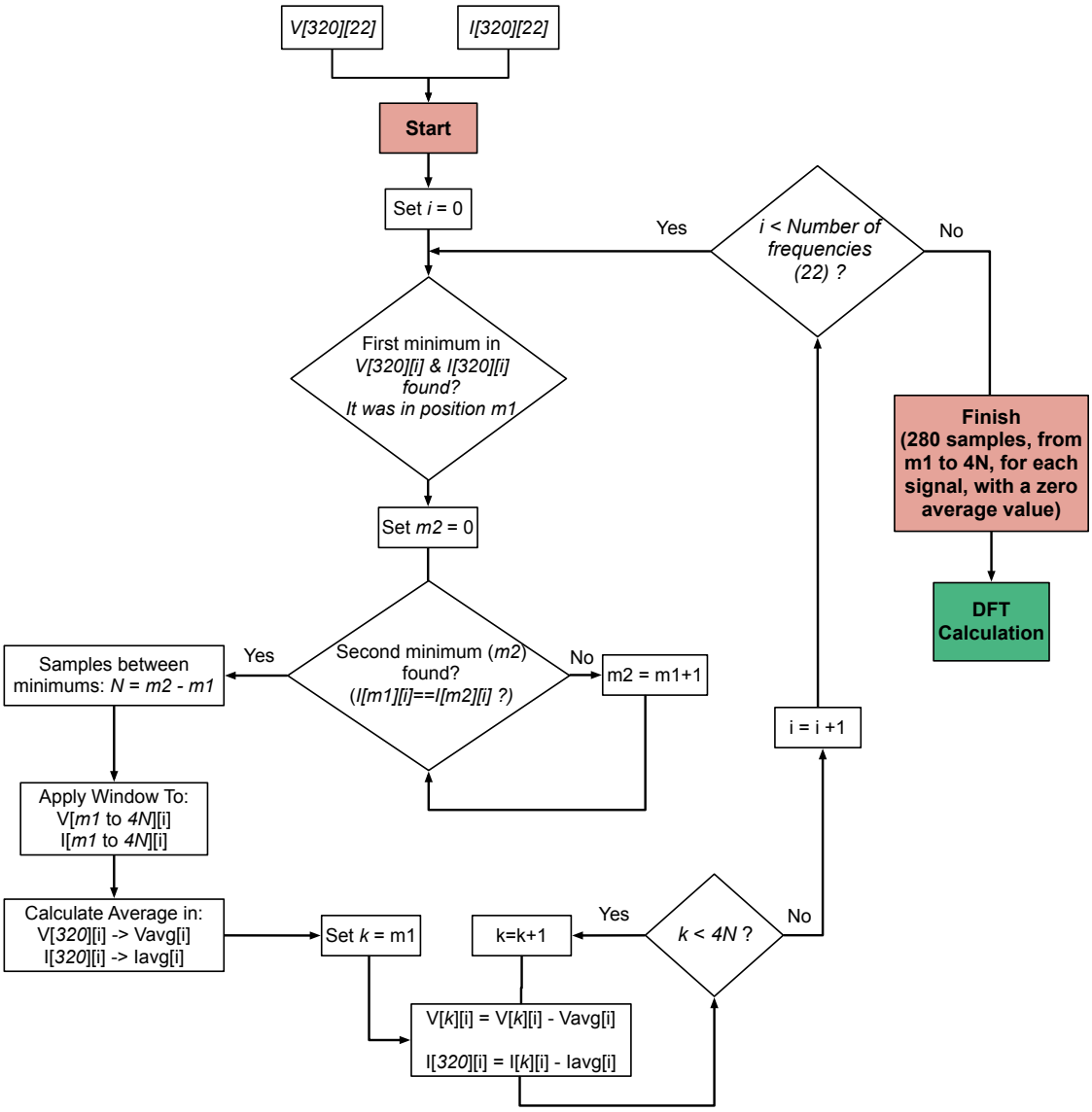



Figure B.3: Windowing routine.

## B.4 Discrete Fourier Transform (DFT) routine

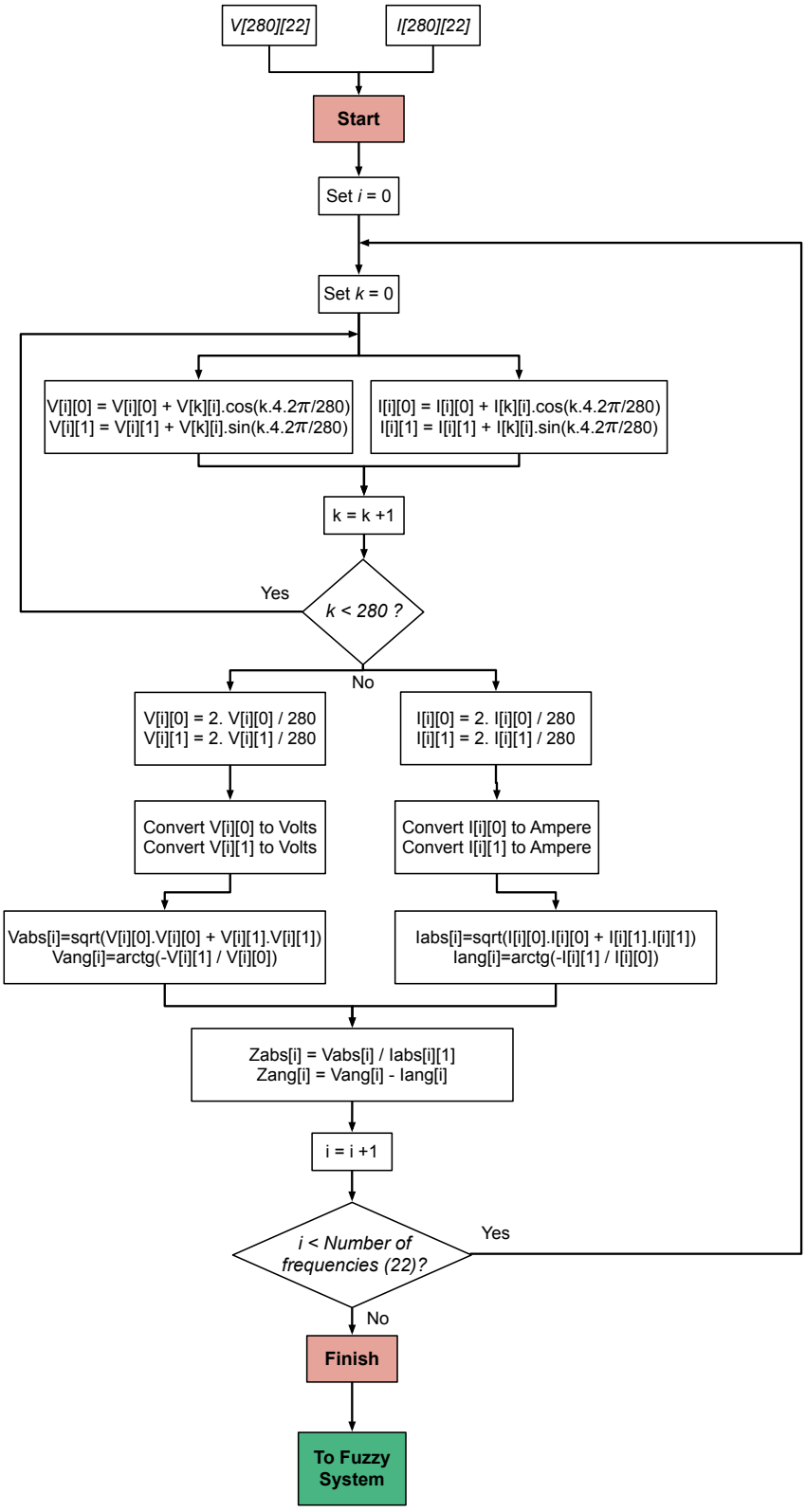



Figure B.4: Discrete Fourier Transform (DFT) routine.

# Appendix C

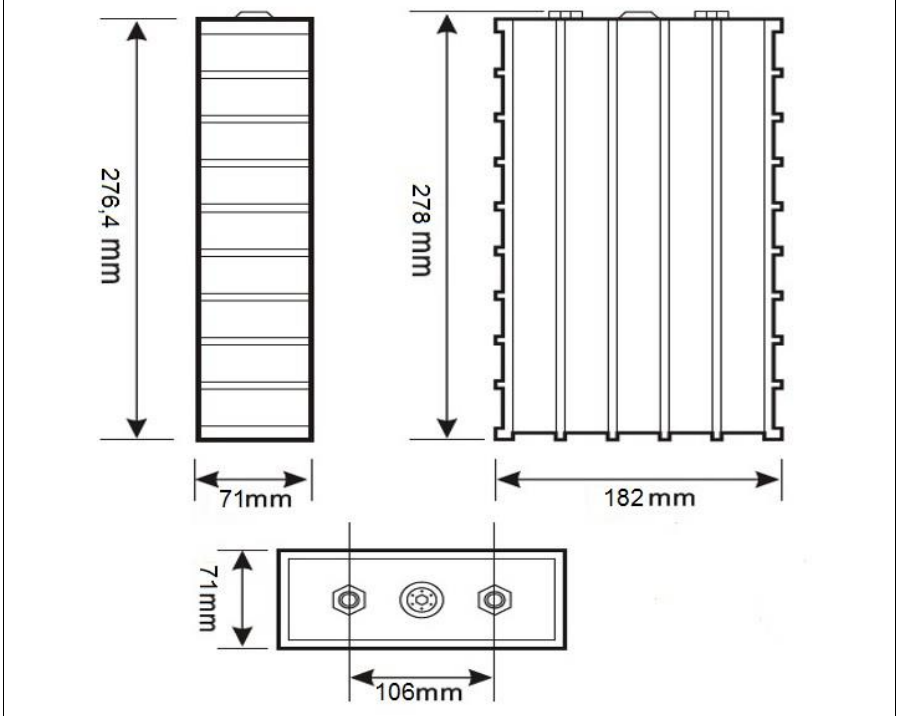
# Technical Datasheets

## C.1 $LiFePO_4$ cell

GWL/ Power Group Technology Solutions - Stay Powered for the Future

**LFP160AHA TALL cell specification**

| | | |
|---|---|---|
| Model name | LFP160AHA TALL | Alternative product mark TS-LFP160AHA, WB-LYP160AHA(A) |
| Nominal voltage | 3.2 V | Operating voltage under load is 3.0 V |
| Capacity | 160 AH | +/- 5% |
| Operating voltage | max 4.0V - min 2.8V | At 80% DOD |
| Deep discharge voltage | 2.5 V | The cells is damaged if voltage drops bellow this level |
| Maximal charge voltage | 4 V | The cells is damaged if voltage exceeds this level |
| Optimal discharge current | < 80 A | 0.5 C |
| Maximal discharge current | < 480 A | 3 C, continuous for max 15 minutes from full charge |
| Max peak discharge current | < 1600 A | 10 C, maximal 5 seconds in 1 minute |
| Optimal charge current | < 80 A | 0.5 C |
| Maximal charge current | < 480 A | < 3 C with battery temperature monitoring |
| Maximal continuous operating temperature | 80 °C | The battery temperature should not increase this level during charge and discharge |
| Dimensions | 182 X 278 X 71 | Millimeters (tolerance +/- 2 mm) |
| Weight | 5.8 kg | Kilograms (tolerance +/- 150g) |




http://www.ev-power.eu/

# C.2 uA741 Operational Amplifier





## µA741 General-Purpose Operational Amplifiers

### 1 Features

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

### 2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

### 3 Description

The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

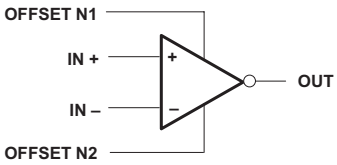
The µA741C device is characterized for operation from 0°C to 70°C. The µA741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

**Device Information(1)**

| PART NUMBER | PACKAGE (PIN) | BODY SIZE (NOM) |
|---|---|---|
| µA741x | SOIC (8) | 4.90 mm × 3.91 mm |
| | PDIP (8) | 9.81 mm × 6.35 mm |
| | SO (8) | 6.20 mm × 5.30 mm |

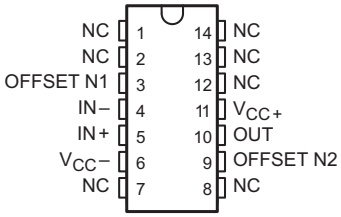
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic

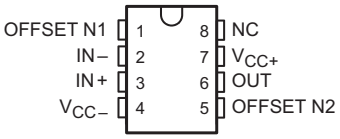


## 6 Pin Configurations and Functions

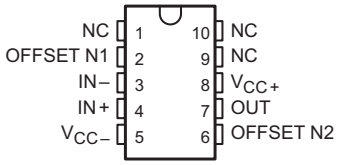
**µA741M . . . J PACKAGE**
**(TOP VIEW)**



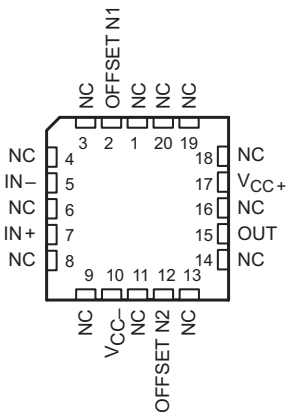

**µA741M . . . JG PACKAGE**
**µA741C, µA741I . . . D, P, OR PW PACKAGE**
**(TOP VIEW)**




**µA741M . . . U PACKAGE**
**(TOP VIEW)**




**µA741M . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**Pin Functions**

| NAME | PIN | | | | TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|
| | J | JG, D, P, or PW | U | FK | | |
| IN+ | 5 | 3 | 4 | 7 | I | Noninverting input |
| IN– | 4 | 2 | 3 | 5 | I | Inverting input |
| NC | 1, 2, 8, 12, 13, 14 | 8 | 1, 9, 10 | 1,3,4,6,8,9,11,13,14,16,18,19,20 | — | Do not connect |
| OFFSET N1 | 3 | 1 | 2 | 2 | I | External input offset voltage adjustment |
| OFFSET N2 | 9 | 5 | 6 | 12 | I | External input offset voltage adjustment |
| OUT | 10 | 6 | 7 | 15 | O | Output |
| $V_{CC}$+ | 11 | 7 | 8 | 17 | — | Positive supply |
| $V_{CC}$– | 6 | 4 | 5 | 10 | — | Negative supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

| | | | μA741C | | μA741M | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage(2) | | –18 | 18 | –22 | 22 | C |
| $V_{ID}$ | Differential input voltage(3) | | –15 | 15 | –30 | 30 | V |
| $V_I$ | Input voltage, any input(2)(4) | | –15 | 15 | –15 | 15 | V |
| | Voltage between offset null (either OFFSET N1 or OFFSET N2) and $V_{CC-}$ | | –15 | 15 | –0.5 | 0.5 | V |
| | Duration of output short circuit(5) | | Unlimited | | | | |
| | Continuous total power dissipation | | See Table 1 | | | | |
| $T_A$ | Operating free-air temperature range | | 0 | 70 | –55 | 125 | °C |
| | Case temperature for 60 seconds | FK package | N/A | N/A | | 260 | °C |
| | Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds | J, JG, or U package | N/A | N/A | | 300 | °C |
| | Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | D, P, or PS package | | 260 | N/A | N/A | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between $V_{CC+}$ and $V_{CC-}$.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or either power supply. For the μA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

## 7.2 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC+}$ | Supply voltage | | 5 | 15 | V |
| $V_{CC-}$ | | | –5 | –15 | |
| $T_A$ | Operating free-air temperature | μA741C | 0 | 70 | °C |
| | | μA741M | –55 | 125 | |

**Table 1. Dissipation Ratings Table**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR | DERATE ABOVE $T_A$ | TA = 70°C POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|---|
| D | 500 mW | 5.8 mW/°C | 64°C | 464 mW | 377 mW | N/A |
| FK | 500 mW | 11.0 mW/°C | 105°C | 500 mW | 500 mW | 275 mW |
| J | 500 mW | 11.0 mW/°C | 105°C | 500 mW | 500 mW | 275 mW |
| JG | 500 mW | 8.4 mW/°C | 90°C | 500 mW | 500 mW | 210 mW |
| P | 500 mW | N/A | N/A | 500 mW | 500 mW | N/A |
| PS | 525 mW | 4.2 mW/°C | 25°C | 336 mW | N/A | N/A |
| U | 500 mW | 5.4 mW/°C | 57°C | 432 mW | 351 mW | 135 mW |

## 7.3 Electrical Characteristics µA741C, µA741M

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ (1) | µA741C | | | µA741M | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 0 | 25°C | | 1 | 6 | | 1 | 5 | mV |
| | | | Full range | | | 7.5 | | ±15 | 6 | |
| $\Delta V_{IO(adj)}$ | Offset voltage adjust range | $V_O$ = 0 | 25°C | | ±15 | | | 20 | 200 | mV |
| $I_{IO}$ | Input offset current | $V_O$ = 0 | 25°C | | 20 | 200 | | | 500 | nA |
| | | | Full range | | | 300 | | | 500 | |
| $I_{IB}$ | Input bias current | $V_O$ = 0 | 25°C | | 80 | 500 | | 80 | 500 | nA |
| | | | Full range | | | 800 | | | 1500 | |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | ±12 | ±13 | | ±12 | ±13 | | V |
| | | | Full range | ±12 | | | ±12 | | | |
| $V_{OM}$ | Maximum peak output voltage swing | $R_L$ = 10 kΩ | 25°C | ±12 | ±14 | | ±12 | ±14 | | V |
| | | $R_L$ ≥ 10 kΩ | Full range | ±12 | | | ±12 | | | |
| | | $R_L$ = 2 kΩ | 25°C | ±10 | | | ±10 | ±13 | | |
| | | $R_L$ ≥ 2kΩ | Full range | ±10 | | | ±10 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_L$ ≥ 2kΩ | 25°C | 20 | 200 | | 50 | 200 | | V/mV |
| | | $V_O$ = ±10 V | Full range | 15 | | | 25 | | | |
| $r_i$ | Input resistance | | 25°C | 0.3 | 2 | | 0.3 | 2 | | MΩ |
| $r_o$ | Output resistance | $V_O$ = 0, See (2) | 25°C | | 75 | | | 75 | | Ω |
| $C_i$ | Input capacitance | | 25°C | | 1.4 | | | 1.4 | | pF |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICRmin}$ | 25°C | 70 | 90 | | 70 | 90 | | dB |
| | | | Full range | 70 | | | 70 | | | |
| $k_{SVS}$ | Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) | $V_{CC}$ = ±9 V to ±15 V | 25°C | | 30 | 150 | | 30 | 150 | µV/V |
| | | | Full range | | | 150 | | | 150 | |
| $I_{OS}$ | Short-circuit output current | | 25°C | | ±25 | ±40 | | ±25 | ±40 | mA |
| $I_{CC}$ | Supply current | $V_O$ = 0, No load | 25°C | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| | | | Full range | | | 3.3 | | | 3.3 | |
| $P_D$ | Total power dissipation | $V_O$ = 0, No load | 25°C | | 50 | 85 | | 50 | 85 | mW |
| | | | Full range | | | 100 | | | 100 | |

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C and the µA741M is –55°C to 125°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

## 7.4 Electrical Characteristics µA741Y

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V, $T_A$ = 25°C (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | µA741Y | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 0 | | 1 | 5 | mV |
| $\Delta V_{IO(adj)}$ | Offset voltage adjust range | $V_O$ = 0 | | ±15 | | mV |
| $I_{IO}$ | Input offset current | $V_O$ = 0 | | 20 | 200 | nA |
| $I_{IB}$ | Input bias current | $V_O$ = 0 | | 80 | 500 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | ±12 | ±13 | | V |
| $V_{OM}$ | Maximum peak output voltage swing | $R_L$ = 10 kΩ | ±12 | ±14 | | V |
| | | $R_L$ = 2 kΩ | ±10 | ±13 | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_L$ ≥ 2kΩ | 20 | 200 | | V/mV |
| $r_i$ | Input resistance | | 0.3 | 2 | | MΩ |
| $r_o$ | Output resistance | $V_O$ = 0, See(1) | | 75 | | Ω |
| $C_i$ | Input capacitance | | | 1.4 | | pF |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICRmin}$ | 70 | 90 | | dB |
| $k_{SVS}$ | Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) | $V_{CC}$ = ±9 V to ±15 V | | 30 | 150 | µV/V |
| $I_{OS}$ | Short-circuit output current | | | ±25 | ±40 | mA |
| $I_{CC}$ | Supply current | $V_O$ = 0, No load | | 1.7 | 2.8 | mA |
| $P_D$ | Total power dissipation | $V_O$ = 0, No load | | 50 | 85 | mW |

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

## 7.5 Switching Characteristics µA741C, µA741M

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | µA741C | | | µA741M | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_r$ | Rise time | $V_I$ = 20 mV, $R_L$ = 2 kΩ, $C_L$ = 100 pF, See Figure 1 | | 0.3 | | | 0.3 | | µs |
| | Overshoot factor | | | 5% | | | 5% | | — |
| SR | Slew rate at unity gain | $V_I$ = 10 V, $R_L$ = 2 kΩ, $C_L$ = 100 pF, See Figure 1 | | 0.5 | | | 0.5 | | V/µs |

## 7.6 Switching Characteristics µA741Y

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | µA741Y | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $t_r$ | Rise time | $V_I$ = 20 mV, $R_L$ = 2 kΩ, $C_L$ = 100 pF, See Figure 1 | | 0.3 | | µs |
| | Overshoot factor | | | 5% | | — |
| SR | Slew rate at unity gain | $V_I$ = 10 V, $R_L$ = 2 kΩ, $C_L$ = 100 pF, See Figure 1 | | 0.5 | | V/µs |

# C.3 LEM LTSR 6-NP

## Current Transducer LTSR 6-NP

$I_{PN}$ = 6 At

For the electronic measurement of currents: DC, AC, pulsed, mixed, with galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

16073

### Electrical data

| | | | | |
|---|---|---|---|---|
| $I_{PN}$ | Primary nominal current rms | | 6 | At |
| $I_{PM}$ | Primary current, measuring range | | 0 .. ± 19.2 [1] | At |
| $\hat{I}_P$ | Overload capability | | 250 | At |
| $V_{OUT}$ | Output voltage (Analog) @ $I_P$ | | 2.5 ± (0.625·$I_P$/$I_{PN}$) | V |
| | | $I_P$ = 0 | 2.5 [2] | V |
| $V_{REF}$ | Reference voltage (internal reference), $Ref_{OUT}$ mode | | 2.5 [3] | V |
| | Reference voltage (external reference), $Ref_{IN}$ mode | | 1.9 .. 2.7 [4] | V |
| G | Sensitivity | | 104.16 | mV/A |
| $N_S$ | Number of secondary turns (± 0.1 %) | | 2000 | |
| $R_L$ | Load resistance | | ≥ 2 | kΩ |
| $C_{L\,max}$ | Maximum capacitive loading | | 500 | pF |
| $R_{IM}$ | Internal measuring resistance (± 0.5 %) | | 208.33 | Ω |
| $TCR_{IM}$ | Temperature coefficient of $R_{IM}$ | | < 50 | ppm/K |
| $V_C$ | Supply voltage (± 5 %) | | 5 | V |
| $I_C$ | Current consumption @ $V_C$ = 5 V | Typ | 28+$I_S$ [5]+($V_{OUT}$/$R_L$) | mA |

### Accuracy - Dynamic performance data

| | | | | |
|---|---|---|---|---|
| X | Accuracy @ $I_{PN}$, $T_A$ = 25°C | | ± 0.2 | % |
| | Accuracy with $R_{IM}$ @ $I_{PN}$, $T_A$ = 25°C | | ± 0.7 | % |
| $\varepsilon_L$ | Linearity error | | < 0.1 | % |
| | | | Max | |
| $TCV_{OUT}$ | Temperature coefficient of $V_{OUT}$/$V_{REF}$ @ $I_P$ = 0 | | | |
| | | - 40°C .. + 85°C | 150 | ppm/K |
| TCG | Temperature coefficient of G | - 40°C .. + 85°C | 50 [6] | ppm/K |
| $V_{OM}$ | Magnetic offset voltage @ $I_P$ = 0, | | | |
| | after an overload of | 3 x $I_{PN}$ | ± 7 | mV |
| | | 5 x $I_{PN}$ | ± 8 | mV |
| | | 10 x $I_{PN}$ | ± 10 | mV |
| $TCV_{REF}$ | Temperature coefficient of internal $V_{REF}$ | | | |
| | @ $I_P$ = 0 | - 10°C .. + 85°C | 50 | ppm/K |
| | | - 40°C .. - 10°C | 100 | ppm/K |
| $t_{ra}$ | Reaction time @ 10 % of $I_{PN}$ | | < 100 | ns |
| $t_r$ | Response time to 90 % of $I_{PN}$ step | | < 400 | ns |
| di/dt | di/dt accurately followed | | > 15 | A/µs |
| BW | Frequency bandwidth (0 .. - 0.5 dB) | | DC .. 100 | kHz |
| | (- 0.5 .. 1 dB) | | DC .. 200 | kHz |

Notes: [1] Only in $ref_{OUT}$ mode or with external REF less than 2.525 V and greater than 2.475 V. For external REF out of these limits see leaflet. [2] $V_{OUT}$ is linked to $V_{REF}$, by conception the difference between these two nodes for $I_P$ = 0 is maximum ± 25 mV, 2.475 V < $V_{OUT}$ < 2.525 V. [3] In $Ref_{OUT}$ mode at $T_A$ = 25°C, 2.475 V< $V_{REF}$ < 2.525 V. The minimal impedance loading the ref pin should be > 220 kΩ. Internal impedance = 600 Ω. For most applications you need to buffer this output to feed it into an ADC for example. [4] To overdrive the REF (1.9 V .. 2.7 V) max ± 1 mA is needed. [5] $I_S$ = $I_P$/$N_S$. [6] Only due to TCR IM.

### Features

- Closed loop (compensated) multirange current transducer using the Hall effect
- Unipolar voltage supply
- Isolated plastic case recognized according to UL 94-V0
- Compact design for PCB mounting
- Incorporated measuring resistance
- Extended measuring range
- Access to the internal voltage reference
- Possibility to feed the transducer reference from external supply.

### Advantages

- Excellent accuracy
- Very good linearity
- Very low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

### Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

### Application Domain

- Industrial.

## Current Transducer LTSR 6-NP

## General data

| | | | |
|---|---|---|---|
| $T_A$ | Ambient operating temperature | - 40 .. + 85 | °C |
| $T_S$ | Ambient storage temperature | - 40 .. + 100 | °C |
| | Insulating material group | III a | |
| ***m*** | Mass | 10 | g |
| | Standards [1] | EN 50178: 1997<br>IEC 60950-1: 2001 | |

## Isolation characteristic

| | | | |
|---|---|---|---|
| $V_d$ | Rms voltage for AC isolation test, 50 Hz, 1 min | 3 | kV |
| $\hat{V}_w$ | Impulse withstand voltage 1.2/50 µs | > 8<br>Min | kV |
| $V_e$ | Rms voltage for partial discharge extinction 10 pC | > 1.5<br>Min | kV |
| dCp | Creepage distance [2] | 15.35 | mm |
| dCl | Clearance distance [3] | 6.2 | mm |
| CTI | Comparative Tracking Index (group IIIa) | 175 | |

### Applications examples

**According to EN 50178 and CEI 61010-1 standards** and following conditions:

- Over voltage category OV 3
- Pollution degree PD2
- Non-uniform field

| | EN 50178 | EIC 61010-1 |
|---|---|---|
| dCp, dCl, $\hat{V}_w$ | Rated insulation voltage | Nominal voltage |
| Single insulation | 600 V | 600 V |
| Reinforced insulation | 300 V | 300 V |

Notes: [1] Specification according to IEC 1000-4-8 not adhered to in DC, error according to two axes 1.5% instead of 1%
[2] On housing
[3] On PCB with soldering pattern UTEC93-703.

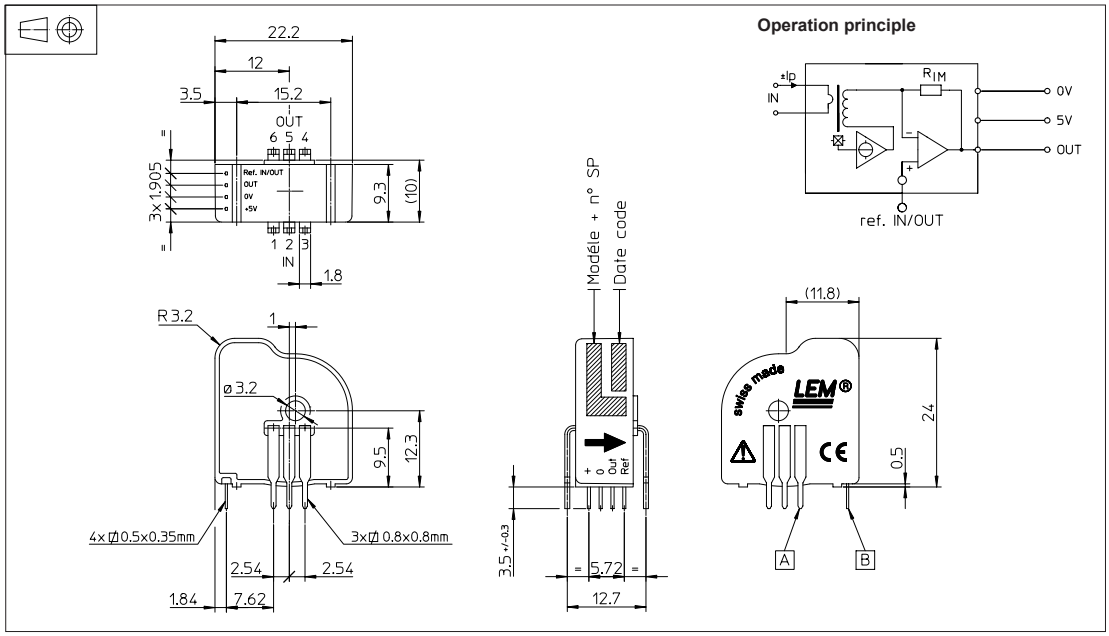
## Safety

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (eg. primary busbar, power supply).
Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a built-in device, whose conducting parts must be inaccessible after installation.
A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

## Dimensions LTSR 6-NP (in mm.)




| Number of primary turns | Primary nominal current rms $I_{PN}$ [ A ] | Nominal [1] output voltage $V_{OUT}$ [ V ] | Primary resistance $R_P$ [ mΩ ] | Primary insertion inductance $L_P$ [ µH ] | Recommended connections |
|---|---|---|---|---|---|
| 1 | ± 6 | 2.5 ± 0.625 | 0.18 | 0.013 | OUT 6 5 4 / IN 1 2 3 |
| 2 | ± 3 | 2.5 ± 0.625 | 0.81 | 0.05 | OUT 6 5 4 / IN 1 2 3 |
| 3 | ± 2 | 2.5 ± 0.625 | 1.62 | 0.12 | OUT 6 5 4 / IN 1 2 3 |

## Mechanical characteristics

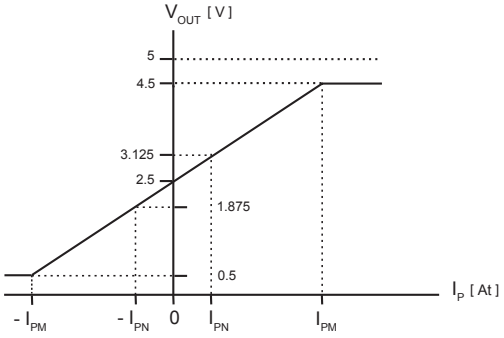
- General tolerance ± 0.2 mm
- Fastening & connection of primary 6 pins 0.8 x 0.8 mm
  Recommended PCB hole 1.3 mm
- Fastening & connection of secondary 4 pins 0.5 x 0.35 mm
  Recommended PCB hole 0.8 mm
- Additional primary through-hole ∅ 3.2 mm

## Remarks

- $V_{OUT}$ swings above the 2.5 V offset when $I_P$ flows from terminals 1, 2, 3 to terminals 4, 5, 6 (with the arrow)
- For the EMC, the acceptance criteria are available on request
- Temperature of the primary conductor should not exceed 100°C.

Note: [1] Output voltage when LTSR 6-NP is used with internal reference.

## Output Voltage - Primary Current



# C.4 OPA548 High-Voltage, High-Current Operational Amplifier



## OPA548 High-Voltage, High-Current Operational Amplifier

### 1 Features

- Wide Supply Range
  - Single Supply: 8 V to 60 V
  - Dual Supply: ±4 V to ±30 V
- High-Output Current:
  - 3-A Continuous
  - 5-A Peak
- Wide Output Voltage Swing
- Fully Protected:
  - Thermal Shutdown
  - Adjustable Current Limit
- Output Disable Control˜
- Thermal Shutdown Indicator
- High Slew Rate: 10 V
- Low Quiescent Current
- Packages:
  - 7-Lead TO-220, Zip and Straight Leads
  - 7-Lead DDPAK Surface-Mount

### 2 Applications

- Valve, Actuator Drivers
- SYNCHRO, SERVO Drivers
- Power Supplies
- Test Equipment
- Transducer Excitation
- Audio Amplifiers

### 3 Description

The OPA548 device is a low-cost, high-voltage and high-current operational amplifier that's ideal for driving a wide variety of loads. A laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high-output voltage and current.

The OPA548 device operates from either single or dual supplies for design flexibility. In single-supply operation, the input common-mode range extends below ground.

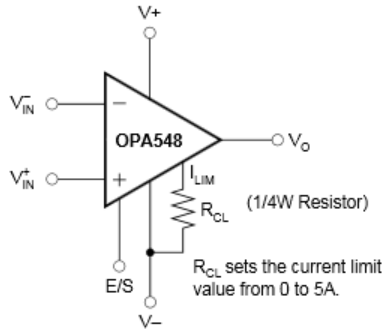
The OPA548 device is internally protected against over-temperature conditions and current overloads. In addition, the OPA548 device was designed to provide an accurate, user-selected current limit. Unlike other designs, which use a *power* resistor in series with the output current path, the OPA548 device senses the load indirectly. This allows the current limit to be adjusted from 0 A to 5 A with a resistor and potentiometer or controlled digitally with a voltage-out or current-out DAC.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA548 | TO-220 (7) | 10.17 mm × 8.38 mm |
| | TO-263 (7) | 10.10 mm × 8.89 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



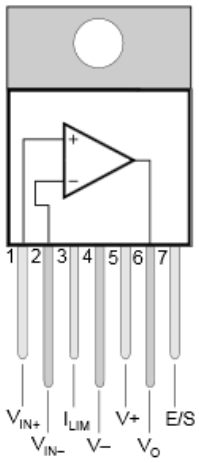
## 5 Description (continued)

The Enable/Status (E/S) pin provides two functions. An input on the pin not only disables the output stage to effectively disconnect the load, but also reduces the quiescent current to conserve power. The E/S pin output can be monitored to determine if the OPA548 is in thermal shutdown.

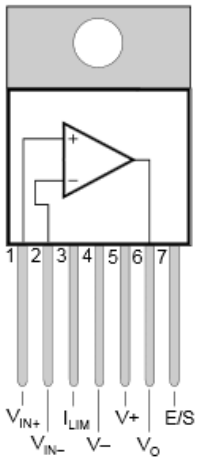
The OPA548 device is available in an industry-standard 7-lead staggered and straight lead TO-220 package, and a 7-lead DDPAK surface-mount plastic power package. The copper tab allows easy mounting to a heat sink or circuit board for excellent thermal performance. The device is specified for operation over the extended industrial temperature range, –40°C to 85°C. A SPICE macromodel is available for design analysis.

## 6 Pin Configuration and Functions

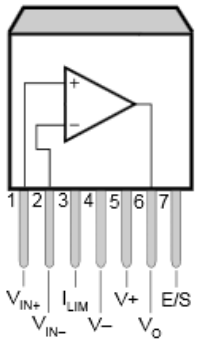
**KVT and KC Packages Stagger-Formed**
**7-Pin TO-220**
**Top View**




**KVT and KC Packages Straight-Formed**
**7-Pin TO-220**
**Top View**




**KTW Package Surface-Mount**
**7-Pin TO-263**
**Top View**



**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $V_{IN+}$ | 1 | I | Noninverting input |
| $V_{IN-}$ | 2 | I | Inverting input |
| $I_{LIM}$ | 3 | I | Current limit set |
| V- | 4 | I | Negative power supply |
| V+ | 5 | I | Positive power supply |
| $V_O$ | 6 | O | Output |
| E/S | 7 | I/O | Enable/disable control input, thermal shutdown status output |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | Output current | See Figure 40 | | |
| | Supply voltage, V+ to V– | | 60 | V |
| | Input voltage | (V–) –0.5V | (V+) + 0.5 | V |
| | Input shutdown voltage | | | V+ |
| | Operating temperature | –40 | 125 | °C |
| | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Machine model | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage (V+-V-) | 8(+/-4) | | 60(±30) | V |
| Specified temperature | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC (1) | | OPA548 | | UNIT |
|---|---|---|---|---|
| | | KVT and KC (TO-220) | KTW (DDPAK) | |
| | | 7 PINS | 7 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 30.2 | 30.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 37.4 | 37.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 14.4 | 14.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.1 | 5.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 14.3 | 14.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.2 | 0.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

# C.5 AD7680 16-Bit ADC

ANALOG DEVICES

# 3 mW, 100 kSPS, 16-Bit ADC in 6-Lead SOT-23

## AD7680

### FEATURES

- Fast throughput rate: 100 kSPS
- Specified for $V_{DD}$ of 2.5 V to 5.5 V
- Low power
  - 3 mW typ at 100 kSPS with 2.5 V supply
  - 3.9 mW typ at 100 kSPS with 3 V supply
  - 16.7 mW typ at 100 kSPS with 5 V supply
- Wide input bandwidth
  - 86 dB SNR at 10 kHz input frequency
- Flexible power/serial clock speed management
- No pipeline delays
- High speed serial interface
  - SPI®/QSPI™/µWire/DSP compatible
- Standby mode: 0.5 µA max
- 6-Lead SOT-23 and 8-Lead MSOP packages

### APPLICATIONS

- Battery-powered systems:
  - Personal digital assistants
  - Medical instruments
  - Mobile communications
- Instrumentation and control systems
- Remote data acquisition systems
- High speed modems
- Optical sensors

### GENERAL DESCRIPTION

The AD7680 is a 16-bit, fast, low power, successive approximation ADC. The part operates from a single 2.5 V to 5.5 V power supply and features throughput rates up to 100 kSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 7 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7680 uses advanced design techniques to achieve very low power dissipation at fast throughput rates. The reference for the part is taken internally from $V_{DD}$, which allows the widest dynamic input range to the ADC. Thus, the analog input range for this part is 0 V to $V_{DD}$. The conversion rate is determined by the SCLK frequency.

### FUNCTIONAL BLOCK DIAGRAM

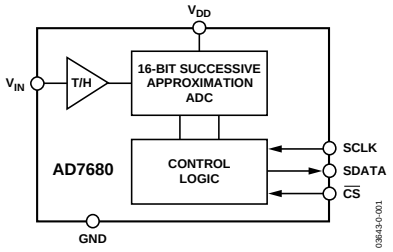



*Figure 1.*

**Table 1. MSOP/SOT-23 16-Bit PulSAR ADC**

| Type/kSPS | 100 kSPS | 250 kSPS | 500 kSPS |
|---|---|---|---|
| True Differential | AD7684 | AD7687 | AD7688 |
| Pseudo Differential | AD7683 | AD7685 | AD7686 |
| Unipolar | AD7680 | | |

### PRODUCT HIGHLIGHTS

1. First 16-bit ADC in a SOT-23 package.
2. High throughput with low power consumption.
3. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced when a power-down mode is used while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 0.5 µA max when in shutdown.
4. Reference derived from the power supply.
5. No pipeline delays.

This part features a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.



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# SPECIFICATIONS[1]

**Table 2. $V_{DD}$ = 4.5 V to 5.5 V, $f_{SCLK}$ = 2.5 MHz, $f_{SAMPLE}$ = 100 kSPS, unless otherwise noted; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted**

| Parameter | A, B Versions[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| DYNAMIC PERFORMANCE | | | $f_{IN}$ = 10 kHz sine wave |
| Signal-to-Noise + Distortion (SINAD)[2] | 83 | dB min | |
| | 85 | dB typ | |
| Signal-to-Noise Ratio (SNR)[2] | 84 | dB min | |
| | 86 | dB typ | |
| Total Harmonic Distortion (THD)[2] | −97 | dB typ | |
| Peak Harmonic or Spurious Noise (SFDR)[2] | −95 | dB typ | |
| Intermodulation Distortion (IMD)[2] | | | |
| Second-Order Terms | −94 | dB typ | |
| Third-Order Terms | −100 | dB typ | |
| Aperture Delay | 20 | ns max | |
| Aperture Jitter | 30 | ps typ | |
| Full Power Bandwidth | 8 | MHz typ | @ −3 dB |
| | 2.2 | MHz typ | @ −0.1 dB |
| DC ACCURACY | | | |
| No Missing Codes | 15 | Bits typ | |
| Integral Nonlinearity[2] | ±4 | LSB typ | |
| Offset Error[2] | ±1.68 | mV max | |
| Gain Error[2] | ±0.038 | % FS max | |
| ANALOG INPUT | | | |
| Input Voltage Ranges | 0 to $V_{DD}$ | V | |
| DC Leakage Current | ±0.3 | µA max | |
| Input Capacitance | 30 | pF typ | |
| LOGIC INPUTS | | | |
| Input High Voltage, $V_{INH}$ | 2.8 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.4 | V max | |
| Input Current, $I_{IN}$ | ±0.3 | µA max | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DD}$ |
| Input Capacitance, $C_{IN}$[2, 3] | 10 | pF max | |
| LOGIC OUTPUTS | | | |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ − 0.2 | V min | $I_{SOURCE}$ = 200 µA |
| Output Low Voltage, $V_{OL}$ | 0.4 | V max | $I_{SINK}$ = 200 µA |
| Floating-State Leakage Current | ±0.3 | µA max | |
| Floating-State Output Capacitance[2, 3] | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | |
| CONVERSION RATE | | | |
| Conversion Time | 8 | µs max | 20 SCLK cycles with SCLK at 2.5 MHz |
| | 9.6 | µs max | 24 SCLK cycles with SCLK at 2.5 MHz |
| Track-and-Hold Acquisition Time | 1.5 | µs max | |
| | 400 | ns max | Sine wave input ≤ 10 kHz |
| Throughput Rate | 100 | kSPS | See the Serial Interface section |
| POWER REQUIREMENTS | | | |
| $V_{DD}$ | 4.5/5.5 | V min/V max | |
| $I_{DD}$ | | | Digital $I/P_S$ = 0 V or $V_{DD}$ |
| Normal Mode (Static) | 5.2 | mA max | SCLK on or off. $V_{DD}$ = 5.5 V |
| Normal Mode (Operational) | 4.8 | mA max | $f_{SAMPLE}$ = 100 kSPS. $V_{DD}$ = 5.5 V; 3.3 mA typ |
| Full Power-Down Mode | 0.5 | µA max | SCLK on or off. $V_{DD}$ = 5.5 V |
| Power Dissipation[4] | | | $V_{DD}$ = 5.5 V |
| Normal Mode (Operational) | 26.4 | mW max | $f_{SAMPLE}$ = 100 kSPS |
| Full Power-Down | 2.75 | µW max | |

[1] Temperature range as follows: B Version: −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] See the Power vs. Throughput Rate section.

# SPECIFICATIONS[1]

**Table 3. $V_{DD}$ = 2.5 V to 4.096 V, $f_{SCLK}$ = 2.5 MHz, $f_{SAMPLE}$ = 100 kSPS, unless otherwise noted; $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.**

| Parameter | A Version[1] | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | $f_{IN}$ = 10 kHz sine wave |
| Signal-to-Noise + Distortion (SINAD)[2] | 83 | 83 | dB min | $V_{DD}$ = 4.096 V |
| | 82 | 82 | dB min | $V_{DD}$ = 2.5 V to 3.6 V |
| | 86 | 86 | dB typ | |
| Signal-to-Noise Ratio (SNR)[2] | 84 | 84 | dB min | $V_{DD}$ = 4.096 V |
| | 83 | 83 | dB min | $V_{DD}$ = 2.5 V to 3.6 V |
| | 86 | 86 | dB typ | |
| Total Harmonic Distortion (THD)[2] | −98 | −98 | dB typ | |
| Peak Harmonic or Spurious Noise (SFDR)[2] | −95 | −99 | dB typ | |
| Intermodulation Distortion (IMD)[2] | | | | |
| Second-Order Terms | −94 | −94 | dB typ | |
| Third-Order Terms | −100 | −100 | dB typ | |
| Aperture Delay | 20 | 10 | ns max | |
| Aperture Jitter | 30 | 30 | ps typ | |
| Full Power Bandwidth | 7 | 7 | MHz typ | @ −3 dB; $V_{DD}$ = 4.096 V |
| | 5 | 5 | MHz typ | @ −3 dB; $V_{DD}$ = 2.5 V to 3.6 V |
| | 2 | 2 | MHz typ | @ −0.1 dB; $V_{DD}$ = 4.096 V |
| | 1.6 | 1.6 | MHz typ | @ −0.1 dB; $V_{DD}$ = 2.5 V to 3.6 V |
| DC ACCURACY | | | | |
| No Missing Codes | 14 | 15 | Bits min | |
| Integral Nonlinearity[2] | ±3.5 | ±3.5 | LSB max | $V_{DD}$ = 4.096 V |
| | ±3 | ±3 | LSB max | $V_{DD}$ = 2.5 V to 3.6 V |
| Offset Error[2] | ±1.25 | ±1.25 | mV max | $V_{DD}$ = 4.096 V |
| | ±1.098 | ±1.098 | mV max | $V_{DD}$ = 2.5 V to 3.6 V |
| Gain Error[2] | ±0.038 | ±0.038 | % FS max | |
| ANALOG INPUT | | | | |
| Input Voltage Ranges | 0 to $V_{DD}$ | 0 to $V_{DD}$ | V | |
| DC Leakage Current | ±0.3 | ±0.3 | µA max | |
| Input Capacitance | 30 | 30 | pF typ | |
| LOGIC INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | 2.4 | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.4 | 0.4 | V max | |
| Input Current, $I_{IN}$ | ±0.3 | ±0.3 | µA max | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DD}$ |
| Input Capacitance, $C_{IN}$[2, 3] | 10 | 10 | pF max | |
| LOGIC OUTPUTS | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ − 0.2 | $V_{DD}$ − 0.2 | V min | $I_{SOURCE}$ = 200 µA |
| Output Low Voltage, $V_{OL}$ | 0.4 | 0.4 | V max | $I_{SINK}$ = 200 µA |
| Floating-State Leakage Current | ±0.3 | ±0.3 | µA max | |
| Floating-State Output Capacitance[2, 3] | 10 | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | | |
| CONVERSION RATE | | | | |
| Conversion Time | 8 | 8 | µs max | 20 SCLK cycles with SCLK at 2.5 MHz |
| | 9.6 | 9.6 | µs max | 24 SCLK cycles with SCLK at 2.5 MHz |
| Track-and-Hold Acquisition Time | 1.5 | 1.5 | µs max | Full-scale step input |
| | 400 | 400 | ns max | Sine wave input ≤ 10 kHz |
| Throughput Rate | 100 | 100 | kSPS | See the Serial Interface section |

| Parameter | A Version[1] | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| POWER REQUIREMENTS | | | | |
| $V_{DD}$ | 2.5/4.096 | 2.5/4.096 | V min/max | |
| $I_{DD}$ | | | | Digital I/Ps = 0 V or $V_{DD}$ |
| Normal Mode (Static) | 2.8 | 2.8 | mA max | SCLK on or off; $V_{DD}$ = 4.096 V |
| | 2 | 2 | mA max | SCLK on or off; $V_{DD}$ = 3.6 V |
| Normal Mode (Operational) | 2.6 | 2.6 | mA max | $f_{SAMPLE}$ = 100 kSPS; $V_{DD}$ = 4.096 V; 1.75 mA typ |
| | 1.9 | 1.9 | mA max | $f_{SAMPLE}$ = 100 kSPS; $V_{DD}$ = 3.6 V; 1.29 mA typ |
| Full Power-Down Mode | 0.3 | 0.3 | µA max | SCLK on or off |
| Power Dissipation[4] | | | | |
| Normal Mode (Operational) | 10.65 | 10.65 | mW max | $f_{SAMPLE}$ = 100 kSPS; $V_{DD}$ = 4.096 V |
| | 6.84 | 6.84 | mW max | $f_{SAMPLE}$ = 100 kSPS; $V_{DD}$ = 3.6 V |
| | 3 | 3 | mW typ | $V_{DD}$ = 2.5 V |
| Full Power-Down | 1.23 | 1.23 | µW max | $V_{DD}$ = 4.096V |
| | 1.08 | 1.08 | µW max | $V_{DD}$ = 3.6 V |

[1] Temperature range as follows: A, B Versions: −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] See the Power vs. Throughput Rate section.

## TIMING SPECIFICATIONS[1]

**Table 4. $V_{DD}$ = 2.5 V to 5.5 V; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.**

| | Limit at $T_{MIN}$, $T_{MAX}$ | | | |
|---|---|---|---|---|
| **Parameter** | **3 V** | **5 V** | **Unit** | **Description** |
| $f_{SCLK}$[2] | 250 | 250 | kHz min | |
| | 2.5 | 2.5 | MHz max | |
| $t_{CONVERT}$ | 20 × $t_{SCLK}$ | 20 × $t_{SCLK}$ | min | |
| $t_{QUIET}$ | 100 | 100 | ns min | Minimum quiet time required between bus relinquish and start of next conversion |
| $t_1$ | 10 | 10 | ns min | Minimum $\overline{CS}$ pulse width |
| $t_2$ | 10 | 10 | ns min | $\overline{CS}$ to SCLK setup time |
| $t_3$[3] | 48 | 35 | ns max | Delay from $\overline{CS}$ until SDATA three-state disabled |
| $t_4$[3] | 120 | 80 | ns max | Data access time after SCLK falling edge |
| $t_5$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK low pulse width |
| $t_6$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK high pulse width |
| $t_7$ | 10 | 10 | ns min | SCLK to data valid hold time |
| $t_8$[4] | 45 | 35 | ns max | SCLK falling edge to SDATA high impedance |
| $t_{POWER-UP}$[5] | 1 | 1 | µs typ | Power up time from full power-down |

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of 1.6 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4] $t_8$ is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, $t_8$, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5] See Power vs. Throughput Rate section.

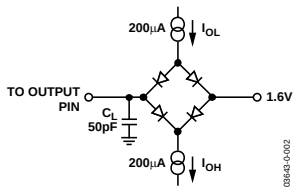


*Figure 2. Load Circuit for Digital Output Timing Specification*

# ABSOLUTE MAXIMUM RATINGS

**Table 5. $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to +7 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | ±10 mA |
| Operating Temperature Range | |
| Commercial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| SOT-23 Package, Power Dissipation | 450 mW |
| $\theta_{JA}$ Thermal Impedance | 229.6°C/W |
| $\theta_{JC}$ Thermal Impedance | 91.99°C/W |
| MSOP Package, Power Dissipation | 450 mW |
| $\theta_{JA}$ Thermal Impedance | 205.9°C/W |
| $\theta_{JC}$ Thermal Impedance | 43.74°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 secs) | 215°C |
| Infared (15 secs) | 220°C |
| ESD | 2 kV |

[1]Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

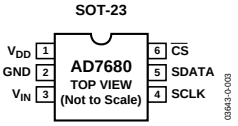


*Figure 3. SOT-23 Pin Configuration*

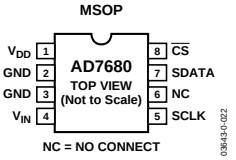


*Figure 4. MSOP Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. SOT-23 | Pin No. MSOP | Mnemonic | Function |
|---|---|---|---|
| 1 | 1 | $V_{DD}$ | Power Supply Input. The $V_{DD}$ range for the AD7680 is from 2.5 V to 5.5 V. |
| 2 | 2, 3 | GND | Analog Ground. Ground reference point for all circuitry on the AD7680. All analog input signals should be referred to this GND voltage. |
| 3 | 4 | $V_{IN}$ | Analog Input. Single-ended analog input channel. The input range is 0 V to $V_{DD}$. |
| 4 | 5 | SCLK | Serial Clock. Logic input. SCLK provides the serial clock for accessing data from this part. This clock input is also used as the clock source for the AD7680's conversion process. |
| 5 | 7 | SDATA | Data Out. Logic output. The conversion result from the AD7680 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7680 consists of four leading zeros followed by 16 bits of conversion data that are provided MSB first. This will be followed by four trailing zeroes if $\overline{CS}$ is held low for a total of 24 SCLK cycles. See the Serial Interface section. |
| 6 | 8 | $\overline{CS}$ | Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7680 and framing the serial data transfer. |
| N/A | 6 | NC | No Connect. This pin should be left unconnected. |