SiPM Multi-Pixel Readout ASIC

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***Abstract* - This work designs an application specific integrated circuit (ASIC) to capture the signal from the silicon photomultiplier sensors (SiPM) which have many applications, since aerospace industry, physics or astronomy.**

Firstly, the possible alternatives existing today by manufactures and the behavior of some sensors of this type are studied in order to justify the circuit design or its future manufacture.

After a first analysis, the development of the circuit consists essentially in two parts, the analog circuit and the digital circuit.

The analog circuit consists in the acquisition of the signal from the sensor, its amplification and its modulation in order to be able to extract useful information from the signal.

The digital circuit is an analog-digital converter, Flash A/D type, which allows the quantification and discretization of the signal coming from the analog circuit. The signal is initially compared with 7 predefined voltage levels being thus possible to quantify 7 amplitude levels that reach the sensor at that moment. Subsequently the signal is encoded and the final outputs are the 3 encoder outputs.

It is intended that in normal operation of the circuit, the clock is turned off, thus the circuit is an asynchronous flash converter. So, prior to encoding it is necessary to synchronize the signal in the converter with an existing circuit for this.

To observe the behavior and results, the circuits were simulated in Cadence software with the technology AMS CMOS C35B4 - 0.35μm.

Index terms: ASIC; SiPM; asynchronous flash converter; quantify 7 amplitude levels.

I. MOTIVATION

Photomultipliers sensors are a type of sensors with a large range of application in engineering that allow the acquisition of electromagnetic radiation and generate electric signals which allow extracting information in order to get the necessary data for the application in question.

The applications for this type of sensors vary widely since the space industry, physics (cosmic ray detection), the aeronautics industry (engine applications), monitoring of nuclear power plants, medical imaging, and so on.

In aerospace industry this type of sensors are used to develop new control technology which uses light detection systems in a non-intrusive method for engines combustion. By observing the flame in the combustion chamber, this method allows a better control and engine performance. [1]

In physics for example, they are used in cosmic ray detection, particles endowed with high energy which collide with existing atoms in the Earth's atmosphere as they are penetrating it. As a result of theses collisions is released electromagnetic radiation, UV-light, that has wavelength capable of being detected by photomultipliers sensors.

Usually, the detection occurs in an Imaging Atmospheric Cherenkov Telescopes equipped with this type of sensors to study the night sky background.

There are several types of sensors for light detection (electromagnetic radiation), the photomultipliers are the ones that have better features for applications with low light, they have fast time response and high energy resolution (capable of detecting a single photon). The silicon photomultipliers (SiPM) are a recent alternative to photomultiplier tubes (PMT), are smaller, usually require lower voltage and suffer less damage by high energy levels.

To detect single photon events these devices are build from an avalanche photodiode (APD) array on common Si substrate and their density usually can vary between 100 and 1000 per mm2. The signal of all photodiodes is added to form the sensor output signal. The typical gain for this type of sensors is 10^6, the same magnitude order of photomultipliers tubes[2].

II. SiPMs

After seeing the applications for these sensors, in this section will be seen how they are composed, what are the main characteristics and operation modes.

A huge gain can be obtained by APD when it is operating at "Geiger Mode" condition. This condition can be achieved when a reverse voltage applied to APD is greater than breakdown voltage, so the internal electric field becomes so high that the gain has an order of magnitude 10^5 to 10^6. When an APD operate in "Geiger Mode" generates a very large pulse when a carrier is injected into the avalanche layer by incident photons.

The conversion from electromagnetic radiation to an electric pulse occurs when the photons having more energy than the banggap of the detector material are absorbed, exciting an electron from the valence band of the semiconductor to the conduction band. The electron in the conduction band moves into the avalanche region, the electric field strength is sufficient to accelerate it to the point at which it can cause "impact ionization" and liberate another electron. Both of these electrons can be accelerated as well, creating an avalanche multiplication. As explained in [3] and seen in the next figure.

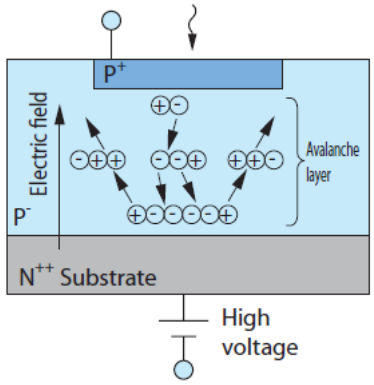

Figure 1 - Operating principle of APD [3] Generated carries produce new electron-hole pairs while being accelerated by high electric field. Newly generated carries are also accelerated to produce further electron-hole pair, and this process repeats itself.

This operation mode can increased the modest gain of an APD to a more significant level. In a single photon counting APD in Geiger mode, the electric field described above increase with increasing the applied voltage, thereby increasing the APD gain. But this work only up to a point. At some operating voltage, the semiconductor junction breaks down and the APD become a conductor (above this breakdown voltage the APD is stable until an electron enter in the avalanche region, this results in avalanche region breakdown and the APD become a conductor, this is known as Geiger discharge).

The reset of this device is accomplished by placing a resistor in series with the detector. When the junction breaks down, large current flows through the resistor, resulting in a voltage drop across the APD.[4]

With a single APD only is possible knows if the APD was triggered or not. Using an APD array can be distinguished a multi or a single photon event. For the Multi-Pixel Photon Counter (MPPC) from Hamamatsu Photonics, the sum of the output from each APD pixel forms the MPPC output, this allows a single photon counting or pulses of multiple photons.

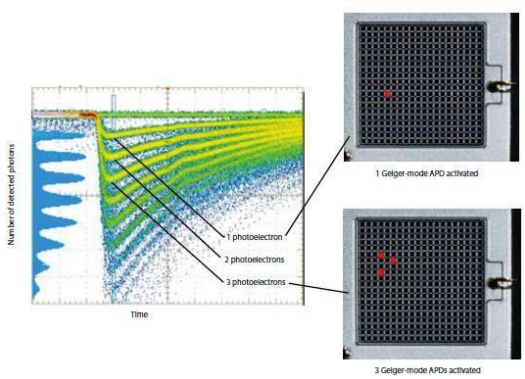

Figure 2 - Numbers of photondetections in a MPPC Hamamatsu [3]

Some of the experimental data were obtained from a Hamamatsu S10362-11-100 MPPC as the Figure 2. This type of sensors has some advantages; the active area of device is very small because the MPPC is an array of APD on a common substrate. The most disadvantage of this device is the dark current, typically at room temperature are 10^5 -10^6 counts per second.

A. State of the Art and SiPM ASICs

This section will present different ASICs and their techniques, which are available at this moment on the market, for the SiPM readout and photon counting.

There are several dedicated devices to SIPM sensors, but since such sensors are relatively new, the variety of the circuits available in the market is quite limited.

The Hamamatsu MPPC module is a photon counting module capable of low light detection. In addition to including a MPPC device mentioned before, the module includes current to voltage converted circuit, high speed comparator circuit, high voltage power supply circuit, temperature compensation circuit, counter circuit and microcontroller. But this cooling system has a very low efficiency and the reduction of temperature degrees is small[3]. These modules of Hamamatsu do not allow the integration of more SIPM sensors than that which is already integrated. In order to find an alternative for this limitation, there are several companies dedicated to developing chips to readout such photon detectors, for example, the Orsay Microelectronic group (OMEGA) with : MAROC, HARDROC, EASIROC and SPIROC.

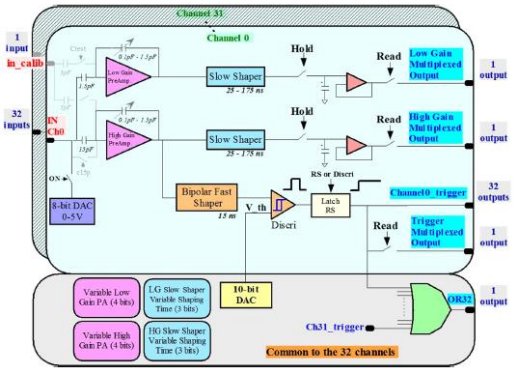

Figure 3 – Diagram of EASIROC [5]

The EASIROC (Extended Analog Silicon PM Integrated ReadOut Chip) is an ASIC with 32 input with bias voltage adjustment for individual channel by 4.5V/8 bit input DAC. Similar to MAROC, the pulse height is sample and holded by external signal and stored in analog memory. The previous figure shows the diagram of the EASIROC ASIC. [5]

The MAROC chip was originally designed to read out MA-PMT (Multi Anode Photo Multiplier Tubes) for a luminometry application. Among the devices presented above, the one that has the most similar characteristics to desirable for this project, is the MAROC chip. But, since this device was design originally for PMT, is already optimized for PMT and some of its features are not suitable for the SiPM tested. The time constant of the shaper are too large for the desired response, however has a 64-channel input front end circuit developed to read out sensor's output.

Another similar device is the HARDROC, it is a mixed signal front-end chip integrating analogue front-end and digital memory. Originally designed to read out RPC (Resistive Plate Chamber) detectors, HARCROC features MAROC front-end therefore it can trigger on SiPM single photoelectron. The manufacturer presents this ASIC as being made of:

- Fast low impedance preamplifier with 6bits variable gain
- Variable shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC.

-Variable gain fast shaper (15ns) followed by two low offset discriminators to autotrig down to10 fC. The thresholds are loaded by two internal 10 bit- DACs.
- A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.

The photon counting is the main features of this project, as seen previously, the output of an MPPC sensor is proportional to the amount of photons that reaches the sensor, however, the discriminator in the previous ASICs does not allow these circuits if one or more photons reached the sensor and quantifies them in a short period of time. Thus, when two detections are near in time, it is not possible to determine the second correctly. To achieve this it is necessary a fast converter (ADC) and the proposed circuit to achieve these results is shown below.

III. SIMULATED AND EXPERIMENTAL DATA

In order to simulate the proposed ASIC two types of data was used as simulation inputs: experimental data which were obtained in LIP and collected in a digital oscilloscope; and a simulated sensor pulse.

The simulation of silicon Photomultiplier signals is explained in [6] and it is used the following circuit to achieve a SiPM pulse.

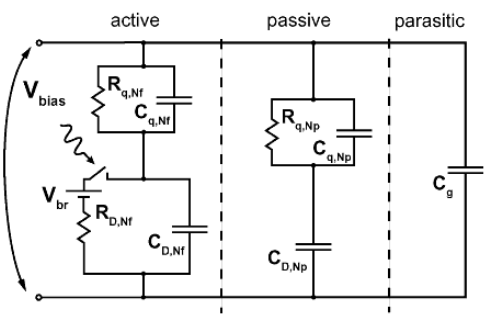

Figure 4 - Circuit for the discharge of N microcells in a MPPC.[6]

The resistors and capacitors of circuit in Figure 4 are given by:

$$C_{D,Nf} = C_D . N_f \qquad R_{q,Nf} = \frac{R_q}{N_f} \tag{1}$$

$$C_{q,Nf} = C_q . N_f \qquad C_{D,Np} = C_D . N_p \tag{2}$$

$$R_{q,Np} = \frac{R_q}{N_p} \qquad C_{q,Np} = C_q . N_p \tag{3}$$

$$R_{D,Nf} = \frac{R_D}{N_f} \tag{4}$$

From all the experimental waveforms obtained, was chosen the waveform that represents the worst possible case. The worst case is when the time between two distinct photon detections is lower than the recovery time of the sensor, in other words, it's when the signal sensor increases voltage before reaches the reference voltage as presented in Figure 5.

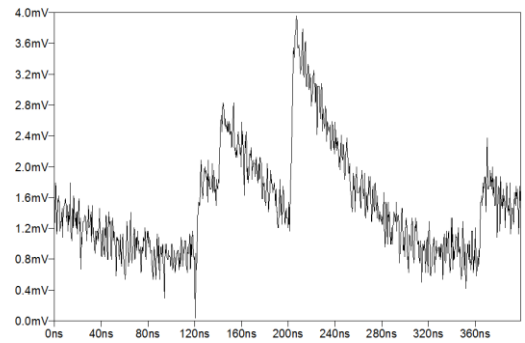

Figure 5 - Experimental data from MPPC sensor

Can be observed that the first two detections have a similar voltage (at 120ns and 140ns) but the voltage difference of the third detection (at 200ns) is approximately the double. This propriety is referenced by manufacturer, as seen before, and means the detection of two photons because the charges generated by sensor are proportional.

A. Data exchange protocol

To ensure the communication with the ASIC was necessary to define how to transmit data from the exterior environment to the chip, in order to implement the desired features with the intention of meet the requirements. One way to do this is through the Serial Peripheral Interface protocol (SPI). The mode used in this work for SPI was the mode 1. All modes and configurations can be seen in [7].

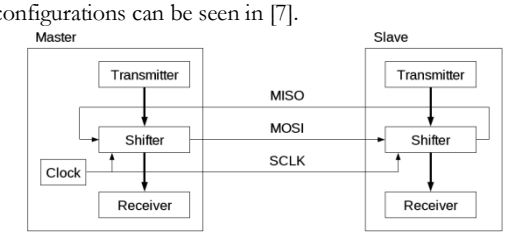

Figure 6 - SPI protocol blocks schematic [7]

The circuit that can implement the communication protocol described above is composed mainly by a shift register (cascade of flip-flops sharing the same clock, the output of each flip-flop is connected to the data input of the next). These shift-registers are configured as serial-in, parallel-out (SIPO), this configuration allows conversion from serial to parallel format, once the data has been input, it may be either read off at each output simultaneously or it can be shifted out and replaced. In Figure 7 can be seen the circuit with cascade of D flip-flop (D-FF) and outputs from Q0 to Qn represent circuit configurations that can be change by user, in order to choose the best for each sensor.

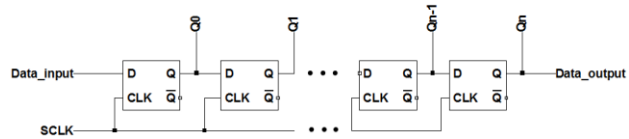

Figure 7 - Shift-register

IV. PROPOSED ANALOG CIRCUIT

The SiPM sensor has an output signal with a specific waveform, which allows knowing how many photon detections reached the sensor. However the output signal is an analog signal, as in most sensors. To convert this analog signal into a useful digital signal is necessary to modify the waveform to be used by a discriminator or in this case by a Flash ADC.

The output signal pulse produced as a result of passage of radiation through a SPIM sensor usually has low amplitude and therefore cannot be directly converted to a digital signal. Unless the detector signal has enough strength, it must be preamplified before it reaches other processing units. The preamplifier is a simple but efficient amplifier connected to the detector output. So, besides the preamplifier, a shaper is necessary in this analog block.

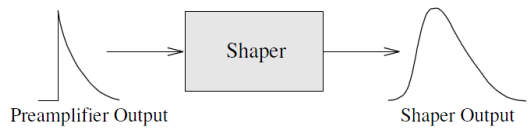

Figure 8 - Pulse Shaping [8]

A. Amplifier

The input signal coming from the SiPM sensor requires a large amplification to be possible convert it into a digital signal. To this work was chosen a differential amplifier (diff-amp) which amplifies the different between two voltages and rejects the average or common mode value of the two voltages.

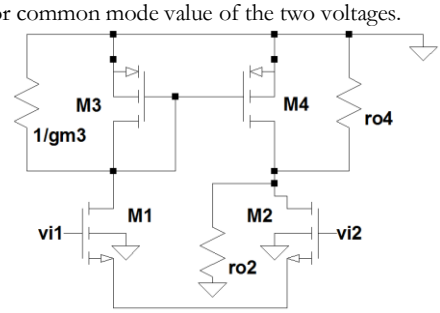

Figure 9 - AC circuit of a diff amp

Using a differential amplifier with current mirror load to performance a large amplification, as Figure 9, where an imbalance in the drain current of M1 and M2 causes the output of the diff-amp to swing either towards VDD or ground.

To determine the AC gain of the diff-amp with a current mirror load, as Figure 9, assuming that the small signal resistance looking into drain of M2 is simply r_{o2} and replace the diode in M3 by $1/g_{m3}$. Since the current in M3 is mirrored by M4, the output voltage is:[9]

$$v_{out} = (i_{d1} - i_{d2}).(r_{o2}||r_{o4}) \tag{5}$$

$$v_{out} = 2i_d.(r_{o2}||r_{o4}) \tag{6}$$

The differential mode gain is then given by:

$$A_d = \frac{v_{out}}{v_{id}} = g_m.(r_{o2}||r_{o4}) \tag{7}$$

In [9] the CMRR is given by,

$$CMRR = \frac{g_{m1}/2g_{m3}}{g_{ds5}/2g_{m3}} = g_{m1}.r_{ds5} \tag{8}$$

In order to reduce the dark current in the sensor to obtain better results, it is necessary to reduce the temperature. Together with specifications was indicated that both the sensor and the circuit should operate close to -50ºC. In simulation was observed the results of amplifier simulation for a range of temperatures. Corners simulations (-70º;150º C)

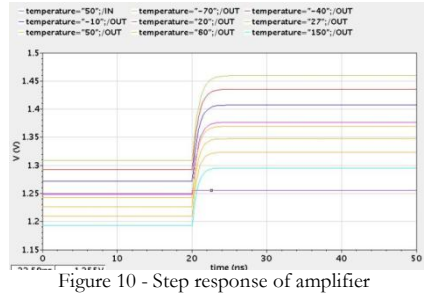

Figure 10 - Step response of amplifier

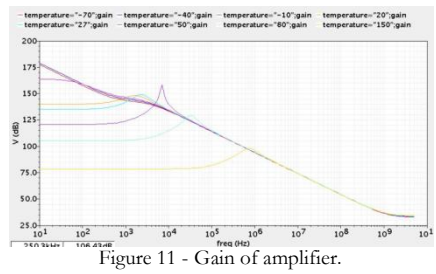

Figure 11 - Gain of amplifier.

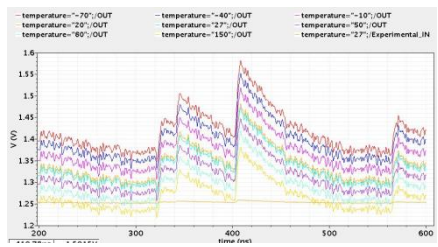

Figure 12 - Response of amplifier with experimental data input.

B. Filter

Among the most popular methods for shaping the signal, was chosen the method of CR-RC², that allows a greater versatility and a better setting for the specifications of the sensors under study. This method, the CR-CR pulse shaping, is perhaps the simplest and the most widely used method of shaping preamplified detector pulses.

The shaper (filter) for this method consists of two parts as the name implies: a CR differentiator (high pass filter) and an RC integrator (low pass filter). As can be seen in [8] and assuming that the input of the CR differentiator is a step function then the pulse after passing the through the CR-RC shaper can be approximated by:

$$V_{out} = \frac{\tau_d(\tau_d e^{-t/\tau_d} + \tau_i e^{-t/\tau_i})}{\tau_d \tau_i(\tau_d - \tau_i)} \tag{9}$$

Realistic shaper output is not similar to a step response of the same shaper. The reason is that the time constant of sensor and the shaper do not differ several orders of magnitude as required by the step function approximation. Realistic SIPM

sensors produce exponential decaying pulses which go into a CR-RC shaper and it exhibit a significant undershoot in the decay part of the shaper output. If a new pulse arrive before the previous one has fully decay, this under undershoot can be a problem especially for a high rate systems. The new pulse will have a lower effective height because it rides on the decaying pulse.

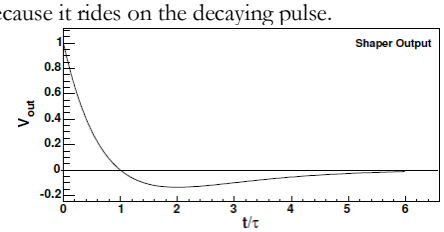

Figure 13 - and shaper response with undershoot in the decaying part [7]

Usually the decay time constant is large with respect to the shaping time, so the undershoot is small. However the decay time constant is set by the signal rate which depends on the sensor used. The rate capability is increased by reducing a quenching resistor, but this increases magnitude of undershoots. By adding a resistor R_{pz} to the shaper's differentiator as shows in Figure 14, the low frequency response is boosted to compensate for the decay of the signal applied to the shaper input [10].

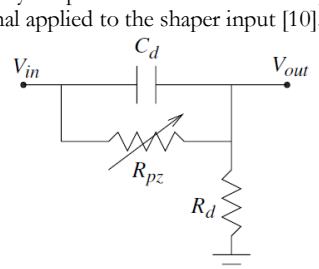

Figure 14 - Pole zero cancellation circuit. Variable resistor allows to minimize the undershoot.

Now the transfer function can be presented as follows [8]:

$$H(s) = \frac{\tau_p \tau_d s}{\tau_p(\tau_d s + 1) + \tau_d} \frac{1}{(\tau_i s + 1)} \tag{10}$$

The response of the filter will depend upon the configuration adopted by user for the sensor in use for each case. To better adapt to several sensors, in the shaper is possible to choose several time constants to the differentiator, to the integrator and for R_{pz}. In the next figures can be observed the obtained results to one of the possible configurations between capacitors and resistors which can be selected by the user according to the sensor used.

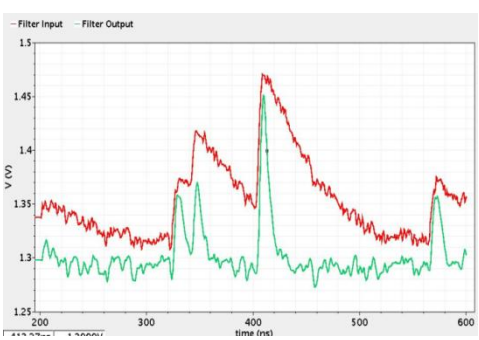

Figure 15 - Filter output and filter input

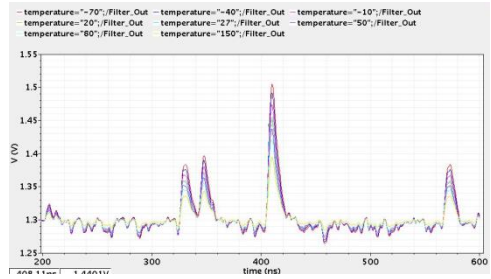

Figure 16 - Filter output to input of experimental data entry before the amplifiers.

V. PROPOSED DIGITAL CIRCUIT

In terms of analyzing and storing the relevant information contained in the signal, the data converter plays an important role, allowing the quantization of the signal to make it useful. Data converters, in this case an Analog-to-Digital converter (ADC), have as input an analog signal with an infinite number of values. To know how many detections were made in the sensor, the input has to be quantized into an N-bit digital word.

The flash ADC has the highest speed allowing the possibility to convert the input analog signal in a useful signal and extract the necessary data. Due to the required speed and technology used in the production of this device, the flash ADC is the most suitable for this work.

A. Flash ADC

A typical flash ADC uses one comparator per quantization level (2N-1) and 2N resistors. Due to its parallel structure, the flash ADC allows fast data conversion some operating at millions of samples per second within different resolutions. The converter in this work is based on common and simple flash ADC with a resistor ladder, an array of comparators (see Figure 17) and a decoder.[11]

One of the main sources of noise is an external clock. So the decoder in this flash ADC has the particularity of being an asynchronous circuit. This previous feature requires an additional configuration of the device as decay time and peak voltage of the sensor, but has the advantage of making this circuit, an asynchronous circuit and thus the clock noise of an external source is eliminated for the entire circuit.

The specifications for this device indicate that are necessary a circuit capable of performing at least 5 detections, so is necessary a 3-bits (N) converter. The ADC input signal V_{IN} is compared with fixed voltages coming from resistor ladder, these are obtained by decomposing the reference voltage V_{REF}. The result of this comparison is a thermometer coded word after comparators and a digital word obtained at decoder output, 2N-1:N.

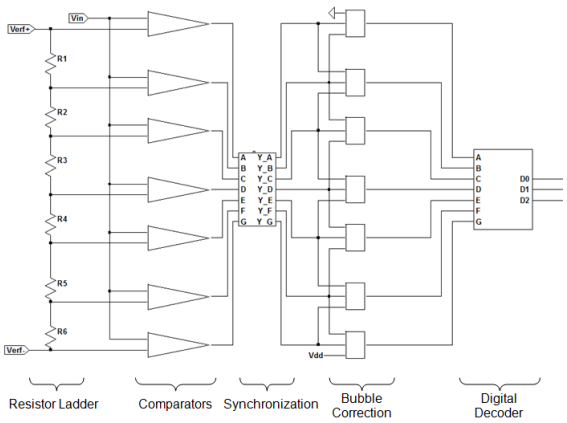

Figure 17 - ADC blocks diagram

To avoid decoding errors the signal passes through two circuit blocks before reaching the decoder. The first of these is a synchronizations circuit since there are no clock, it is important that the edges of the signal to be synchronized. Other circuit is the bubble error correction that ensures a thermometer code before the decoder.

B. Synchronization circuit

To have a useful signal in order to be used in digital devices is necessary that rise and fall edges are synchronized. The input signal in flash A/D has several nanoseconds in both rise and fall time. For a correct decoding is necessary that the input signal edges in decoder are synchronized otherwise is obtain an incorrect decoding losing some of the signal data. The input signal for synchronization circuit is thermometer coded which has as comparators output a logic value of 1 (2.5V) until the corresponding detection or 0 (0V) otherwise.

In Figure 18 can be seen the synchronization circuit. For an example of 3 detections in thermometer coded the inputs G, F and E are at logic value 1, all other inputs are at 0.

Ideally the different between rise times and between fall times for all inputs should be 0s, however that does not happen and there are a delay between the first rise or fall edge and the last one.

For 3 detections, the first input to change for logic value 1 is G in Figure 18, then changes input F and finally the input E. The opposite happens at the end of the detection, the first to change the logic value to 0 is input E and the last is input G.

This ASIC is designed to operate for a variety of SIPM sensors, with different decay times, forms of signal and rate of detections. This is the main reason why the external clock was removed. Thus, the device is set depending on the sensor used.

When the user configure this device should choose the delay time depending on the chosen sensor. The delay time is essential for the proper operation of the Delay block in Figure 18 and should be choose based on the decay time and detections rate of the sensor for a better match. The delay circuit was implemented using a chain of current deprived inverters.

With the delay proper configured for the sensor, the output (Y) of blocks X1:7 allows maintaining the logic level of the input which corresponds to a detection level.

Digital block analog input has a waveform that can be approximated to a Gaussian waveform. Thus the comparator which corresponds to one detection (input G) is the first to change the logic level to 1 and the last to return to 0. This is how all falling edges are aligned, the outputs of X1:7 blocks keep the logic levels at 1 until the delay on G input signal become 0 then all blocks output X1:7 that have the logic level 1 return to 0, thus all falling edges are synchronized.

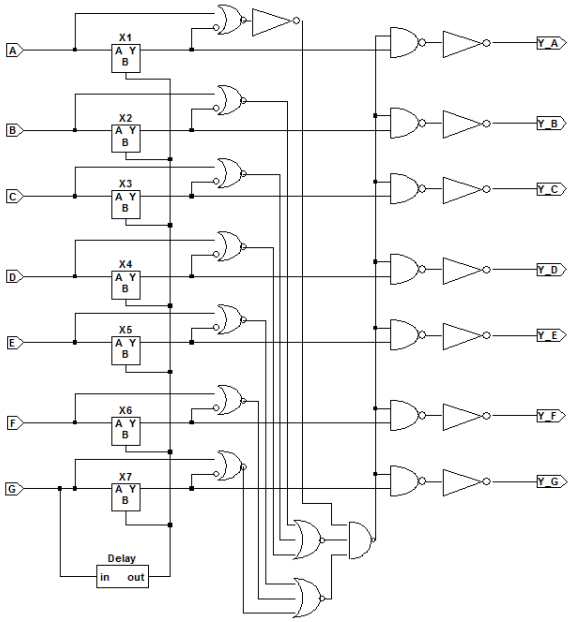

Figure 18 -Synchronization circuit

To align the rising edges is observed the transition from the logic level 1 to 0 of all inputs simultaneously. In this case, the last input to change from 0 to 1, is the first to change from 1 to 0. For the previous example of 3 detections, input E is the first to return to 0, causing all outputs of the synchronization block with detection to have a logic level 1.

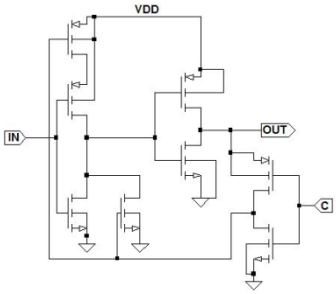

Figure 19 - Circuit of blocks X1:7

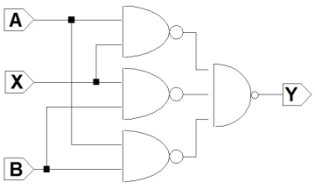

Figure 20 - Bubble correction circuit

C. Digital Decoder

The last block of this work is the decoder of the A/D flash that allows a 3-bits output. A simple 2N-1:N digital thermometer decoder circuit converts the comparators output into a N-bit digital word. After build a truth table were obtained the expressions for each output as following:

$$Q0 = A + \overline{F}G + \overline{D}E + \overline{B}C \tag{11}$$

$$= \overline{\overline{A}.\overline{\overline{F}G}.\overline{\overline{D}E}.\overline{\overline{B}C}} \tag{12}$$

$$Q1 = B + \overline{D}F \tag{13}$$

$$= \overline{\overline{B}.\overline{\overline{D}F}} \tag{14}$$

$$Q2 = D \tag{15}$$

With the above expressions was possible to build the following flash ADC circuit:

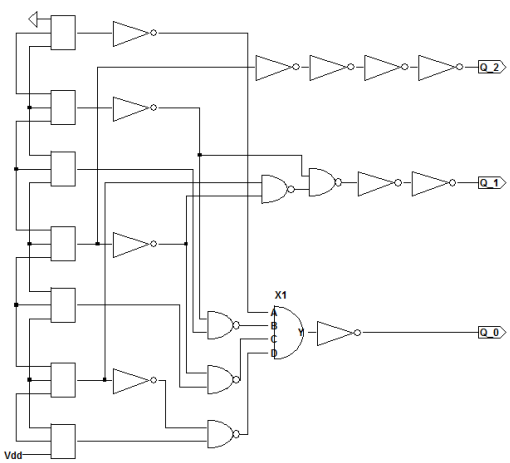

Figure 21 - Decoder gates circuit of flash

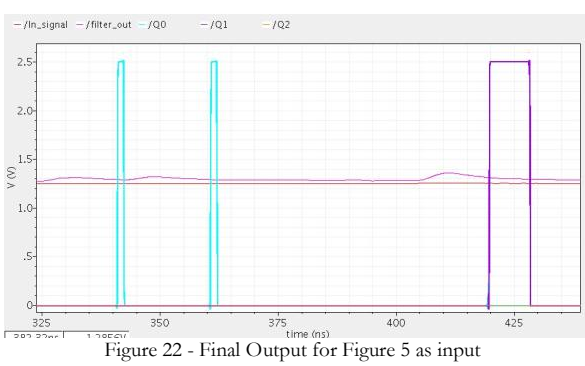

Figure 22 - Final Output for Figure 5 as input

In the Figure 22 is seen the final result for the input observed in Figure 5 from the experimental SiPM sensor. In this figure can be observed two detections of 1 photon each (at 340ns and 360ns) and a third detection of 2 photons (at 420ns). This signal is shifted 200ns in time with respect to Figure 5 because it was the time that the clock was turned on to configure the circuit.

VI. CONCLUSIONS

The proposed concludes that it is possible to design a SiPM Multi-pixel readout ASIC with the implementation of detection up to 7 photons. The circuit was designed in AMS 0.35µm technology and validated with their simulations. This circuit was designed to be used with a variety of SiPM sensors and successful simulated. All the configurations allow the circuit adapts to the sensors chosen by the user. These characteristics vary from the shaping time to the final pulse width. The configuration of the ASIC must be performed initially in order to work with all desired settings, if these configurations are not implemented, the results did not correspond to reality and do not have any valid information. After setting the ASIC, the clock can be turned off and the detection values observed in the final outputs.

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