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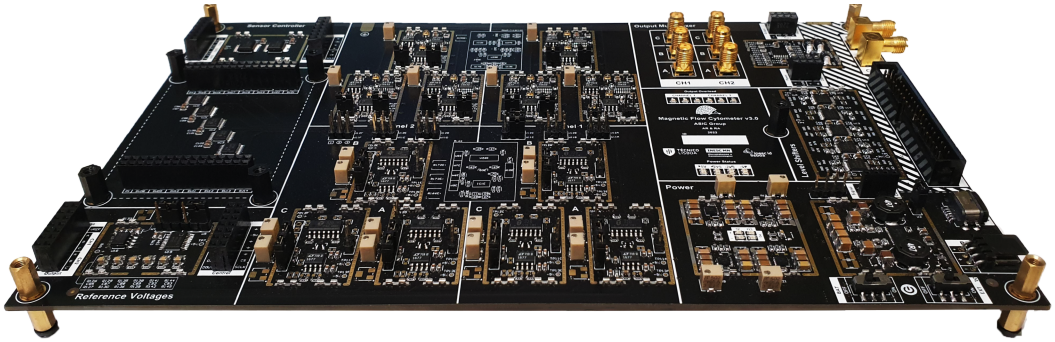

Ultra-Low Noise Analog Electronic Interface for Early Cancer Detection

Applications to Biomedical Analysis

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Thesis to obtain the Master of Science Degree in

Electronics Engineering

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Declaration

I declare that this document is an original work of my authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

Acknowledgments

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To Carolina Guerra, my wonderful girlfriend, who would do everything in her power to make me feel happy, even when she was not feeling so well. During all the stress involved in this dissertation, she was always there with kind and reassuring words.

I thank my fellow friends, João Faustino and Diogo Bernardo, for the stimulating discussions, for the sleepless nights we were working together before deadlines, and for all the fun we had in the last five years. To all the friends I have met that led to this point in my life.

Lastly, throughout the development of this dissertation, I have received a great deal of support and assistance. I would like to thank and apologize to all the people that I have left outside of this acknowledgement.

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Abstract

This work introduces an ultra-low noise magnetic flow cytometer for circulating tumor cell detection. The system comprised analog bias and amplification, analog-to-digital conversion, and signal processing stages. The sensor biasing circuit offers two distinct topologies: one with the sensor inside the feedback loop and the other with the sensor outside that allow precise 16-bit digital control of the current, delivering up to $5\ \mathrm{mA}$ for a sensor with a nominal resistance of $500\ \Omega$. The two-stage amplification utilizes differential AC-coupled inputs providing a total gain of $80\ \mathrm{dB}$ over two stages. A $1\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ ultra-low noise instrumentation amplifier is followed by a non-inverting amplifier topology, while a detection circuit provides a visual and digital alert of possible first-stage saturation. A 4$^{\text{th}}$-order anti-aliasing filter, provides a bandwidth limitation of $100\ \mathrm{kHz}$. The signal chain achieves a noise level of $4\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ at a frequency of $10\ \mathrm{kHz}$. That to the best of the author's knowledge surpasses any previously reported work. The system incorporates a sensor 24 to 6 multiplexing scheme, enabling the digital selection of the desired sensors. The 6 analog channels are multiplexed to two high-speed $65\ \mathrm{MSPS}$ ADCs connected to a DE-10 Standard FPGA for digital signal processing. The board can be powered by batteries, USB, or FPGA. The functionalities of the platform have been successfully implemented and validated.

Keywords

Biomedical analysis; Magnetic flow cytometry; Magnetoresistive sensors; Low-noise analog front-end; Signal measurement chain

Resumo

Este trabalho apresenta um citómetro de fluxo magnético de ultra baixo ruído para deteção de células tumorais circulantes. O sistema é composto por etapas de bias e amplificação analógica, conversão analógico-digital e processamento de sinal. O circuito de polarização do sensor oferece duas topologias distintas: uma com o sensor dentro da malha de realimentação e outra com o sensor fora, permitindo um controlo digital preciso de 16-bits da corrente até $5\mathrm{mA}$ para um sensor com uma resistência nominal de 500Ω. A amplificação de dois estágios utiliza entradas diferenciais com acoplamento AC, proporcionando um ganho total de $80\mathrm{dB}$ nos dois estágios. Um amplificador de instrumentação de ultra baixo ruído de $1\mathrm{nV}/\sqrt{\mathrm{Hz}}$ é seguido por uma topologia de amplificador não inversor, enquanto um circuito de deteção fornece um alerta visual e digital de possível saturação no primeiro estágio. Um filtro antialiasing de 4ª ordem limita a largura de banda a $100\mathrm{kHz}$. A cadeia de sinal alcança um nível de ruído de $4\mathrm{nV}/\sqrt{\mathrm{Hz}}$ a uma frequência de $10\mathrm{kHz}$, que, segundo o conhecimento do autor, supera qualquer trabalho previamente relatado. O sistema incorpora um esquema de multiplexagem de 24 sensores para 6, permitindo a seleção digital dos sensores desejados. Os 6 canais analógicos são multiplexados por dois ADCs de alta velocidade de $65\mathrm{MSPS}$ conectados a uma FPGA DE-10 Standard para processamento digital de sinal. A placa pode ser alimentada por baterias, USB ou FPGA. As funcionalidades da plataforma foram implementadas e validadas com sucesso.

Palavras Chave

Análise biológica; Citometria de fluxo magnético; Sensores magnetoresistivos; Interface analógica de baixo ruído; Cadeia de medição de sinal

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List of Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AC	Alternating
ADC	Analog-to-Digital Converter
AFE	Analogue Front-End
AMR	Anisotropic MagnetoResistance
BPF	BandPass Filter
BJT	Bipolar Junction Transistor
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
DC	Direct
DSP	Digital Signal Processing
FDM	Frequency-Division Multiplexing
FC	Flow Cytometry
FPGA	Field-Programmable Gate Array
GMR	Giant MagnetoResistance
GBWP	Gain–Bandwidth Product
GPIO	General-Purpose Input/Output
HSMC	High-Speed Mezzanine Connector
HPF	HighPass Filter
IC	Integrated Circuit
I2C	Inter-Integrated Circuit

INESC Instituto de Engenharia de Sistemas e Computadores

INESC-ID Instituto de Engenharia de Sistemas e Computadores – Investigacão e Desenvolvimento em Lisboa

INESC-MN Instituto de Engenharia de Sistemas e Computadores – Microsistemas e Nanotecnologias

INL International Iberian Nanotechnology Laboratory

LED Light-Emitting Diode

LDO Low-DropOut

LPF LowPass Filter

MFC Magnetic Flow Cytometry

MNP Magnetic NanoParticles

MR MagnetoResistive

MTJ Magnetic Tunnel Junction

PDMS Polydimethylsiloxane

PCB Printed Circuit Board

PWN Pulse Width Modulation

RC Resistor–Capacitor

RFI Radio-Frequency Interference

SEPIC Single-Ended Primary-Inductor Converter

SNR Signal-to-Noise Ratio

SPI Serial Peripheral Interface

SV Spin Valve

TDM Time-Division Multiplexing

TIA Transimpedance Amplifier

TMR Tunneling MagnetoResistance

USB Universal Serial Bus

VCCS Voltage-Controlled Current Source

1

Introduction

Preamble

This chapter serves as an introduction to the objective of this work, providing insight into the motivation behind the development of an interface for magnetoresistive sensors. The magnetoresistive sensor technology offers unique advantages and potential applications, and this work aims to explore and leverage its capabilities. The core contribution of this work is the design and implementation of an interface specifically tailored for magnetoresistive sensors. The interface will facilitate accurate and reliable measurement of the sensor outputs, ensuring optimal performance and compatibility with existing measurement systems. Special attention will be given to signal conditioning, noise reduction, and data acquisition techniques to enhance the overall quality and reliability of the measurements. The main contributions of this work are also highlighted and the document structure is explained.

Contents

1.1 Motivation

The motivation and incentives, along with a historical context, have influenced the embrace of all the challenges that may lie in this dissertation project. Cancer is one of the world's biggest health problems. It begins when a cell breaks free from the typical restraints on uncontrolled growth and cellular division, which can invade adjacent tissues or organs at a distance. The fast spread of these cells tends to be very aggressive, causing tumors that can propagate to other body regions. Cancer is not just one disease; it is a broad term. It is a group name for more than a hundred and counting diseases, and almost all patients who have cancer develop metastases and die. Therefore, it remains a major unsolved health problem, with conventional cancer treatments having little impact on the disease course [1]. However, early detection can dramatically improve survival rates and reduce treatment costs by 70%. The effect of new treatments for cancer on mortality has been largely disappointing. The most promising approach to control cancer is a national commitment to prevention, with a concomitant rebalancing of the focus and funding of research [2]. The battle against cancer is far from over.

Since the beginning of time, the medical science field, responsible for improving health, treating diseases, and understanding biological functions in humans and animals, had to be in constant development to face the needs of the many. Innovation and medicine have gone hand and hand for a long time. This progress provided the means that allowed Mankind to survive for this long. Proven by the vast and far from over list of known epidemics and pandemics that humans have lived throughout. For example, beginning in 1720, an outbreak of bubonic plague in Marseille, France (known as The Great Plague of Marseille) killed an estimated 100 million people in that city and surrounding provinces and towns. In 1817 the first cholera pandemic recorded in modern history spread from India to Southeast Asia, the Middle East, Europe, and Eastern Africa. The "Spanish flu" influenza in 1918 killed upwards of 50 million people worldwide. And nowadays, declared officially as a pandemic in 2020 [3], the Coronavirus disease outbreak, which is still taking casualties, brought us one overwhelming realization of how fragile life is. As the dates imply, around every 100 years, there is a new pandemic that the world must face. Although the disease that this project aims to prevent, cancer, is not transmissible directly from one person to another and doesn't have a direct relationship with the mentioned ones, the concept being conveyed is that the medical field must be in constant evolution. The genetic basis of cancer, recognized in 1902, with a death toll of 9.6 million in 2012 [4], still doesn't have a cure. Hence, this field has extreme importance and interest concurrently and has my devotion and support.

Furthermore, just like any other scientist, researcher, engineer, or medic that came before or shall come later to improve what began in prior generations. Curiosity, the sense of wonderment that comes from discovery, the act of learning, and deep understanding were the main reasons that motivated me to pick up on this project.

1.2 Purpose and Objectives

The following section discloses the purpose and the objective of this master thesis developed at Instituto de Engenharia de Sistemas e Computadores (INESC). Since the discovery of microorganisms, cell counting techniques induced a great impact on biological sciences [5], including medical diagnosis and treatment. The future of medical diagnostics is detecting the presence of one or more biomarkers through a molecular test. Currently, these molecular tests are accomplished through optical means. However, with recent advances in micro and nanotechnologies, which have enabled new transducers with the same size scale as biomolecules, it is now possible to use electronics to perform this test [6]. To this end, novel biosensing platforms are imperative to make this transition possible. The work accomplished in this dissertation will assist with the development of a system whose purpose is to detect circulating tumour cells responsible for tumour metastasis. The system has a unique combination of microfluidics, magnetic sensors and microelectronics for early cancer detection.

The objective of the work presented in this dissertation is to improve the analog front-end that interfaces the sensors of a previously developed magnetic cytometer. This analog interface contains all the electronic components required to bias the sensors, establishing the necessary electrical condition for the sensor to produce a signal, and all the electronic components used to amplify and filter the signal before the digitalization. This dissertation aims to address the limitations of the previous magnetic cytometer platform while introducing novel features to facilitate further studies in the field. A key aspect of this endeavor is ensuring a high Signal-to-Noise Ratio (SNR), as any noise generated by the circuit can affect the accuracy and reliability of the output. It is crucial to carefully manage the noise level so that it does not overshadow the desired signal response from the sensors. Special attention will be given to minimizing noise sources, optimizing debugging techniques, and implementing effective noise reduction strategies. By prioritizing the maintenance of a favorable SNR, this new platform will enable enhanced sensitivity and improved performance for magnetic field detection and measurement. The noise generated by this discrete electronic circuit should be less or equal to the noise produced by the sensors without compromising the maximum gain and bandwidth necessary for the early cancer detection application. In addition, increasing the number of sensors and the microfluidic channels that contain the sensors is also an objective. Afterwards, a Printed Circuit Board (PCB) designed, assembled and tested will be included in a magnetic flow cytometer prototype system, tailored by several dissertations concurrently to this. With a successful system assembly, the interface is tested by validating the detection of different sized magnetic particles. Hereupon, an article describing the results with the collaboration of all the colleagues involved is published.

All the circuits presented in this work have been meticulously designed either by myself or by research teams affiliated with Instituto de Engenharia de Sistemas e Computadores – Investigacão e Desenvolvimento em Lisboa (INESC-ID). The magnetic sensors utilized in the cytometer system were de-

veloped by separate teams working at Instituto de Engenharia de Sistemas e Computadores – Microsistemas e Nanotecnologias (INESC-MN) and the International Iberian Nanotechnology Laboratory (INL). The collaboration and expertise of these teams have been instrumental in creating robust and cutting-edge circuitry and sensor technology for this project. This collective effort ensures that the resulting platform integrates state-of-the-art work and provides reliable and accurate performance for magnetic field analysis in the cytometer system.

1.3 Document Organization

The document, composed of five distinct chapters, aims to demonstrate the research and work performed in the scope of an ultra-low signal analog electronic interface for early cancer detection. The subsequent paragraphs provide a summary of each chapter.

• Chapter 1 presents the developed project. It covers the motivation to embrace the project challenges (Section 1.1), the purpose and objectives associated with it (Section 1.2), and the structure of this dissertation document (Section 1.3).

• Chapter 2 contains the state of the art that provides valuable information about the sensors used in this work (Section 2.1) and an overview of systems developed inside and outside INESC to interface those sensors (Section 2.2).

• Chapter 3 addresses the application project describing the current technology (Section 3.1) used for similar applications and the working principle of the new technology (Section 3.2) developed to mitigate the old associated issues. This chapter also presents the system architecture (Section 3.3), explaining how it operates and the ambitions of the INESC research team, emphasizing the development of a front-end interface with key specifications (Section 3.4) in the ambit of this work.

• Chapter 4 discloses a comprehensive overview of the developed circuitry within the front-end interface. The chapter delves into various essential circuits, including the analog channel (Section 4.1), the addressing mechanism for the sensors (Section 4.2), the necessary interface for the digital acquisition (Section 4.3 and 4.4), and the power (Section 4.5) vital to the overall system operation. Furthermore, the chapter highlights significant results pertaining to the performance of the complete system (Section 4.6).

• Chapter 5 closes the work performed in this dissertation, stating key outcomes and conclusions (Section 5.1) and defining the future work (Section 5.2).

2

State of the Art

Preamble

This chapter presents the state of the art in the field of magnetoresistive sensors and their interfaces. It provides valuable information about the sensors utilized in this work, as well as an overview of the systems developed both within and outside of INESC that interface with these sensors. By including a comprehensive review of the state of the art in magnetoresistive sensors and their interfaces, this chapter establishes a solid foundation of knowledge to understand the subsequent chapters and support the development of an optimized interface for the magnetoresistive sensors.

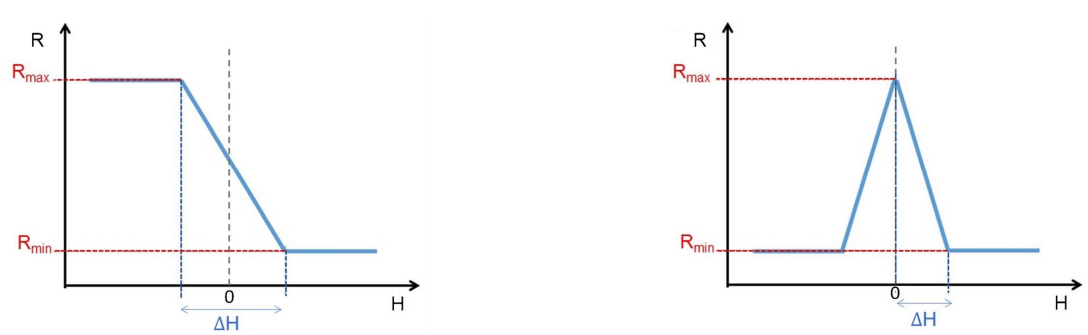
Contents

2.1 Magnetoresistive Sensors

MagnetoResistive (MR) sensors are small components designed to sense an applied magnetic field. Their MR effect occurs when the electrical conductor present in the sensor changes resistance based on an applied magnetic field. The resistance value may increase or decrease, depending on the orientation of the magnetic field [7].

The MR sensors were discovered in 1857 by Lord Kelvin that noticed a slight change in the electrical resistance of a piece of iron when he placed it in a magnetic field. Although the mechanism responsible for Anisotropic MagnetoResistance (AMR) discovered by Kelvin and Giant MagnetoResistance (GMR) discovered by Grünberg [8] and Fert [9] is different, both surge from the interaction of a current with the magnetism of the material [10]. However, the GMR phenomen is the most interesting for this project so it will be explained in detail in the next section. The cause of magnetism in a ferromagnetic material is the uneven distribution of electrons in atoms [11]. That results in a spin-polarized band structure in which there is an imbalance in the number of spin-up and spin-down electrons and consequently net magnetization [10]. The MR sensors have linear change of their electrical resistance with magnetic fields.

Figure 2.1 illustrates the transfer curve that has two types, depending on the sensors. Spin Valve (SV), Magnetic Tunnel Junction (MTJ), and planar Hall sensors have a response to an external magnetic field like Figure 2.1a with the linear region centered at $0T$. However, AMR and GMR multilayer sensors have a transfer curve like Figure 2.1b with the resistance value near R_{max} at $0T$, meaning that it is required an external magnetic field to obtain their maximum linearity.



(a) Spin valve, magnetic tunnel junctions, and planar Hall.

(b) AMR and GMR multilayers.

Figure 2.1: Schematic of the linear MR sensors transfer characteristic (from Soares *et al.* [12]).

The performance of the sensors depends on the magnetoresistance ratio and sensitivity. The MR_{ratio} (Equation 2.1) is the relative resistance variation, while S (Equation 2.2) is the slope of the linear zone,

the MR_{ratio} per unit of the magnetic field [12].

$$MR_{ratio} = \frac{R_{max} - R_{min}}{R_{min}} \quad [\%] \tag{2.1}$$

$$S = \frac{1}{R_{min}} \frac{\partial R}{\partial H} = \frac{1}{R_{min}} \frac{\Delta R}{\Delta H} = \frac{MR_{ratio}}{\Delta H} \quad [\%/T] \tag{2.2}$$

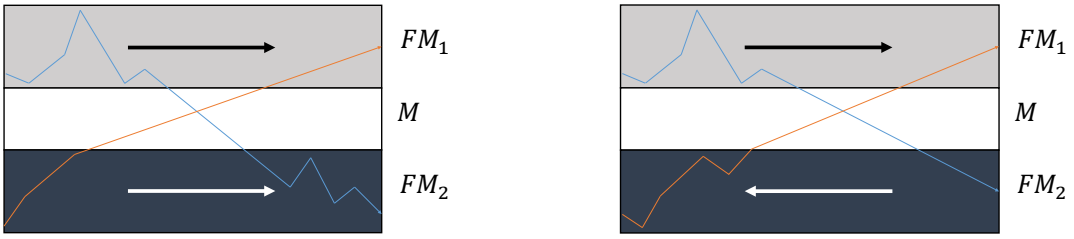
Hence R_{max} and R_{min} are the MR sensor maximum and minimum resistance, and ΔH is the field span where the sensor is linear.

The MR phenomena are based either on: intrinsic magnetoresistance of the ferromagnetic material for the AMR sensors; or ferromagnetic/non-magnetic heterostructure in the case of GMR, SV, and Tunneling MagnetoResistance (TMR) [13].

Giant Magnetoresistance

The GMR phenomenon happens when there is a change in the electrical resistance in thin, stacked layers of ferromagnetic and non-magnetic materials due to the presence of a magnetic field [9].

In 1988, Albert Fert [9] and Peter Grünberg [8] discovered the GMR effect that relies on spin-dependent transmission of conduction electrons between two ferromagnets that sandwich a non-magnetic material. Nowadays, this quantum mechanical magnetoresistance effect is exploited in magnetic field sensors, which are used to read data in hard disk drives, biosensors, microelectromechanical systems and other devices [14].



(a) Parallel ferromagnetic layers alignment.

(b) Antiparallel ferromagnetic layers alignment.

Figure 2.2: Working principle of the GMR effect (adapted from Soares *et al.* [12]).

Figure 2.2 shows the working principle of the GMR effect using stacked layers. The effect occurs whether the magnetization of adjacent ferromagnetic layers is parallel alignment shown in Figure 2.2a or antiparallel alignment shown in Figure 2.2b. Among the various combination of materials used for forming these layers: Co, Fe, NiFe, CoFe and other alloys are used as ferromagnetic layers, while Cr, Cu, Ag, and others are used for the interlayer [15]. In the first case, spin-down electrons have a higher scattering probability than the spin-up electrons creating a lower resistivity channel for spin-up

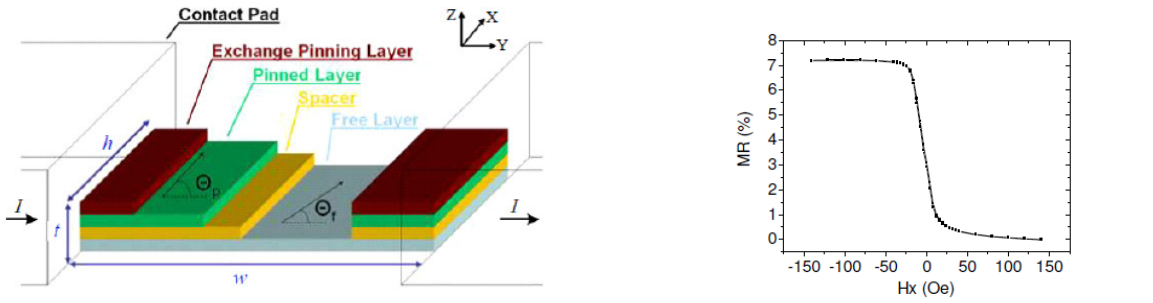
electrons, which lowers the overall resistance of the device. In the second case, both the spin-up and spin-down electrons will have a high scattering probability in the respective ferromagnetic layer with opposite moments generating two channels with the same resistivity. The resistivity of this channel is higher than the low resistance channel of the first case, therefore producing an overall higher resistivity than the parallel state.

A GMR stack is typically composed of several ferromagnetic and non-magnetic layers and has a magnetic response illustrated in Figure 2.1b. The MR_{ratio} of these sensors can amount to 10%.

Spin Valve Sensors

A SV sensor is a device in which the electrical resistance varies within the interval of two values. The SV consists of two conducting magnetic materials (pinned and free layer) with different magnetic coercivities. The resistance change is a result of the GMR effect.

In 1991 Dieny *et al.* [16] introduced the principle of an SV sensor comprising a fixed ferromagnetic layer, called pinned layer, and another ferromagnetic layer free to rotate with the external field. This concept was further developed and tested in 1994 [17]. Nowadays, SV sensors are used in magnetic sensors, hard disk read heads [18], and magnetic random access memories.



(a) Simplied structure.

(b) Experimental transfer curve (MR characteristic).

Figure 2.3: SV sensor features (from *Dr.* Tiago Costa [19]).

The simplified SV sensors structure, illustrated in Figure 2.3a, consists of a copper spacer sandwiched between two ferromagnetic layers, one of which is fixed (pinned) by an antiferromagnet that raises the magnetic coercivity of that layer.

As outlined in the previous section, the electrical resistance is higher when the alignment of the magnetic layers is antiparallel than in parallel. The working principle is based on the GMR phenomenon, and upon sensing a magnetic field with an appropriate strength, the free layer switches polarity, resulting in a resistance change shown in Figure 2.1a. When the maximum magnetic field is applied, the electron spin of both ferromagnetic layers are in the parallel state, and thus the SV sensor resistance has its minimum value of R_{min}. When such a magnetic field is applied that causes the electron spin of both

ferromagnetic layers to be in the anti-parallel state, the SV sensor resistance reaches its maximum value R_{max}. Between these two states, the SV sensor resistance has a linear response with the applied magnetic field [19].

Freitas *et al.* [13] fabricated several SV sensors with different ferromagnetic materials and thicknesses and reported up to 20% MR_{ratio}. One of these sensors with a width of $6\ \mu\mathrm{m}$ and height of $2\ \mu\mathrm{m}$ was used to obtain the MR characteristic illustrated in Figure 2.3b. These dimensions achieved a typical relative value for the MR_{ratio} of around 7%.

2.2 Sensor Front-End Interfaces

The MR sensors are resistive sensors that change their resistance according to a magnetic field. To obtain these resistance values and translate them to meaningful information, an analog interface is fundamental to bias the sensors, amplify their signal and perform other required functions.

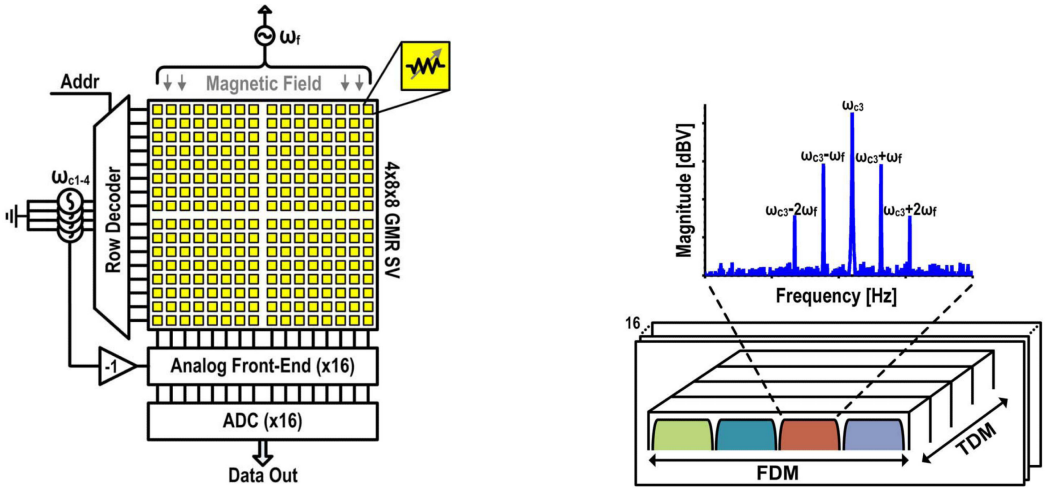
Over the last decades, the front-ends have benefited from technological advances to be a low-cost and versatile interface for resistive sensors offering both a wide operative range and robustness to component and power supply variations. The result is a simple, compact, low-cost, low-voltage and low-power solution [20].

The type of resistance variation of the sensor follows two different paradigms. In the first measurement paradigm, the resistance variation of the sensors can last for several decades [21]. Where the interface, depending on the type of application, must have: a high dynamic range and precision for the entire range [21, 22]; a increased throughput for very high resistance values [23]; temperature gradient control [24]; auto-scaling scheme [25]; reduced power consumption [26]; among other features. The second measurement paradigm is related to the minimum detectable resistance variation that the interface can recognize for a given resistive sensor. The SV sensors are a great example because they can measure weak magnetic fields and thus may produce signals with low intensities ($\mu\mathrm{V}$). Therefore, when designing a front-end interface for this type of sensor, it is crucial to ensure that the interface noise remains below the level of the sensor noise. This ensures that the SNR is not compromised or diminished.

2.2.1 Work from Hall *et al.* at Stanford University

The team Hall *et al.* [6] were aware that the future of medical diagnostics lies within magnetic nanotechnologies. It has proven potential in several nanomedicine areas like imaging, therapeutics, and early disease detection. The advancements in nanotechnology promote new transducers with the same size scale as biomolecules, using electronic detection instead of the typical optical molecular tests. However, to achieve this end, novel biosensing interfaces are required to make this transition possible.

Hall *et al.* project presents a quantitative platform that uses magnetic immunoassays coupled with an array of magnetic biosensors and an integrated data acquisition system. It performs high-sensitivity electronic molecular tests enabling quantitative proteomic analysis, following a similar working principle as the system in this dissertation by detecting with MR sensors Magnetic NanoParticles (MNP) attached to the analytes.



(a) Architecture of the MR sensor system.

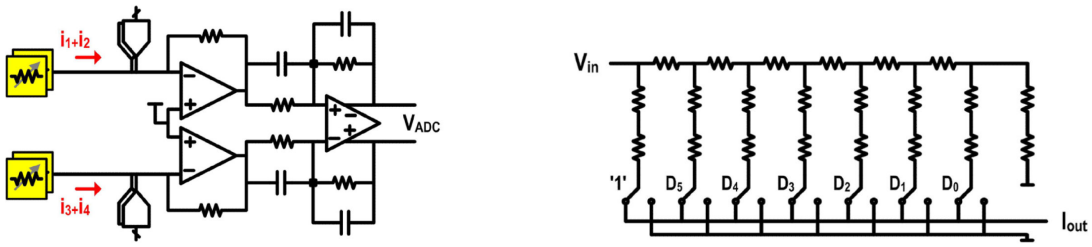
(b) FDM spectrum and principle.

Figure 2.4: SV sensor interface (from Hall *et al.* [6]).

Figure 2.4a depicts the organization of the MR sensors within the interface, composed of four sub-arrays, each with an 8x8 Two-Dimensional (2D) matrix of SV sensors. The sensor array exceeds in mitigating the 1/f noise component of MR sensors by modulating the signal and applying an Alternating (AC) magnetic field (w_f) to excite the MNPs and an AC voltage ($w_{c_{1-4}}$) to bias the sensors. The system is composed of a decoder that selects a particular row of the sensors that are readout in parallel by column level Analog-to-Digital Converter (ADC)s.

The sensor array has a total of 256 individually addressable sensors MR sensors. Usually, in large arrays, Time-Division Multiplexing (TDM) is used to scan each sensor. However, this project uses 16 parallel readout channels and an Frequency-Division Multiplexing (FDM) to reduce the readout time due to the adopted signal modulation scheme. As shown in Figure 2.4b, the FDM is performed by biasing each of the four sub-arrays with a different carrier frequencies ($w_{c_{1-4}}$) and summing the resultant MR sensor currents. The spectrum tone at w_c, the carrier tone, is due to the non-magnetoresistive portion of the sensor, whereas the side tones at $w_c \pm wf$ result from the magnetoresistive component. Additionally, the signal baseline ratio is improved by extracting the side tones (magnetoresistive component) of the signal.

The Analogue Front-End (AFE), in Figure 2.5a, is implemented by two differential Transimpedance Amplifier (TIA)s followed by a fully-differential ADC driver. The split architecture optimizes each amplifier



(a) Readout channel with carrier suppression.

(b) R-2R ladder for carrier suppression.

Figure 2.5: Analog front-end schematic (from Hall *et al.* [6]).

separately, using the TIA low noise and high linearity and the high speed of the ADC driver. The TIAs process the current from two of the four sub-arrays and use a carrier suppression technique to increase the dynamic range. The four Digital-to-Analog Converter (DAC)s at the input of each TIA, corresponding to the four different carrier signals ($w_{c_{1-4}}$), attenuate the non-magnetoresistive component, which provides no information regarding the measurement. The DACs topology, depicted in Figure 2.5b, is a 7-bit R-2R ladder with the most significant bit tied to logic one.

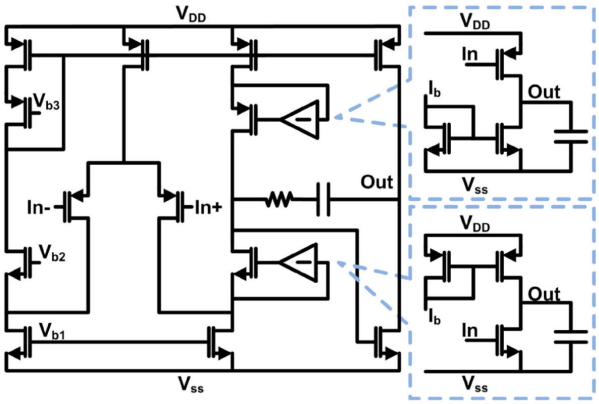


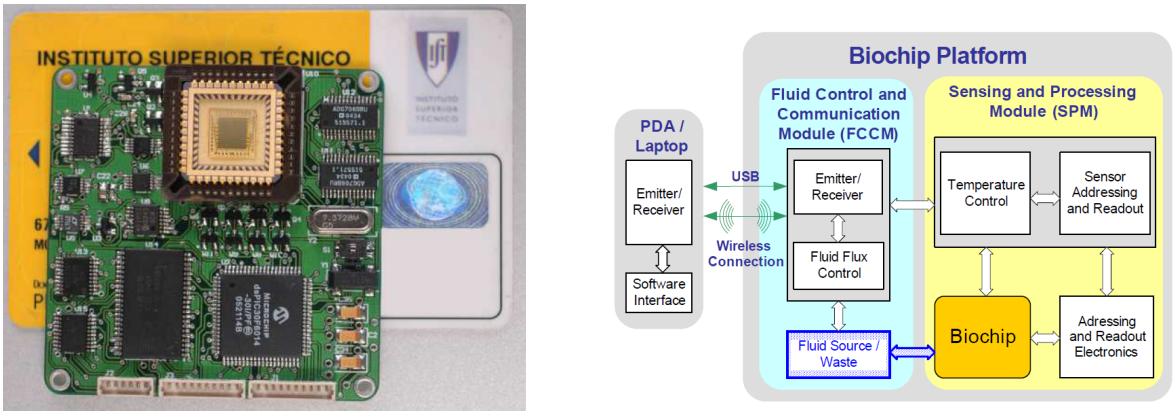
Figure 2.6: Transimpedance amplification stage with carrier suppression and gain-boosters (from Hall *et al.* [6]).

Figure 2.6 illustrates the schematic of a TIA, implemented with a two-stage folded-cascode amplifier with gain-boosting and resistive feedback. The system uses pseudo-differential instead of fully-differentials TIAs because it would add too much 1/f noise or require too much area. The closed-loop gain is established by resistive feedback, and the gain-boosters are implemented with common-source amplifiers.

2.2.2 Work from Germano *et al.*

Germano *et al.* [27] developed a microsystem for biomolecular recognition (e.g. enzymes) based on a biochip. The biochip follows the same principle of this project. It uses high sensitivity sensors to detect

magnetically tagged biomolecules. The microsystem provides the electronic circuitry to address and read the MR sensors, based on an MTJ, organized in a 2D array. The developed prototype (Figure 2.7a) with credit card dimensions has all the required electronics to address, read and sense the sensors, besides controlling the temperature and the microfluidics chamber.



(a) Prototype: main board.

(b) Platform architecture.

Figure 2.7: Microsystem for biological analysis (from Germano *et al.* [27]).

The platform architecture, depicted in Figure 2.7b, is organized into two main modules: the sensing and processing module; and the fluid control and communications module. The first module directly interacts with the array of biosensors. It is responsible for addressing and reading the sensors and monitoring the temperature in different sub-areas of the chip. The second module, fluid control and communications, is the interface between the external world and the biochip platform. The architecture is flexible and reliable, including wired (Universal Serial Bus (USB) protocol) and wireless (Bluetooth technology) communication. This module also controls the fluid that carries the magnetically tagged biomolecules. The interface between the user and the portable system is through a handheld analyzer that allows a user-friendly interaction and provides the performed biological measures.

Since the MTJ sensors are passive elements, they require a biasing structure to supply the necessary current. The current generator circuit in the biochip uses a DAC and a voltage-to-current converter, as demonstrated in Figure 2.8.

The output voltage of the 10-bit DAC is converted to current, through a non-inverting amplifier topology, with a Bipolar Junction Transistor (BJT) (Q_{feed}) and a resistor (R_1). The current mirror assures that the converted current injected into the sensor and the reference sensor has equal value. The degenerated current mirror replicates the same current value through the different branches if the degenerating resistances (R_e) have the same value. These R_e resistances also introduces negative series-series feedback and increase the circuit output impedance improving the circuit operation. This topology reduces the current errors introduced by the current mirror and the feedback transistors, but the offset

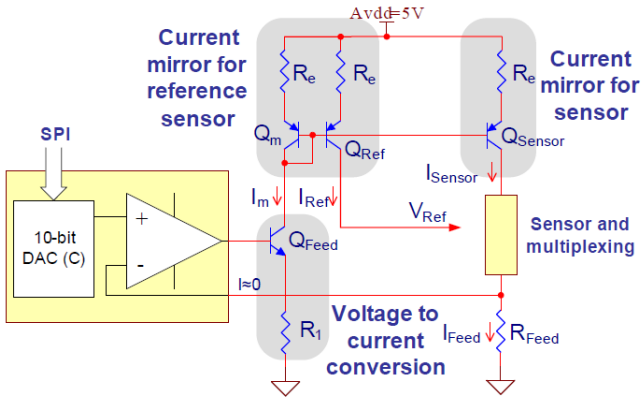


Figure 2.8: Current generation circuit (from Germano *et al.* [27]).

error of the op-amp remains.

The MR sensors arranged in a 2D array (16x16) are addressed based on a multiplexer and a commutating matrix of integrated diodes, acting as a switch. The microcontroller is responsible for addressing a single element, providing the row and column of the desired sensor to be read. The addressing requires two multiplexers (row and column) to establish a single current path that includes the demanded sensor. Figure 2.9 depicts the explained addressing architecture.

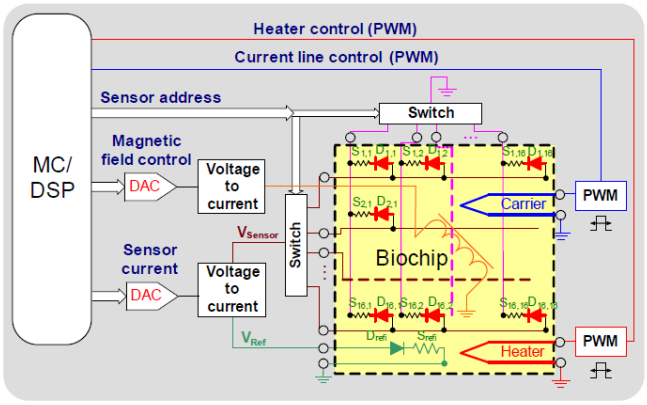


Figure 2.9: Addressing and sensor drive (from Germano *et al.* [27]).

The biochip also included several heaters placed in different chip areas to control the temperature using Pulse Width Modulation (PWN) signals. It also has carrier lines to guide the target biomolecules over the magnetic sensor. The signal response of the MR sensors can be measured by reading the voltage drop at V_{sensor} in Figure 2.9. This voltage is measured using the conditioning circuit in Figure 2.10.

Figure 2.10 illustrates the diagram of the sensor readouts. The signals connected to the amplifier stage are defined using two switches. This circuit can provide several measurement types, including

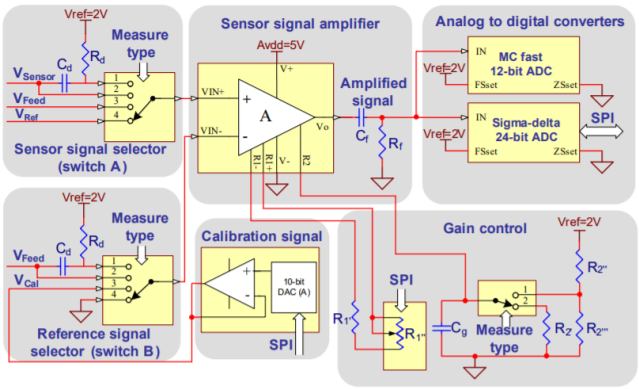


Figure 2.10: Circuit diagram of the sensor reading (from Germano *et al.* [27]).

calibration measurements, with two different resolutions/speeds and controllable gain [27].

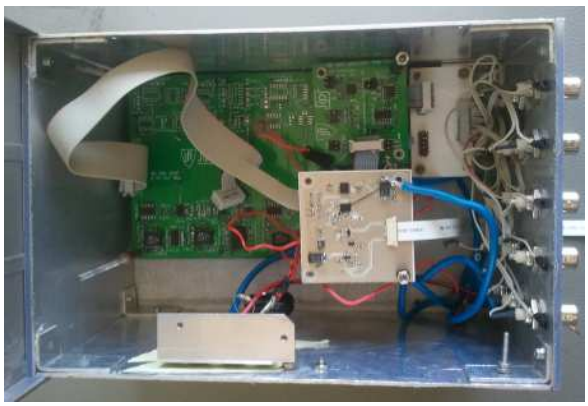
The amplified signal is converted to the digital domain with a sigma-delta converter or a faster successive approximation ADC. The signal information is transmitted to the microcontroller through a serial peripheral interface. The gain control circuit controls the sensor's temperature by adjusting the amplifier gain stage and, therefore, the sample acquisition time.

2.2.3 Work from Costa *et al.*

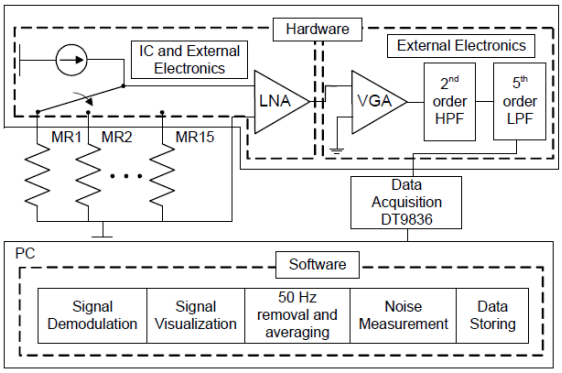
The research team, Costa *et al.* [28], developed a neural signal detector for biologically generated magnetic fields. The system purpose is to record the magnetic field generated by ionic currents. It measures the voltage generated by the flow of ionic currents due to neuronal interactions [29], providing valuable information regarding how neurons interact. The system electronics include an ultra-low noise Direct (DC) or/and AC source to bias the MR sensors and the amplification and filtering circuit for the resulting signal.

Figure 2.11a represents the prototype of the instrumentation system used in this project. The system includes three different boards: the current source and pre-amplifier, variable gain amplifiers and filters, and control board. The current source and the pre-amplifier provide the necessary current for the MR sensors to generate a weak amplified signal in response to the neuronal signal. The variable gain amplifiers and filters perform the remaining amplification and remove unwanted components. The control boards allow for a manual configuration of the amplifiers and filters of the system.

The instrumentation system follows the architecture presented in Figure 2.11b by a block diagram. The system is composed of hardware and software parts. Although, only hardware, the pertinent topic in the scope of this dissertation, will be approached in detail. The developed front-end includes a current source to bias the MR sensors and an ultra-low noise AC coupled instrumentation amplifier to intensify the signal response of the sensors. Furthermore, it has a variable gain amplifier, a 2nd order HighPass



(a) Instrumentation system prototype.



(b) Block diagram of the system architecture.

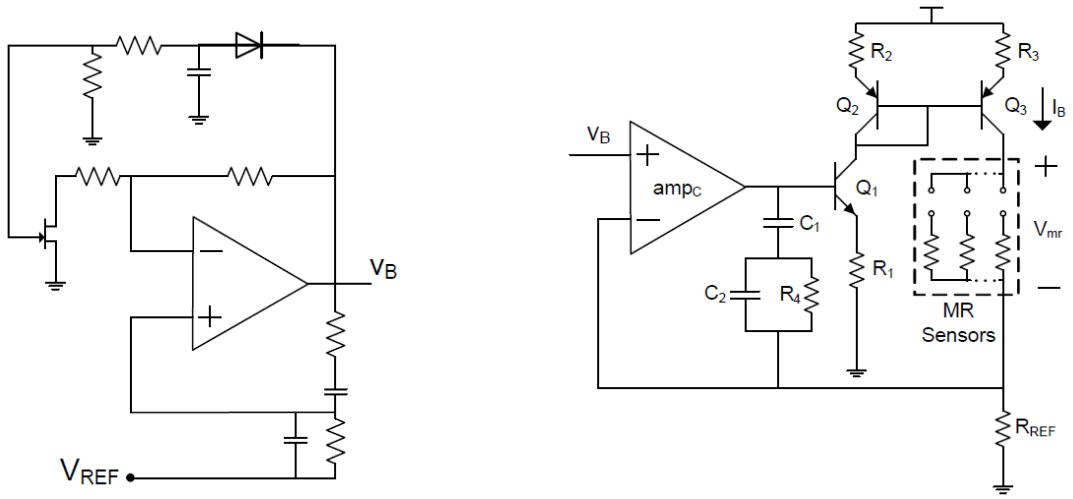
Figure 2.11: Neuronal signal detector for biological generated magnetic fields (from Costa *et al.* [28]).

Filter (HPF) and a 5th order LowPass Filter (LPF) to amplify and limit the measurement bandwidth. The analog data is converted to digital using an ADC, and it is the channel between the interface and the computer with the software implemented in MATLAB. The software allows the visualization and storage of the measurement signals.

The neuronal measurement with the MR sensor follows this principle. A brain slice stimulated with an electrode generates action potentials due to neuronal activity at the tissue surface. These action potentials lead to ionic currents that produce magnetic fields. The MR sensors detect this magnetic field, and the measurement is performed by biasing the sensors with a current and converting their resistance change into a voltage. However, the capacitive coupling between the brain and the MR sensors induce an undesired voltage that masks the signal generated in response to the ionic currents. Biasing the sensors with a DC+AC current enables an amplitude modulation scheme that distinguishes the coupling voltage. The voltage variation due to neuronal magnetic interaction will appear in the baseband and around a specific frequency, whereas the coupling voltage is only present in the baseband.

The biasing current source, presented in Figure 2.12b, is based on a typical voltage regulator structure with negative feedback with a current output. A voltage DC or DC+AC is applied to the ultra-low noise amplifier (amp_c) that, due to negative feedback, ensures the current I_B, and the voltage drop on R_{REF} equals V_B. As mentioned before, to filter the coupling voltage, the V_B voltage must have an AC component generated by the circuit in Figure 2.12a. The schematic represents a typical Wien bridge oscillator, using a low noise rail-to-rail amplifier. This type of oscillator is known for having a BandPass Filter (BPF) (HPF followed by LPF) Resistor–Capacitor (RC) network in the feedback loop. A buffered voltage divider from the power supply generates the voltage V_{REF}.

Figure 2.13 depicts the amplification and filtering block diagram. The amplification has two stages, an ultra-low noise instrumentation amplifier ($\mathrm{AD8429}$) and a variable gain instrumentation amplifier ($\mathrm{AD8231}$). The typical neuronal signal is in the $\mu\mathrm{V}$ range. However, it can have a higher amplitude.



(a) Wien bridge oscillator for DC+AC current generation.

(b) MR sensor biasing current source.

Figure 2.12: Biasing schematic (from Costa *et al.* [28]).

The 2nd stage amplifier has a variable gain to prevent system saturation. The 1st stage amplifier is an ultra-low noise to decrease the next stage impact on the SNR of the measurement. The 2nd order HPF (LMF100) reduces the flicker noise, whereas the 5th order LPF reduces the high-frequency noise.

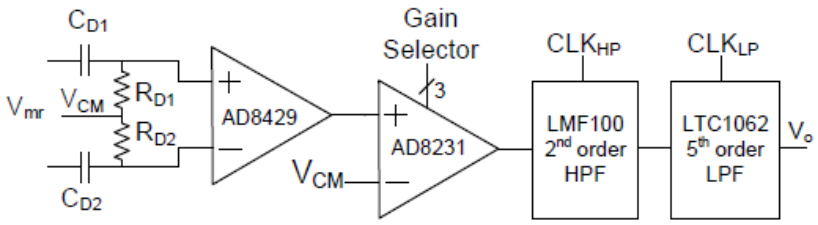


Figure 2.13: Variable gain amplifier and bandpass filter block diagram (from Costa *et al.* [28]).

Neuronal applications such as this one require a measurement system with a high spatial resolution. The instrumentation system described can measure signals from a maximum of 16 sensors if there are 16 current sources designed. Hence, the research team from INESC is developing new biasing and amplification circuit to allow scaling the number of sensors. The enhancement of the system with a high spatial resolution, and immunity to external interference's, is being pursued to tolerate high-density neuronal measurements.

2.2.4 Work from Caetano *et al.*

This dissertation purpose is to improve the system implemented by the Caetano *et al.* research team. The work disclosed in this sub-section is developed on top of previous efforts done by a multidisciplinary

research team from INESC-MN and INESC-ID. This team was composed of Dr. Diogo Caetano, Eng. Rita Soares, and Eng. Ruben Afonso.

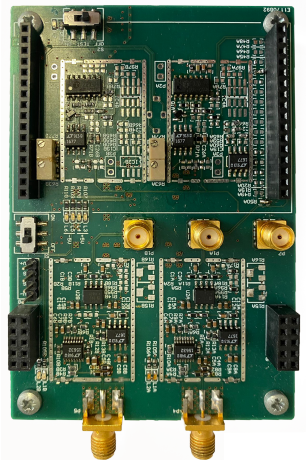


Figure 2.14: Cytometer platform designed by Eng. Ruben Afonso.

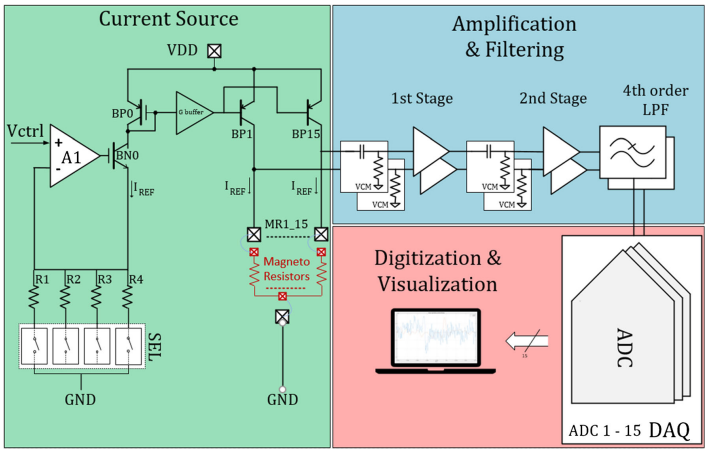


Figure 2.15: Schematic representation of the electronics for sensor biasing and signal acquisition used in MFC experiments (from Soares *et al.* [12]).

The system for the Magnetic Flow Cytometry (MFC), presented in Figure 2.15, consists of three main sections: sensor biasing, signal amplification, and digitalization. In the biasing section, the output of the amplifier (A_1), established by a control voltage (V_{crtl}), is converted to current through the transistor B_{N_0} and the R_{1-4} resistances. The current mirror, performed by B_{P_0} and $B_{P_{1-15}}$, assures that the converted current injected into all the sensors has the same value (I_{ref}). The signal amplification and filtering section comprise two AC coupled amplification stages followed by a 4th order anti-aliasing LPF. This section takes the most space out of the board because each MR sensor requires signal amplification and filtering circuitry. The digitalization section uses a Data Acquisition (DAQ) board, limiting the number of sensors to 15, which digitizes and multiplexes the analog inputs and allows to store the signal in a computer. Dr. Diogo Caetano also developed a script to process the raw signal data. The conceived script consisted of additional signal filtering, signal subtraction between a reference sensor with mismatch estimation, and the application of heuristics to select candidates to be identified by a machine learning algorithm.

Figure 2.14 showcases the current MFC platform developed by Eng. Ruben Afonso. This board features two analog channels consisting of a biasing architecture with an open-loop topology and an amplification scheme. The analog channels were meticulously designed using discrete electronic components selected specifically for their intended purpose. In addition to the analog channel, the board incorporates a saturation detector in the 1st stage of amplification and a power supervisor circuit. However, the saturation detector does not perform as expected when the saturation time is short. Eng. Ruben Afonso also designed two additional PCBs that can be attached to the platform: one for the detection of magnetic field changes using SV sensors, and another for DAQ purposes. Overall, Afonso's

work has yielded a compact and modular system.

Caetano's work was perfomed on the previously explained prototypes, consists of techniques to interface the MR sensors. The developed and designed techniques improve the extraction of reliable information according to the specific application in the scope of biomolecular recognition. The developed AFE consists of an adapted architecture from Germano *et al.* [27] built on a platform implemented by Costa *et al.* [28]. *Dr.* Diogo Caetano work is focused on an AFE for non-destructive tests and the digital signal processing for the MFC.

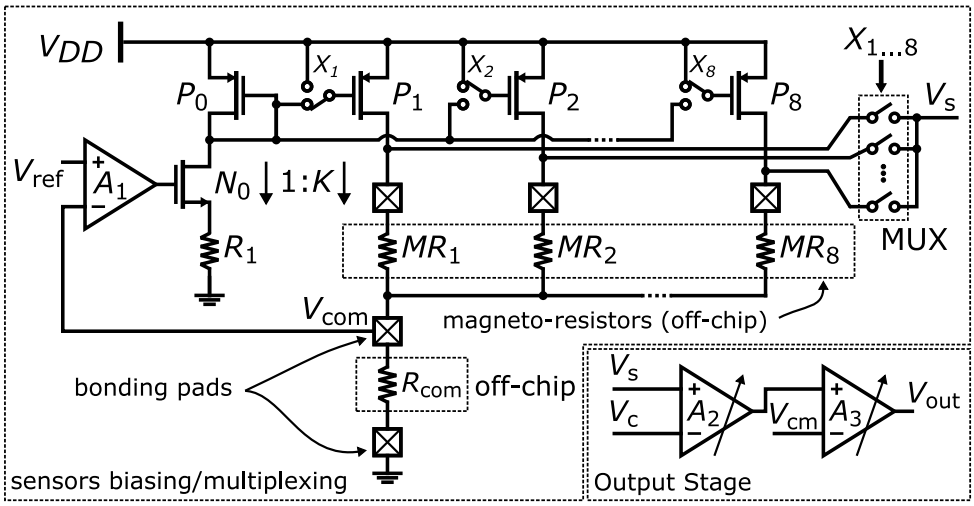


Figure 2.16: Schematic representation of the electronics for sensor biasing and simplified output stage used in non-destructive tests experiments (from Dr. Diogo Caetano [30]).

The biasing topology, shown in Figure 2.16, used in the non-destructive tests system, has a similar working methodology as the previous system (Figure 2.15). The interface bias the sensors with current and reads their response in voltage. The biasing current, controlled externally by V_{ref}, is converted to current with the transistor N_0 and the resistance R_1. The current mirror feeds all the sensors with the same current value. To do so, the transistor P_0 converts the current back to voltage, and the transistors P_{1-8} convert the voltage into current to mirror it to all sensor branches. The MR sensors change their resistance proportional to a magnetic field, resulting in the V_s voltage signal. The sensors are addressed individually using a multiplexer controlled by the inputs X_{1-8}. The major difference between Figure 2.15 and Figure 2.16 systems is the feedback loop. Non-destructive tests system has sensors inside the feedback loop (closed-loop). Unlike the MFC system, which is an open-loop with the sensors outside the feedback loop. The closed-loop approach provides an improvement in the noise, as most of the noise introduced by the circuitry is reduced by the amplifier. However, the disadvantage of this loop methodology is that it is more difficult to stabilize.

2.3 Discussion

In this chapter, the concept of MR sensors was explored, specifically focusing on SV sensors, which will be utilized in this project. MR sensors are designed to detect and measure changes in magnetic fields by utilizing the magneto-resistive effect. Several platforms have been developed to interface with MR sensors, enabling accurate and reliable measurements. By leveraging the advancements in MR sensor technology and the design of these interface platforms, this work aims to achieve a precise and efficient magnetic field detection and measurement system.

MR sensor is a broad term for devices designed to sense magnetic fields. Their resistance value change in the presence of a magnetic field. This project will take advantage of SV sensors that are based on the GMR effect. In the comprehensive review by the INESC-MN research team (Soares *et al.* [12]), out of the thirty-one related works: twenty used GMR sensors (SV and GMR stacks); four used hall sensors; and six used TMR, coils, or giant magneto impedance sensors. The multilayers GMR sensors have the best compromise between noise, signal, and fabrication simplicity. Another important feature when developing an interface for them is the ease of biasing and obtaining their response, either in AC or DC mode. To support this, *Dr.* Diogo Caetano's work [30] compared the SV sensors with the MTJ, which use the TMR effect. On the one hand, he concluded that in noisy environments, MTJs tend to perform better [31–34] as they produce more signal per unit of field but have a more considerable noise. On the other hand, in very low-signal and low-noise applications, SVs generate less noise, so they are used more often [12, 35–38]. In summary, it is clear that biomolecular recognition applications are driving SV sensors development. Yet, there is also a growing number of other applications, such as flow cytometry, neuronal magnetic recording and non-destructive tests based on eddy current.

The AFE interfaces are crucial to obtain the resistance change in the MR sensors and translate them to meaningful information according to the application. Usually, the interfaces integrate the full analog path, from sensor biasing to signal digital conversion. Nevertheless, noise is one of the fundamental considerations, common through all interfaces that serve different applications. It is clear that MR sensors have a huge potential in several applications, but it is crucial to develop ultra-low noise interfaces according to the application specifications. This chapter detailed four AFE prototypes, three of them conceived in INESC. The interfaces that Hall *et al.* [6] and Germano *et al.* [27] created were within the scope of biomolecular recognition applications. As opposed to Costa *et al.* [28] and Caetano *et al.* [12, 30], which focused on flow cytometry applications.

The examination of these cutting-edge prototypes has provided valuable insights for this thesis. Germano *et al.* work introduced an intriguing concept of utilizing a DAC to supply the reference voltage required by the biasing architecture. This concept allows for a easy adjustment of the biasing current without electronic expertise. This feature is particularly advantageous for this multidisciplinary project. Moreover, Dr. Tiago Costa, followed by Dr. Diogo Caetano, initiated studies on a novel biasing topology

where the sensors are placed inside the feedback loop. This innovative topology holds the potential to significantly reduce the noise introduced by the cytometer platform. Eng. Ruben Afonso laid the groundwork for the MFC system using discrete electronics. However, there is still room for improvement in the current system. To address this, the work presented in this thesis aims to develop an enhanced version of the system with additional debugging tools for comprehensive analysis and optimization.

3

Magnetic Flow Cytometry

Preamble

This chapter provides an in-depth examination of flow cytometry, focusing specifically on magnetic flow cytometry. The working principle of magnetic flow cytometry will be elucidated, accompanied by an exploration of its practical requirements. Furthermore, the system employed for magnetic flow cytometry will be introduced, highlighting the assigned role within this work. Additionally, the integration of the developed ultra-low noise platform into the system will be discussed, ensuring adherence to a specific set of specifications for optimal performance and precise analysis in magnetic flow cytometry.

Contents

3.1 Flow Cytometry

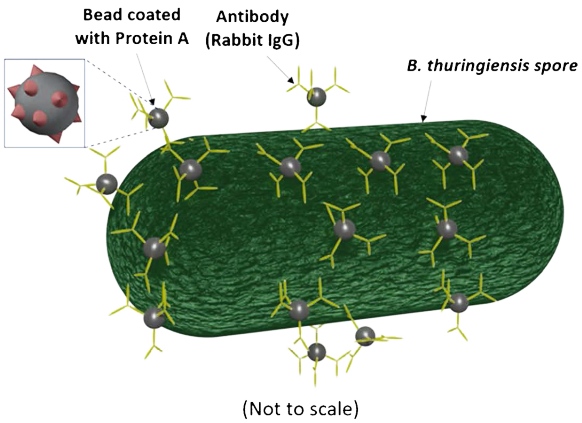
Flow Cytometry (FC) is a technology that provides rapid multi-parametric analysis of single cells in a solution [39]. It is a type of automated cell cytology. Cytology is a branch of biology that studies the origin, structure, functions, multiplication, pathology and history of cells. FC is used in several applications to count, sort, and characterize cells while analyzing thousands of particles per second. The FC original concept is composed of three systems. Firstly, the flow system, where the injected cells flow through a fluidic channel. Secondly, the optical system, represented by the lasers that act as light sources to produce both scattered and fluorescent light signals. Thirdly, the electronic system to process and obtain the resulting signal, composed of detectors such as photodiodes or photomultiplier tubes. However, this work will use a different FC principle – MFC, based on magnetic fields instead of light sources.

Throughout the past years, and encompassing several areas of expertise, INESC-ID and INESC-MN research teams have developed a magnetic-based cell cytometer. The magnetic flow cytometer counts cells marked with magnetic particles when they flow near the MR sensors.

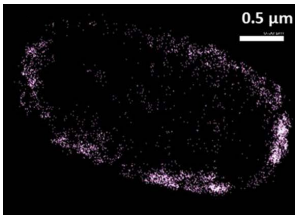
3.2 Working Principle

The MFC, just like FC, is a single-cell analytical tool used to characterize immune cell phenotypes to monitor solid tumours, haematological malignancies, minimal residual disease or metastatic progression [39]. The FC principle, as explained before, uses lasers as light sources to produce both scattered and fluorescent light signals read by detectors such as photodiodes or photomultiplier tubes, unlike the MFC, where the excitation source is from a magnetic field like a permanent magnetic or a coil. This project uses SV sensors, explained in Section 2.1. Besides this, in the MFC principle, since the cells do not have a magnetic nature, magnetic markers have to bond with the analyte, generating a magnetic field near the permanent magnet. This section explains the working principle of the MFC and how it will influence the analog interface for the MR sensors.

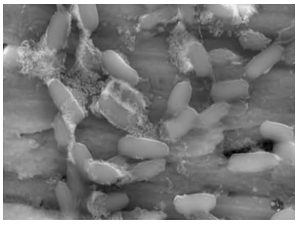
The biological entities in the MFC detection system, cells within a blood sample, have a non-magnetic nature and are thus invisible to the magnetic sensors. Therefore, it is required to bind the analyte with several MNP. Figure 3.1a illustrates the labelling process, to attach particles to the analyte it is required a ligand molecule, to make the bridge between the magnetic particle and the outer surface of the cell. The ligand molecule edges bear different affinities: the magnetic bead coated with protein A bonds to the tail of the antibodies, leaving the head free to attach to specific markers on the membrane of the targeted cell (*thuringiensis* spore on Figure 3.1a). The bonding process has different efficiency rates, depending on the size of the magnetic label. Figure 3.1b represents a high fluorophore labelling efficiency as evidenced by the homogeneous cover on the antigen's surface. Unlike Figure 3.1c, which has a low labelling efficiency, the MNPs are aglomerated in specific regions instead of covering the bacteria.



(a) Schematic of a bacterial spore labeled with immunomagnetic nanoparticles.



(b) High labeling efficiency.



(c) Low labeling efficiency.

Figure 3.1: Cell labeling (from Soares *et al.* [12]).

There is always a constant requirement for the MFC detection system, which is efficiency. The MR sensors' signal depends on the amount of MFC on the cell's surface. The MFC system has a dynamic range, which is the range between the lower and higher boundaries of the sensor detection. The MR sensor response is proportional to the average fringe field generated by the MNP in the sensor area. Undoubtedly, a high labelling efficiency is desirable in this quantitative analytical detection mode. The research team from INESC-MN, Freitas *et al.* [35] strove to choose or create the correct beads and antibodies conjugates. Figure 3.2 illustrates the process of sample preparation.

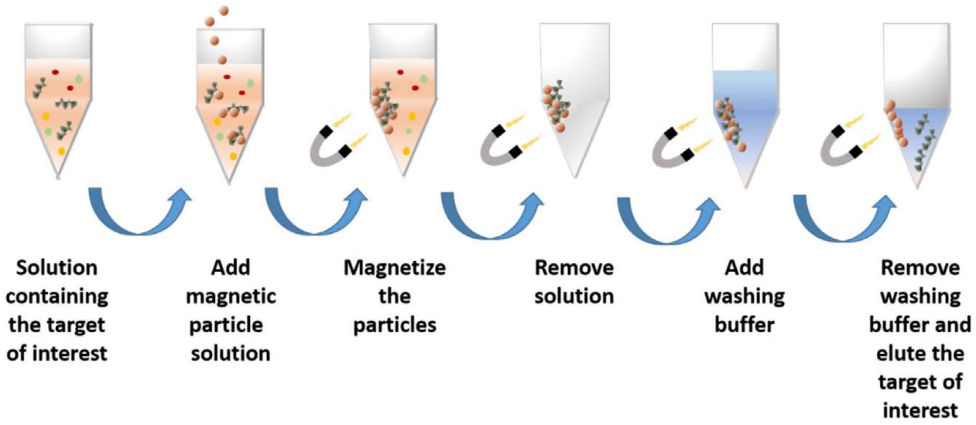
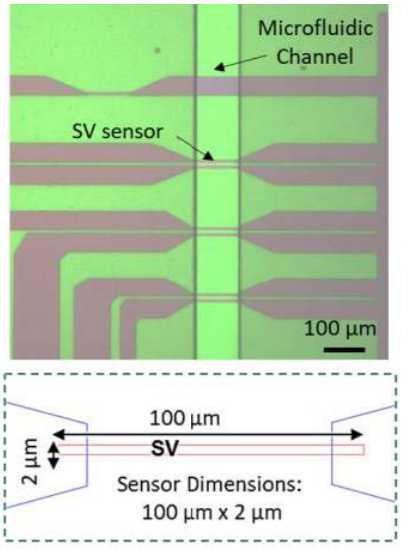


Figure 3.2: Schematic of the standard protocol for magnetic particle-based separation (from Freitas *et al.* [35]).

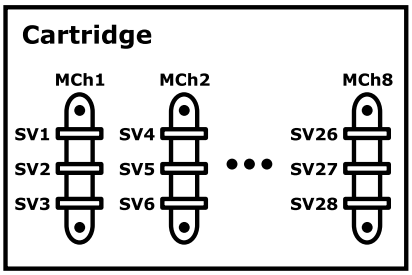
The magnetic particle-based separation, depicted in Figure 3.2, is performed before injecting the sample into the MFC system. The MNPs mixed in a solution containing the target of interest will bond to the specific marker after some incubation time. Then, the tagged particles are magnetized to remove the

original liquid solution. The washing step removes the remaining unwanted molecules because some MNP may remain free in the sample. After this purification process, the resulting mixture is ready to be injected into the magnetic cytometer, more precisely, in a microfluidic channel to perform the assay.

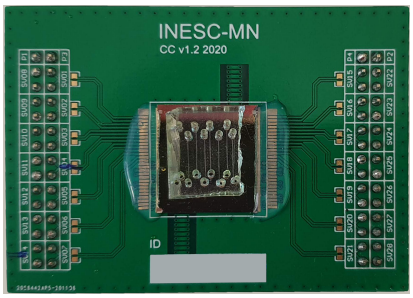
Figure 3.3 shows the chip and PCB containing the microfluidic channels used in this project. The chip designed in Figure 3.3a has four sets of rectangular SV sensors that cover the entire width of the microfluidic channel, defined by the two parallel lines perpendicular to the sensors. Figure 3.3b presents the arrangement of the SV sensors across the microfluidic channels. The PCB, containing the sensors and the microchannels mounted together in Figure 3.3c, represents the disposable cartridge used in the assay. The detection chips are disposable, which means they are discarded after an assay to prevent sample contamination.



(a) Microscopic image of a set of SV sensors aligned with a microfluidic channel (from Soares *et al.* [40]).



(b) Microfluidic channels and SV sensors diagram.



(c) Sensor chip bounded to the microfluidic channels and wire-bounded to the PCB (assay disposable cartridge).

Figure 3.3: MFC system's cartridge.

The detection mechanism in the MFC platform has fundamental guidelines based on the constraints and particularities of in-flow magnetic detection [12]. Figure 3.4 shows the diagram of an interaction between the MNP flowing within a microfluidic channel and the magnetic field sensors. The permanent magnet magnetize the MNPs attached to the analytes and pulls the beads closer to the sensor surface, acting as a vertical magnetophoresis. When in proximity to the sensor, the magnetic field produced by the particles is gradually picked up by the MR sensors [30].

As explained in Section 2.1, the MR sensor's resistance value increases or decreases, depending on the orientation and intensity of the magnetic field. Equation 3.1 describes the resistance change

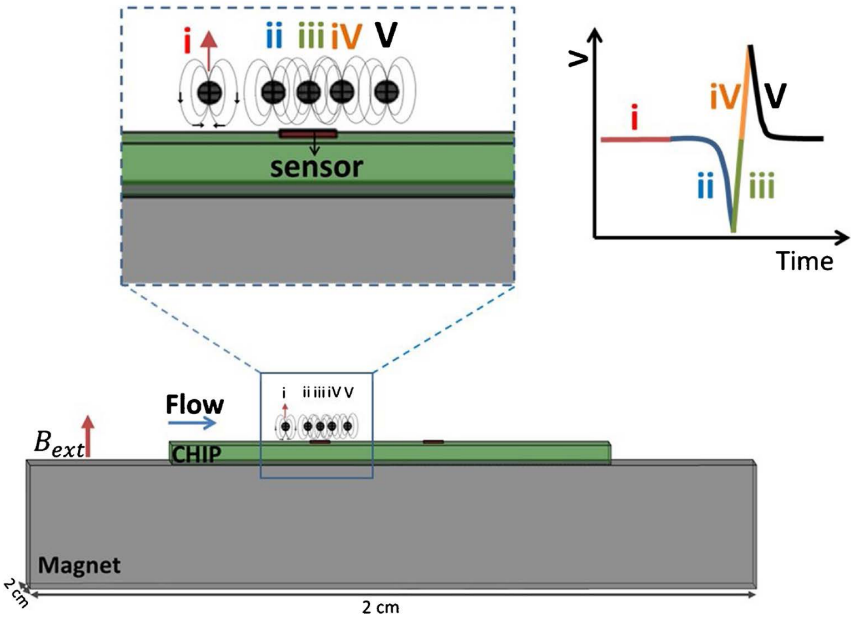


Figure 3.4: Schematic representation of the MFC concept for magnetic particle detection (from Soares *et al.* [12]).

behaviour of the MR sensors.

$$R(H) = R_{NOM} + \Delta R(H) \quad [\Omega] \tag{3.1}$$

Whence R_{NOM} is the sensor's resistance at $0T$ and $\Delta R(H)$ is the field-dependent resistance variation. Considering the target/MNP conjugate behaves like a magnetic dipole, where the vector of field intensity has a different direction "in front" and "behind" the target in the sensor axis [30], ensuing the signal illustrated in Figure 3.4. The interaction between sensors and particles results in a monocycle pulse if the excitation field is perpendicular to the particle. The signal negative flank occurrence before the positive is due to the MR sensors direction axis.

3.3 System Overview

As presented in Section 2.2, the systems that interfaces the sensors usually provide a fully analog path, from biasing to digital conversion. The interface system used in this dissertation brings continuity to a project developed by the INESC research team to support a FC application for early cancer detection. Whom, besides having a fully analog path, also has a fully digital path, from the raw data bitstream to the data measurement visualization.

Figure 3.5 illustrates the block diagram of the MFC system. The interface consists of five main sections: biasing, amplification, filtering, digital conversion and digital signal processing. The biasing structure provides the demanded current for the MR sensors to generate a signal when faced with

a magnetic field. The amplification circuit boosts the low magnitude signal response of the sensors. The filtering increases the signal quality by removing unwanted components or features and using anti-aliasing filters. The ADC, as the name implies, converts the analog signal into a digital representation. At last, the digital processing section enriches the system output signal, easing the event detection process that extracts the necessary information and displays it.

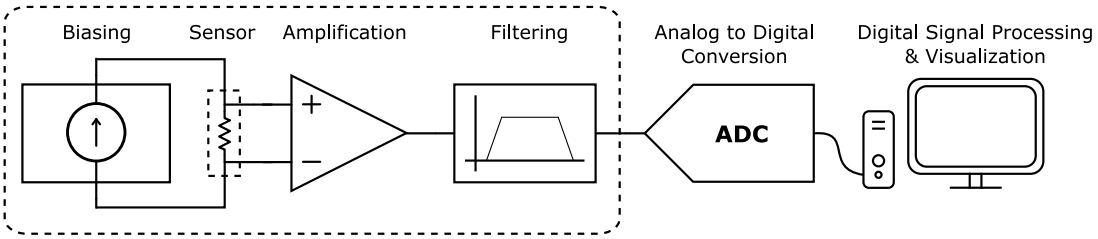


Figure 3.5: Block diagram of the MFC system.

Several master thesis dissertations are being developed concurrently with this work, whose purpose is to improve the different sections that compose this system. The following paragraphs provide a brief explanation of the expected work by each of them.

• Eng. João Faustino is responsible for the ADC and all the electrical circuits that support it. The intention is to research a substitute system (*e.g.* Field-Programmable Gate Array (FPGA)) to the data acquisition board that limits the number of sensors and the sampling rate. In addition to his work, João will implement an oversampling technique while converting the output signal to digital, which ideally will lead to an improvement in the overall SNR and resolution of the system. This section performs the first steps towards event detection, storing the events into a bitstream for preprocessing.

• Eng. Diogo Bernardo work is between the ADC, the digital signal processing and the visualization section. Diogo is researching and implementing advanced methods to improve the SNR using Digital Signal Processing (DSP) methodologies. The idea is to have an independent system performing a real-time analysis of the MFC bitstream output. The computer analysis consists of a machine learning algorithm that improves the success of the application event detection process.

• Eng. Rita Ramos' dissertation thesis focused on the digital signal evaluation and visualization domain, specifically aiming to enhance the accurate detection of magnetically labeled analytes. Her work focused on improving a machine learning algorithm that utilizes neural networks [41]. The purpose of this algorithm was to classify events based on whether they corresponded to magnetically tagged cells or clusters of magnetic particles employed in the tagging process.

The scope of this dissertation, highlighted by a dashed box in Figure 3.5, encompasses all the circuitry involved in the analog path, including biasing architecture, signal amplification, and filtering. Additionally, it marks the initial stages of the digital path. The developed PCB not only serves as an interface for the sensors but also to the acquisition board ADCs and the FPGA. The primary objective

of this work is to significantly reduce the system-generated noise, making the MR sensors the primary source of noise. Moreover, the new ultra-low noise cytometer platform will address several limitations present in the previous platform version.

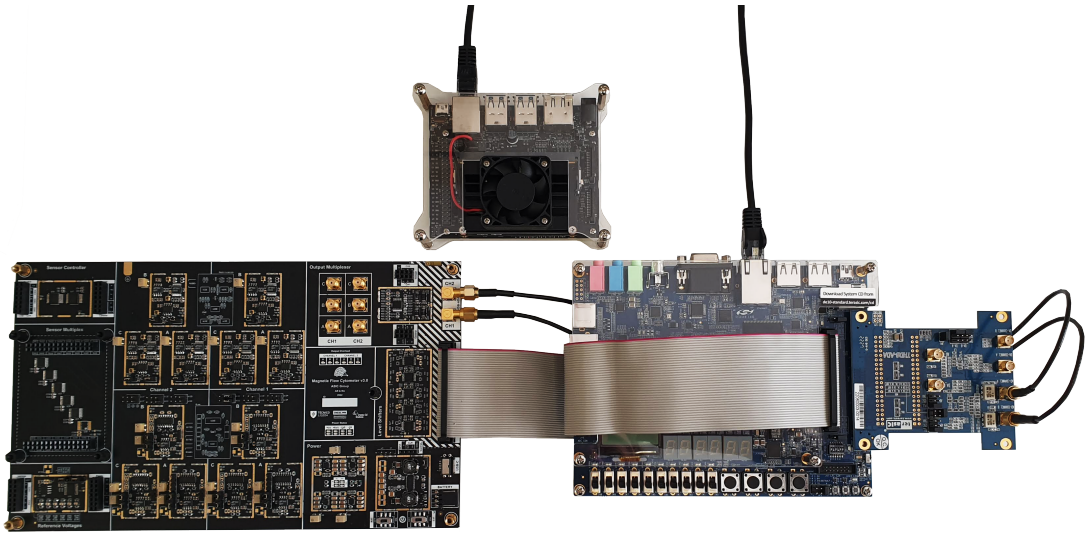


Figure 3.6: MFC system.

Figure 3.6 depicts the various boards comprising the system. The left PCB, distinguished by its black solder mask, represents the cytometer platform developed as part of this work, which will be elaborated upon in the subsequent chapter. On the right, the blue PCB represents the FPGA (DE-10 Standard) and the acquisition board (THDB-ADA) selected by Eng. João Faustino for his project. At the top, the compact computer (Jetson-Nano) serves as the platform where Eng. Diogo Bernardo will execute his real-time machine learning algorithm.

3.4 Interface Specifications

The specifications play a critical role in the design and development of electronic systems. By accurately defining and knowing the specifications, designers ensure the foundation for successful system integration. This section, will delve into the different specifications for the developed interface and explore their impact on the system performance and functionality.

As mentioned earlier, the cytometer platform attaches another PCB (assay disposable cartridge) that accommodates the SV sensor chip through wire bonding. This chip, developed at INESC, incorporates 28 different MR sensors arranged within 8 microfluidic channels. The nominal resistance (Equation 3.1) of these sensors may vary across different batches, with a range of approximately $500\ \Omega$ to $1.5\ \mathrm{k}\Omega$. The biasing circuit, responsible for supplying a current to the passive sensors, must be capable of delivering at least $5\ \mathrm{mA}$ when the sensors have the minimum nominal resistance. However, the circuit must also

account for a potential increase in nominal resistance by at least $1\ \mathrm{k\Omega}$, and ensure a stable current supply. When subjected to a magnetic field, the sensors generate a signal whose frequency primarily depends on the speed of the sample passing through the microfluidic channel. In a study [30] conducted by Dr. Diogo Caetano, it was determined that for accurate flow rate measurements up to $30\ \mu\mathrm{l/min}$, a minimum bandwidth of $100\ \mathrm{kHz}$ is required. Additionally, the sensor response signal typically falls within the range of hundreds of microvolts. To amplify it to volt-level units and ensure maximum dynamic range for the ADCs, the amplification circuit must have a gain of $10000\ \mathrm{V/V}$.

An analog channel in the cytometer platform consists of a biasing circuit, an amplification circuit, and a filtering circuit. A minimum of 3 analog channels are required in the platform. This provides opportunities for experimentation and analysis. For example, utilizing two sensors within a microfluidic channel allows for redundant measurements. If both sensors experience a simultaneous resistance change caused by a magnetic particle, it confirms the presence of a particle rather than external interference. Moreover, including a third sensor in a channel without sample flow, serving as a reference channel, facilitates optimal particle detection by effectively eliminating common noise shared by all three sensors. Therefore, to fulfill this purpose, a minimum of 3 channels and 3 addressable sensors is required.

In addition to the analog path, the digital path of the signal also requires consideration. The DE-10 Standard FPGA, used to control the cytometer and digital signal pre-processing, lacks built-in ADCs. To overcome this limitation, an acquisition module called THDB-ADA is employed. However, this external card poses a significant constraint with only two available ADCs. The ADCs have a sampling rate of $65\ \mathrm{MSPS}$ and cannot tolerate signals exceeding $2\ \mathrm{Vp\text{-}p}$.

Table 3.1: Front-end interface specifications.

Feature	Specification
$\mathrm{R_{sensor}}$	$0.5 \geq \mathrm{R_{sensor}} \leq 1.5\ \mathrm{k\Omega}$
$\mathrm{I_{bias}}$	$\mathrm{I_{bias}}(500\Omega) \geq 5\ \mathrm{mA}$
Bandwidth	$100\ \mathrm{kHz}$
Signal Gain	$10000\ \mathrm{V/V}$
Nº Channels	≥ 3
Nº Sensors	$3 \geq$ Sensors ≤ 28
FPGA	DE-10 Standard
Sampling Rate	$\leq 65\ \mathrm{MSPS}$
Nº ADCs	2
Output Voltage	$\leq 2\ \mathrm{Vp\text{-}p}$

Table 3.1 presents an overview of the specifications discussed. The subsequent chapter will delve deeper into these specifications, exploring their significance and discussing how they were taken into account during the design process.

4

Front-End Interface

Preamble

This chapter provides a detailed examination and evaluation of the circuitry utilized in the cytometer platform. Building upon the shortcomings identified in the previous platform, the current study incorporates innovative features to overcome these limitations. Through extensive testing and evaluation, valuable insights into the enhanced performance and effectiveness of the cytometer platform are obtained.

Contents

4.1 Analog Channel

The MR sensors, as explained in Section 2.1, are a type of sensor that undergo changes in resistance when exposed to a magnetic field. To interpret these fluctuations in resistance values, an analog interface is necessary. This interface plays a critical role in biasing the sensors, amplifying their signal, and filtering out any noise or interference. While the theoretical basis of the AFE interface can be described as the application of Ohm's law, by biasing the sensors with a current and amplification of the resulting voltage, the practical implementation of an ultra-low noise front-end that can handle high sensitivity SV sensors is a challenging task. Proper design and implementation of the analog interface are critical to obtaining accurate and reliable data from MR sensors. Thus, this section will address the discrete electronics of the analog front-end that has been developed.

Electronic system noise can significantly impact the accuracy and reliability of measurements obtained from sensors. The noise can arise from various sources within the electronic system, including the biasing architecture and the first amplification stage. The biasing architecture, in this work, is responsible for providing the appropriate DC current to the sensor, and any noise introduced at this stage directly adds to the sensor's overall noise. On the other hand, the first amplification stage amplifies the sensor's signal response, and any noise present at this stage is also amplified, resulting in an increase in the sensor-referred noise. To mitigate the impact of electronic system noise, proper design and implementation of the biasing architecture and the first amplification stage are critical. Careful consideration must be given to selecting appropriate components and minimizing noise sources, such as by using low-noise amplifiers and properly shielding sensitive components. In addition, advanced signal processing techniques, can be applied to further reduce the noise impact on the sensor measurements. By minimizing the noise and maximizing signal strength, the accuracy and reliability of sensor measurements can be significantly improved.

The block diagram shown in Figure 4.2 illustrates the organization of the channel, which consists of three sub-channels each with three main blocks: sensor biasing, the MR sensor, and signal amplification. The sensor biasing block provides the current required to operate the sensor and converts its output into a voltage signal. The MR sensor block is responsible for sensing the magnetic field which is then processed by the signal amplification block. The signal amplification block is the first stage of signal processing and is responsible, as the name implies, for amplifying the weak signal generated by the MR sensor, increasing its amplitude to a level that can be reliably processed by the subsequent stages.

The bias circuit A has a topology that allows biasing to three sensor branches. Hence, bias circuit A can be considered the master within its channel as it has the capability to utilize sensors from the other sub-channels (B and C). This feature eases the process of testing and comparing different current source topologies to determine the optimal circuit design for the application. However, it is important to note that an amplification circuit is required for each sensor used.

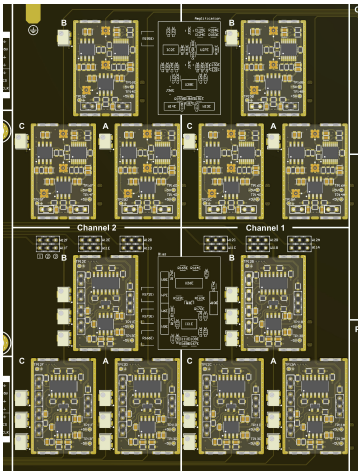


Figure 4.1: 3D view of the PCB with the channels.

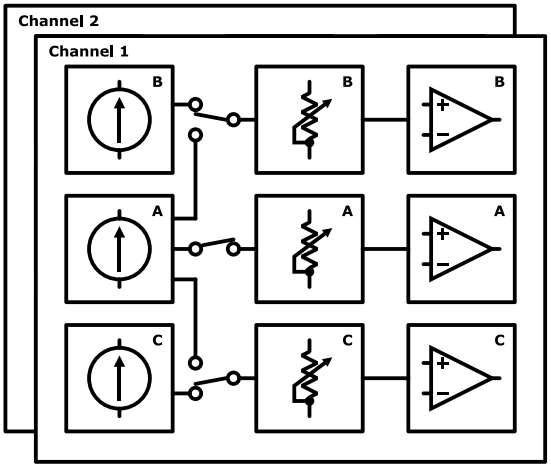


Figure 4.2: Analog channel block diagram (for more details refer to Appendix A).

The size of the PCB area required for the channel is directly proportional to the number of channels needed, as each channel comprises three sub-channels. In this interface, illustrated in Figure 4.1, both channels occupy about 45% of the PCB length. Each sub-channel contains two independent and complex circuits that are connected to the sensor terminals, making it crucial to carefully design and optimize the layout of the PCB to minimize cross-talk and interference between sub-channels. This is particularly important for multi-channel systems, where the presence of noise and interference can significantly affect the accuracy and reliability of the measurements.

4.1.1 Bias Architecture

The SV sensors are passive elements, thus they need to be biased in order to measure their signals effectively. The biasing architecture, as shown in Figure 4.3, is composed of two major circuit blocks: the reference voltage and the biasing topology. While the sensors are shown in the figure for visualization purposes, they will not be discussed in this section. The circuit that supplies the reference voltage is represented at the level of a sub-channel for simplicity, but it will be explained in more detail later in this chapter. The reference voltage provides a stable voltage level that is used as a reference for the biasing topology. The biasing topology, in turn, ensures that the SV sensor is operating in its linear range, where its output signal is most sensitive to changes in the input stimulus, as explained in Section 2.1. By carefully controlling the biasing conditions, the AFE can achieve accurate and reliable measurements of SV sensor signals.

The SNR of the system is largely determined by its biasing architecture and the first amplification stage. The biasing noise directly contributes to the overall sensor-referred noise. While the noise from electrical devices that come after the first amplification stage can be attenuated by the stage gain, the

achieved noise voltage is still considerably high for the application at hand. Therefore, it is crucial to carefully design the biasing and amplification stages to minimize noise and achieve the best possible SNR.

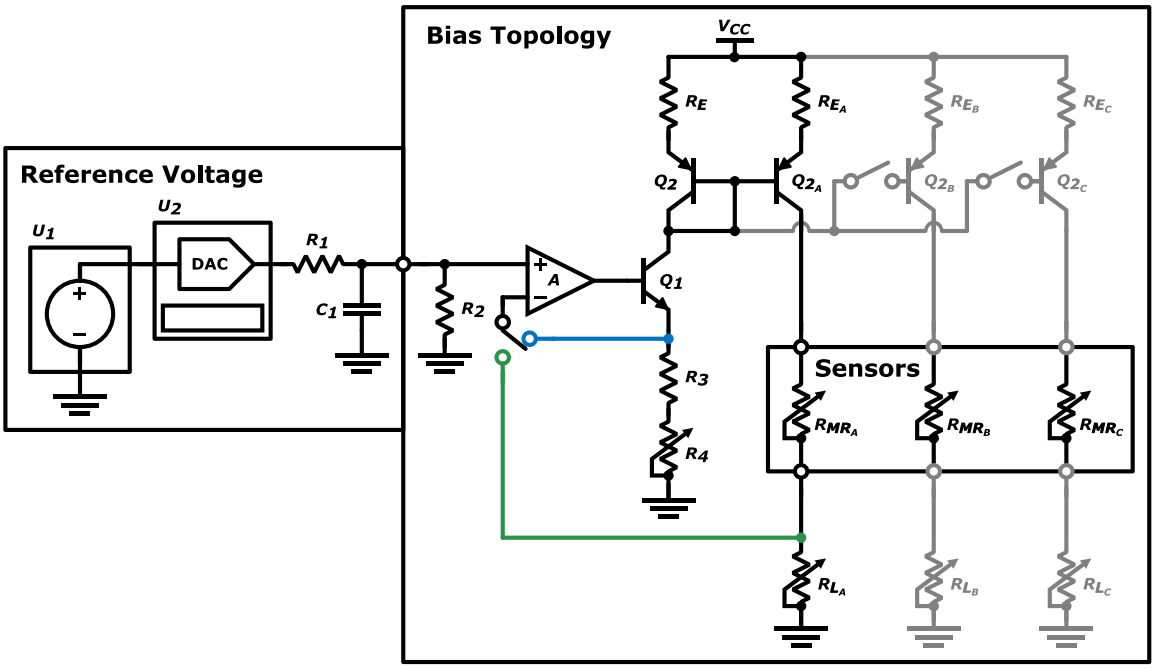


Figure 4.3: Biasing architecture (for more details refer to Appendix A).

The bias circuit was designed to encompass two types of topologies, which differ in the position of the sensor relative to the feedback loop. The blue line topology places the sensor outside the feedback loop, and this is the topology that was used in the previous versions of the cytometer and will be emphasized in this thesis. The green line topology places the sensor inside the feedback loop, which is an alternative that has not yet been proven to reduce the noise but is included in the architecture to enable further investigation of this topology without having to modify the PCB.

Topology with Sensor Outside Feedback Loop

To obtain a signal from MR sensors, a constant current is supplied to the sensors, and the voltage across their terminals is measured. These sensors have a fixed resistance and a variable resistance that changes according to the strength and direction of the magnetic field they are exposed to. By utilizing Ohm's law, the voltage across the sensor's terminals will also change proportionally. By measuring this change in voltage, it is possible to determine the magnitude and direction of the magnetic field being sensed by the sensor (Figure 2.3b). This section discusses the electronic circuit that was designed by previous studies, mentioned in Chapter 2, which produces a constant current output independent of the output load.

The op-amp's high forward gain and differential input design can be utilized to create a nearly perfect

Voltage-Controlled Current Source (VCCS), also known as a voltage-to-current converter. To achieve this, the input voltage that needs to be converted (reference voltage) is applied to the non-inverting input terminal of the op-amp A, as shown in Figure 4.4. The inverting input terminal is connected to one end of resistor R_3 and the emitter of transistor Q_1. The op-amp output (v_{amp}) drives the base of the transistor. Due to the high open loop gain of the amplifier, the base of Q_1 will be forced to the necessary voltage so that v_{ref} is present across R_{cur}. Consequently, the current (i_{bias}) in R_{cur} will only flow in the emitter and also appear in the collector of the transistor Q_1, and its value is given by:

$$i_{sen} = \frac{v_{ref}}{R_3 + R_4} = \frac{v_{ref}}{R_{cur}} \quad [\mathrm{A}] \tag{4.1}$$

In summary, the designed VCCS uses an op-amp circuit with a negative feedback loop and a power transistor to produce an output current, which is proportional to the controlled input voltage v_{ref} and the adjustable loop resistor R_{cur} (Equation 4.1).

After the precision VCCS, this current is mirrored using an emitter degenerated current mirror circuit with transistors. A current mirror circuit replicates or mirrors the current flowing through one transistor (the reference transistor) into one or more transistors (the output transistors). The basic idea behind a current mirror circuit is to make the output current independent of the output voltage by using a feedback loop to adjust the current. Adding a resistor in series with the emitter of the transistors increases the stability and linearity of the circuit. This technique is called emitter degeneration. The resistor will reduce the gain of the transistor, but it also makes the circuit less sensitive to variations in the transistor's parameters. In addition, this technique adds a current mirroring factor that depends on the ratio of the emitter resistors. For this application, the goal is to mimic the current generated by the voltage-to-current converter. Therefore, all of the emitter resistors must have the same value, ensuring that $i_{bias} = i_{sen_{\{A,B,C\}}}$. An emitter degenerated current mirror circuit combines these two concepts. In Figure 4.4 circuit, the collector of the reference transistor Q_2 is connected to a current source (VCCS), and its emitter is degenerated with the R_E resistor. The output transistors Q_{2_A}, Q_{2_B}, Q_{2_C} are connected in parallel with the reference transistor, and their emitter is also degenerated with a resistor (R_{E_A}, R_{E_B}, R_{E_C}). The base of the output transistors is connected to the base of the reference transistor, forming a feedback loop. This loop ensures that the voltage across the emitter resistors of the two transistors is the same, as long as the degenerated resistors have the same value.

The resistor R_2 acts as a pull-down resistor. When the reference voltage v_{ref} is $0\ \mathrm{V}$, which comes from a DAC as illustrated in Figure 4.3, no current flows into the non-inverting input terminal of the op-amp. This can cause the op-amp to saturate and potentially damage the circuit downstream. Therefore, R_2 ensures that, in this situation, the non-inverting input is always connected to a low voltage, preventing the op-amp from saturating. Additionally, it is good practice to include an input resistor to account for the op-amp's leakage currents.

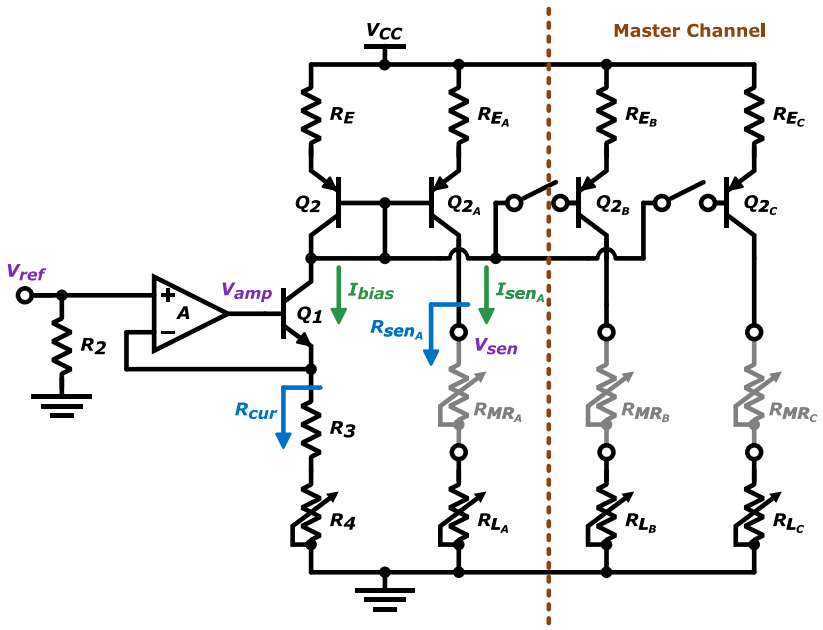


Figure 4.4: Biasing topology where the sensor is outside the feedback loop (for more details refer to Appendix A).

Eng. Ricardo Lorena conducted a study in his master's thesis [42] where he investigated the bias noise in a circuit using the same topology as the one under discussion. The study focused on the effects of different emitter resistance values on the circuit's noise performance. Through careful experimentation and analysis, he determined that the optimal emitter resistance value was $1\ \mathrm{k}\Omega$. This finding was significant because it demonstrated that the choice of emitter resistance can have a notable impact on the circuit's overall noise performance. However, at the time of the practical and theoretical analysis performed in this chapter, Eng. Lorena's work had not yet established the optimal value of the emitter resistance. Therefore, the values of R_E, R_{E_A}, R_{E_B}, and R_{E_C} resistances were all set to the value of $150\ \Omega$ as used in other projects presented in Chapter 2. Nevertheless, all noise measurements discussed further in the document were obtained using the optimal value of $1\ \mathrm{k}\Omega$, as established by Eng. Lorena's research.

To ensure that the circuit generates the required current for the sensors, it is necessary to ensure that all the transistors must operate in the forward active region. While transistor Q_2 always remains in this region, other transistors may not. The reason why transistor Q_2 remains forward active is that its base is connected to its collector, resulting in no voltage differential between these, which means that:

$$V_{EC_{Q2}} = V_{EB(on)_{Q2}} \approx 0.7\ \mathrm{V} \quad \left(> V_{EC(sat)_{Q2}}\right)$$

To make sure that the other transistors remain in the forward active region, the designed circuit offers three degrees of freedom that can be adjusted: v_{ref}, R_{cur} and R_{sen}. By applying the mesh current law to

the first branch, which defines the current value, we can determine the operating conditions for transistor Q_1.

$$\begin{gathered}
-V_{CC} + R_E \cdot i_{sen} + V_{EC_{Q2}} + V_{CE_{Q1}} + v_{ref} = 0 \quad \Leftrightarrow \\
\Leftrightarrow \quad V_{CE_{Q1}} = V_{CC} - R_E \cdot i_{sen} - V_{EC_{Q2}} - v_{ref} \\
\text{where} \quad V_{CE_{Q1}} > V_{CE(sat)_{Q1}} \\
\text{thus} \quad V_{CE(sat)_{Q1}} < V_{CC} - R_E \cdot i_{sen} - V_{EC_{Q2}} - v_{ref} \quad \Leftrightarrow \\
\Leftrightarrow \quad v_{ref} < V_{CC} - R_E \cdot i_{sen} - V_{EC_{Q2}} - V_{CE(sat)_{Q1}} \quad [\mathrm{V}]
\end{gathered} \tag{4.2}$$

Equation 4.2 illustrates the trade-off between v_{ref} and the operation of transistor Q_1 in the circuit. If the reference voltage exceeds the value determined by the mesh analysis equation, the transistor will no longer operate in the forward active region. This, in turn, results in the circuit's inability to generate a current that depends on the values of v_{ref} and R_{cur} as intended. The VCCS circuit relies on Q_1 operating in the forward active region.

Similarly, the same method can be applied to determine the operating conditions for the transistors Q_{2_x} in the circuit. By analyzing the following mesh equations we can ensure that Q_{2_x} operates in the forward active region and mirrors the generated current for the sensor.

$$\begin{gathered}
-V_{CC} + R_{E_x} \cdot i_{sen_x} + V_{EC_{Q2_x}} + R_{sen_x} \cdot i_{sen_x} = 0 \quad \Leftrightarrow \\
\Leftrightarrow \quad V_{EC_{Q2_x}} = V_{CC} - R_{E_x} \cdot i_{sen_x} - R_{sen_x} \cdot i_{sen_x} \\
\text{where} \quad V_{EC_{Q2_x}} > V_{EC(sat)_{Q2_x}} \\
\text{thus} \quad V_{EC(sat)_{Q2_x}} < V_{CC} - R_{E_x} \cdot i_{sen_x} - R_{sen_x} \cdot i_{sen_x} \quad \Leftrightarrow \\
\Leftrightarrow \quad R_{sen_x} < \frac{V_{CC} - R_{E_x} \cdot i_{sen_x} - V_{EC(sat)_{Q2_x}}}{i_{sen_x}}, \; x \in \{A, B, C\} \quad [\Omega]
\end{gathered} \tag{4.3}$$

Equation 4.3 provides a useful guideline for determining the maximum load that the current mirror circuit can support. If the load exceeds this value, the circuit will fail to replicate the required current for the sensors, as the current will not be properly mirrored across the circuit. Therefore, it is important to ensure that the load at the end of the circuit is within the safe operating limits determined by the mesh analysis equation.

It can be observed from Figure 4.4 that this topology can accommodate multiple sensors by adding more current mirror branches. However, only the bias circuit A (shown in Figure 4.2) from each channel can utilize this feature. Although all the bias architecture circuits have the same routing for replication purposes, only the bias circuit A has a physical connection to the sensors from the other circuits B and C, as explained before.

As previously mentioned, MR sensors consist of a nominal resistance and a variable resistance that

changes with the strength of the magnetic field. The MR sensors used in this project were fabricated at INESC-MN, and have varying nomimal resistance values. While the initial batches had a nominal resistance of $500\ \Omega$, recent batches have a nominal resistance of $1\ \mathrm{k}\Omega$ to $1.5\ \mathrm{k}\Omega$. For the sake of simplicity, the following calculations will be performed for a single sensor, and therefore only one output branch will be taken into consideration. Additionally, the emitter resistances for both transistors are set to $150\ \Omega$. The circuit in Figure 4.4 is designed to accommodate different nominal resistance values by adjusting parameters such as v_{ref}, R_{cur}, and R_{sen}. It should be noted that one of the requirements for the architecture is to be able to provide a maximum biasing current of $5\ \mathrm{mA}$ for a sensor with a nominal resistance of $500\ \Omega$. Using Equation 4.2, one can determine the maximum v_{ref}:

$$v_{ref} < 5 - 150 \cdot 5m - 0.7 - 0.4 \quad \Leftrightarrow \quad v_{ref} < 3.15\ \mathrm{V}$$

As the reference voltage is provided by a DAC, its value can be easily adjusted digitally. To ensure that the transistor Q_1 stays in the forward active region, we provide a margin and assume a maximum value of $3\ \mathrm{V}$ for v_{ref}, which should correspond to the maximum biasing current. By solving Equation 4.1 for R_{cur}, we can guarantee that the maximum biasing current is not exceeded.

$$R_{curr} = \frac{3}{5m} = 600\ \Omega$$

As R_{cur} is the sum of a fixed resistance value and a potentiometer that serves the purpose of fine-tuning, the R_3 resistance was set to $470\ \Omega$, and the R_4 potentiometer was adjusted to match the remaining difference of $130\ \Omega$. With this last tweak, the VCCS is now able to provide a $5\ \mathrm{mA}$ current. With this adjustment, the VCCS can provide a $5\ \mathrm{mA}$ current. The final step is to use Equation 4.3 to determine the maximum output load that the current mirror can handle, to ensure that it can mimic the biasing current.

$$R_{sen} < \frac{5 - 150 \cdot 5m - 0.4}{5m} \quad \Leftrightarrow \quad R_{sen} < 770\ \Omega$$

R_{sen} is also the sum of two resistances, the sensor and a potentiometer. To simplify the experiment setup and improve measurement accuracy, the sensor was simulated by setting the potentiometer to $500\ \Omega$ and shorting the sensor terminals. In brief, these were the values obtained:

$$v_{ref} = 3\ \mathrm{V}\,; \quad R_{cur} = 600\ \Omega\,; \quad i_{sen} = 5m\ \mathrm{A}\,; \quad R_{sen} = 500\ \Omega$$

Table 4.1 was obtained by measuring the voltage at terminals of the transistors in the circuit (Q_1, Q_2, Q_{2_A}). These voltage values confirm all the previous calculations to make sure that all the transistors are operating in the forward active region.

The transistor Q_1 needs to have a voltage V_{CE} greater than the $V_{CE(sat)}$ value, which is $0.4\ \mathrm{V}$. In

Table 4.1: Transistors operating conditions.

	Voltage [V]
$V_{CE_{Q_1}}$	0.594
$V_{EC_{Q_2}}$	0.705
$V_{EC_{Q_{2_A}}}$	1.747

transistor Q_2, since its base is connected to its collector, the voltage V_{EC} is equal to the voltage V_{EB}, which is approximately $0.7\ \mathrm{V}$. The transistor Q_{2_A} has a voltage V_{EC} that corresponds to the difference between the emitter voltage $(5-150\cdot 5m)$ and the collector voltage $(500\cdot 5m)$, which is $1.75\ \mathrm{V}$. This value must also be greater than $V_{EC(sat)}$.

To more accurately demonstrate the bias topology behavior, the DAC responsible for generating the reference voltage was programmed, using an Arduino, to produce a ramp signal ranging from $0\ \mathrm{V}$ to $3\ \mathrm{V}$, with increments of $0.2\ \mathrm{V}$. The measured voltages, which are indicated in purple in Figure 4.4, were used to generate the following figure, providing a clear representation of the bias behavior.

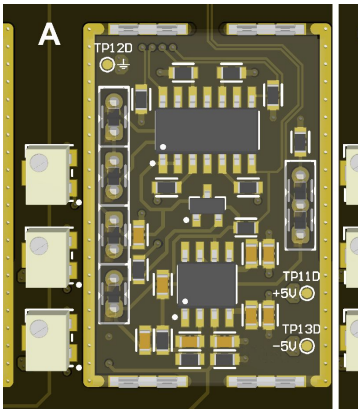


Figure 4.5: 3D view of the bias circuit in the PCB.

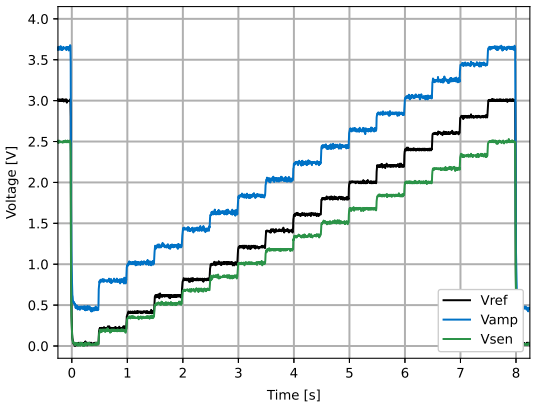


Figure 4.6: Biasing exercise.

Upon analyzing Figure 4.6, it is apparent that the topology is performing as intended since the voltage v_{amp} is consistently $V_{CE_{Q1}}$ higher than v_{ref} (as listed in Table 4.1). Additionally, the relationship between v_{ref} and v_{sen} can be described by Equation 4.4, which utilizes Equation 4.1 for simplification. Therefore, v_{sen} is equal to $5/6$ of v_{ref}.

$$v_{sen} = R_{sen}\cdot i_{sen} \quad \Leftrightarrow \quad v_{sen} = \frac{R_{sen}}{R_{cur}}\cdot v_{ref} \quad [V] \tag{4.4}$$

The PCB layout of this module can be seen in Figure 4.5. This module encompasses two different topologies, which can be controlled using the visible jumpers (headers or $0\ \Omega$ resistors). The module is housed within an Radio-Frequency Interference (RFI) shielding to minimize electromagnetic interference caused by external sources or generated within the system itself while ensuring a compact arrangement.

Topology with Sensor Inside Feedback Loop

The work presented in this thesis offers the opportunity to explore an alternative topology where the sensor is placed inside the feedback loop. This topology is included to demonstrate its potential for attenuating noise from all the sources in the biasing topology, except for the noise introduced by the reference voltage, amplifier, and sensor. However, it is worth mentioning that if the sensors have a high capacitance, there is a possibility of amplifier oscillation in this topology. It is important to clarify that the topology involving the sensor inside the feedback loop, developed by Dr. Tiago Costa [43], is referenced in this work to acknowledge its existence and potential advantages. Nevertheless, it is important to note that this topology is not extensively covered or extensively analyzed in detail within the scope of this master's thesis. The primary focus of this thesis is on the previously explained topology, which has been thoroughly examined and optimized. Further investigation and in-depth exploration of the sensor-inside-feedback-loop topology would require dedicated research and analysis beyond the scope of this study.

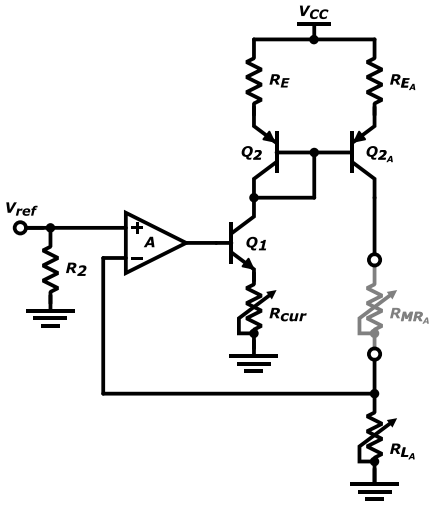


Figure 4.7: Biasing topology where the sensor is inside the feedback loop (for more details refer to Appendix A).

Figure 4.7 depicts the sensor-inside-feedback-loop topology, as introduced by Costa [43]. In this topology, the voltage reference v_{ref} serves as the input to the amplifier, which generates an output voltage to ensure a desired output current, resulting in a voltage across R_L that matches v_{ref}. Additionally, transistor Q_1 and resistor R_{cur} create an auxiliary current path, enabling the amplifier output to be independent of the sensor resistance value, thereby relaxing the output excursion requirements. It was observed in the study that by choosing R_L to be higher than R_{MR}, the noise power generated by the current source is attenuated by a factor of $(R_{MR}/R_L)^2$.

Reference Voltage

To ensure that the biasing circuit performs correctly, it requires a precise and stable reference voltage.

However, using the power supply to generate the reference voltage is often not ideal due to the inherent noise and fluctuations that can arise in the supply voltage. To overcome this issue, a common approach is to use a voltage reference generator paired with a DAC to generate and precisely adjust the reference voltage.

This circuitry to generate a reference voltage is a widely used technique in electronic circuits, particularly in applications where a stable and accurate current source is required, such as in industrial automation, instrumentation, and control systems. By using a DAC, the reference voltage can be adjusted digitally, providing precise control over the output current of the biasing circuit. In the work of Germano *et al.* [27], this technique was implemented to generate a reference voltage in the biochip platform, as discussed in Chapter 2. By utilizing the generator and a DAC, they were able to achieve a stable and accurate current source, even in the presence of environmental factors such as temperature variations and power supply fluctuations. Additionally, this approach provides high flexibility as arbitrary waveforms can be generated by programming the DAC.

The reference voltage schematic used in the AFE interface is depicted in Figure 4.8. While the biasing topology can provide a bias current regardless of the load, variations in the sensor's nominal resistance may occur. However, by using a DAC to individually adjust each current that feeds the sensors, this resistance difference can be overcome without the need for more accurate components such as precise resistors or potentiometers. In addition, calibration can be performed via software, eliminating the need for manual adjustments to the PCB. As a result, the user can simply select the values in the application, making the process more efficient and less prone to errors.

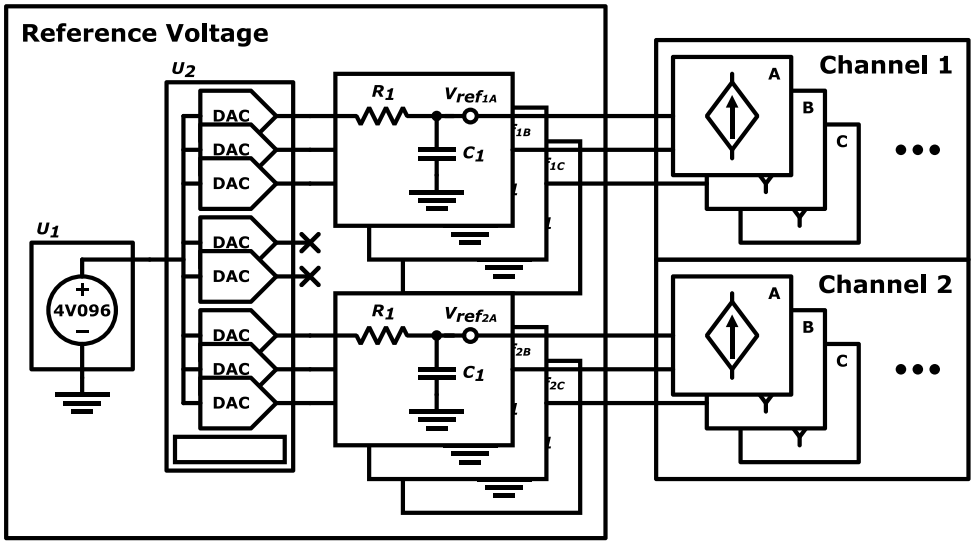


Figure 4.8: Reference voltage schematic (for more details refer to Appendix A).

To accommodate the six different sub-channels on the board, a DAC with a minimum of six channels is required, as shown in Figure 4.2 where there are two main channels each with three sub-channels.

In addition, it is important to use an external input voltage for the DAC, as an ultra-low noise reference voltage is required to minimize the impact of noise on the output signal of the sensors. Figure 4.8 illustrates how this is achieved through the use of U_1 and U_2, where U_1 provides the input voltage to the DAC U_2, which then adjusts each output voltage based on its programming. As for the voltage reference, it must meet two requirements: have low-noise characteristics and provide a voltage higher than $3\ \mathrm{V}$ to enable a $5\ \mathrm{mA}$ biasing current to flow through the sensor when its nominal resistance is $500\ \Omega$, as previously determined. Before each DAC outputs feeds the bias circuit, some additional filtering is performed using a RC filter, acting as a LPF. The RC circuit will smooth the output waveform of the DAC, by filtering out high-frequency noise components and harmonics present in the signal, leaving only the low-frequency signal intact. The cutoff frequency of the RC filter depends on the values of R (resistance) and C (capacitance) used in the circuit – and can be calculated using the following Equation 4.5.

$$f_c = \frac{1}{2\pi RC} \quad [\mathrm{Hz}] \tag{4.5}$$

The selection criteria for the DAC Integrated Circuit (IC) was straightforward. Analog Devices has a product family called *nano*DAC+ that includes several compact package ICs with low-power, rail-to-rail strings of DACs whose outputs have high precision. This family of ICs is great because it gives flexibility in terms of the communication protocol to control the IC. For the schematic shown in Figure 4.8, U_2 belongs to the $\mathrm{AD567xx}$ family, which was the best choice in terms of versatility. Depending on the IC, the communication protocol can be either Serial Peripheral Interface (SPI) or Inter-Integrated Circuit (I2C), the input voltage can be either internal or external, and the resolution can be either 16-bit or 12-bit. For this project, the $\mathrm{AD5676}$ was used because it encompasses SPI, external input voltage, and 16-bit resolution. Furthermore, by selecting a versatile family like the *nano*DAC+, there is no need to limit the pool search according to the communication protocol for future ICs in other circuits.

The reference used in the design is the $\mathrm{ADR444}$, also from Analog Devices, it uses an XFET reference, providing better noise performance than buried Zener references, which was the type used in the previous work (Chapter 2.2). Additionally, the output voltage of $4.096\ \mathrm{V}$, making it ideal to be controlled with a minimum of a 12-bit DAC for achieving a resolution of $1\ \mathrm{mV}$. The RC filter, comprised of R_1 ($100\ \Omega$) and C_1 ($100\ \mu\mathrm{F}$), has a cutoff frequency of approximately $16\ \mathrm{Hz}$, calculated using Equation 4.5. The main purpose of the filter is to provide a clean DC current to the sensors, free from switching noise introduced by the DACs, clock harmonics, and high-frequency noise components. The capacitance value of C_1 is the highest available in a 0603 package, which is $100\ \mu\mathrm{F}$, while the resistance value was chosen based on the settling time of the filter output. A lower cutoff frequency leads to a longer settling time. This circuit has been thoroughly tested, as shown in a previous figure (Figure 4.6).

Even though the reference voltage and the biasing topology were designed to provide a DC current to the sensors, further studies using an AC current can be performed by removing the RC filter. Biasing

in AC is a common practice [6, 28, 32], and allows for the output signal from the sensors to be shifted into a higher frequency where the noise is lower, thus improving the SNR. However, it is important to note that this work focuses on DC biasing.

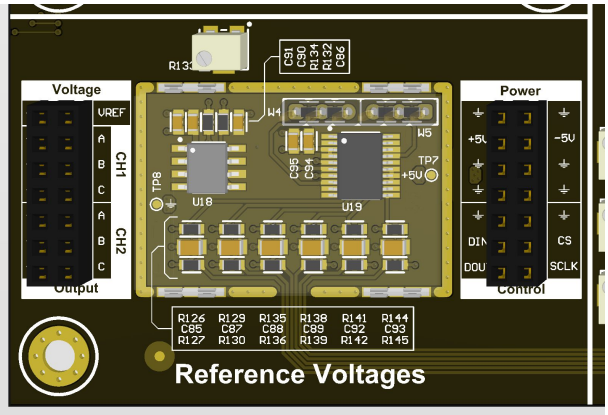


Figure 4.9: 3D view of the reference voltage circuit in the PCB.

Figure 4.9 showcases the reference voltage module integrated into the cytometer platform. This module introduces a new feature, and to ensure adaptability in the event of malfunction, the headers are responsible for providing access to all circuit inputs, outputs, and power supplies. If a failure were to occur, potentially compromising the entire board, a separate small PCB can be affixed to the headers, providing a fixed solution for the problem. This arrangement allows for the isolation and disconnection of the faulty circuit from the rest of the board while utilizing the small PCB. Moreover, the headers also offer control capabilities specific to this circuit.

4.1.2 Amplification Scheme

As explained in Section 3.2, when a magnetic particle passes through a magnetic sensor and is excited by a permanent magnet, the magnetic sensor reacts to the field generated between the magnet and the particle, resulting in the generation of a pulse. The purpose of this application is to measure the number of pulses per sample, which corresponds to the number of analytes present in the sample. The resulting data will be analyzed by a computer and undergo digital processing. In order to convert the sensor signal, we will be using ADCs. It's important to take the quantization resolution into consideration, especially since the sensor response signal typically falls in the hundreds of μV range, which is close to the first decision level of most ADCs. To make sure that we utilize the maximum dynamic range of the ADC and reduce the quantization noise associated with the conversion, we need to amplify the signal.

The amplification scheme used in this work is based on Eng. Ruben Afonso work in Section 2.2, which was developed from Tiago Costa's thesis [19]. In ultra-low noise applications, differential amplifiers are commonly used to increase the SNR ratio and minimize the impact of external interference on

measurement accuracy. These amplifiers work by taking the difference between two input voltages while suppressing any voltage that is common to both inputs. By doing so, they can reduce the impact of common noise between the positive and negative terminals.

The amplification scheme used in this work is illustrated in Figure 4.10, and it employs the $\mathrm{AD8429}$ instrumentation amplifier (U_1) from Analog Devices. This IC is an excellent choice for measuring extremely small signals, thanks to its high-precision architecture. The $\mathrm{AD8429}$ features a high-bandwidth and a high-gain architecture that can be adjusted from $1\ \mathrm{V/V}$ to $10000\ \mathrm{V/V}$. However, it's important to note that the voltage input offset will also be amplified, accordingly to the gain. Therefore, when choosing the gain for the amplifier, a trade-off must be made between the differential amplifier's dynamic response and the voltage input offset.

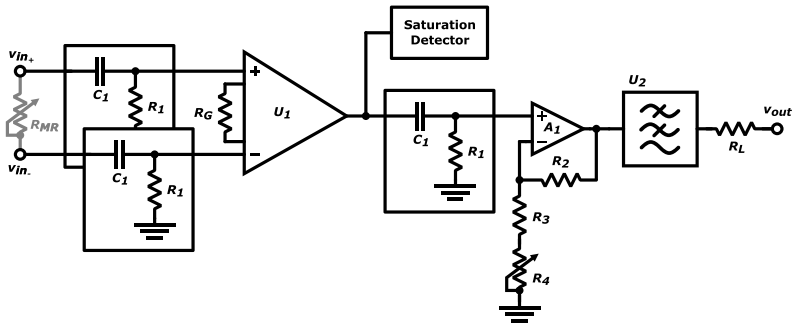


Figure 4.10: Amplification and filtering schematic (for more details refer to Appendix A).

In applications developed at INESC that utilize SV sensors, the required bandwidth is typically low [44, 45]. However, the necessary bandwidth can vary depending on factors such as the size of the particles or the sensor design. To ensure accurate flow rate measurements up to $30\ \mu\mathrm{l/min}$, a bandwidth of at least $100\ \mathrm{kHz}$ is required, according to a recent study by Dr. Diogo Caetano [30]. The signal response frequency is directly proportional to the velocity of the particles flowing through the sensors. To process the signals from the sensors, it is crucial to select an amplifier with a dynamic response that can respond to the signal without causing excessive attenuation. However, increasing the amplifier gain reduces the available bandwidth. This relationship is given by the Gain–Bandwidth Product (GBWP), which represents the maximum gain that can be achieved for a given bandwidth. For the $\mathrm{AD8429}$ instrumentation amplifier, the GBWP is $15\ \mathrm{MHz}$. Therefore, if the gain is set to $1000\ \mathrm{V/V}$, the dynamic response of the amplifier is reduced to $150\ \mathrm{kHz}$. This response is sufficient to provide satisfactory performance when processing the sensors' signals, while still leaving room for any potential flow rate increases. This gain is also sufficient to prevent the signal from undershooting or overshooting when the amplified input noise is added to the sensor's signal. If the amplified noise adds too much voltage to the signal, it may exceed the amplifier rails, leading to the clipping of the output signal. This is undesirable as it can cause distortion of the signal and compromise the accuracy of the measurement.

Even though amplifying the signal by a factor of 1000 is significant, it is not enough to fully utilize the dynamic range of the ADC. As a result, the amplification circuit in Figure 4.10 combines the instrumentation amplifier with a non-inverting amplifier, creating a cascade or multistage amplifier architecture. This extra amplifier helps to improve the overall gain, allowing for better utilization of the ADC dynamic range. It is known that adding an extra amplifier will not significantly impact the overall noise of the system. This is due to the Friss formula, which states that when several devices are cascaded, the total noise figure is given by:

$$F = F_{A_1} + \frac{F_{A_2} - 1}{G_1} + \frac{F_{A_3} - 1}{G_1 G_2} + ... + \frac{F_{A_n} - 1}{G_1 G_2 ... G_{n-1}} \quad \left[\frac{\mathrm{dB}}{\mathrm{Hz}}\right] \tag{4.6}$$

Where F is the noise figure of the n-th stage and G_n is the power gain of the n-th stage. With Equation 4.6, it becomes clear that the F of the initial stage in an amplification chain has the most significant effect on the total noise figure than the following stages. This is because the F of each stage is divided by the gain of all the previous stages. This means that the circuits from the input signal to the first amplification stage play a crucial role in determining the overall noise of the AFE system, and can be considered to be the key circuits for establishing the system SNR.

The gain of the non-inverting amplifier (A_1) is given by Equation 4.7. In this circuit, the resistances R_2, R_3, and R_4 were adjusted so that the gain of the second-stage amplifier is $10\ \mathrm{V/V}$, which gives an overall amplification gain of $10000\ \mathrm{V/V}$. This high gain is necessary to boost the signal from the hundreds of microvolts to the volts range, which is required for proper signal acquisition and processing. As such, R_2 is a $9.1\ \mathrm{k\Omega}$ and the sum of R_3 and R_4 is approximately $1\ \mathrm{k\Omega}$. The adjustable R_4 allows more precision over the gain, which otherwise wasn't possible, using only two resistances.

$$G_{A_2} = 1 + \frac{R_2}{R_3 + R_4} \tag{4.7}$$

The amplification process not only boosts the desired signal but also amplifies any unwanted noise or interference that may be present. Thus, it is essential to remove any unwanted noise from the signal before processing it further. To achieve this, each stage of the multi-stage amplification scheme is equipped with an RC filter, which acts as a HPF. These RC filters are represented inside the squares in Figure 4.10. The signal response from the sensors includes a DC component inherent to the bias, as well as an AC component that carries the magnetic information [30]. To remove the DC component, which is not relevant, and the low-frequency noise generated in the biasing topology, one HPF filter is used at both inputs of the differential amplifier. The RC filter at the output of the differential amplifier, removes the voltage offset and reduces the amplification noise introduced in that stage. The filters used in both amplification stages have an identical cutoff frequency because they use capacitors C_1 and resistors R_1 with the same value. The cutoff frequency is approximately $160\ \mathrm{Hz}$, which is calculated using Equation 4.5, as C_1 is $100\ \mathrm{nF}$ and R_1 is $10\ \mathrm{k\Omega}$.

In Figure 4.10, the final component (U_2) is a 4th-order LPF filter, implemented using the LTC1563-2 IC. The filter has a sharper roll-off, providing improved frequency selectivity and more effectively attenuating frequencies outside the passband. A key advantage of the LTC1563-2 IC is that its cutoff frequency can be easily adjusted using a single resistor value, making it a flexible component that can be tailored to specific needs. It's important to note that the cutoff frequency must be chosen carefully to avoid aliasing. According to the Nyquist theorem, the minimum sampling rate should be at least twice the highest frequency component of the input signal. In this case, the maximum signal frequency is assumed to be $100\ \mathrm{kHz}$, so the minimum sampling rate must be $200\ \mathrm{kSPS}$. Without the filter, the amplification scheme would require an ADC with at least $300\ \mathrm{kSPS}$, since the differential amplifier's band-width is $150\ \mathrm{kHz}$. By setting the U_2 filter's cutoff frequency to approximately $100\ \mathrm{kHz}$, the requirements for choosing the ADC are lower. In summary, this filter serves as an anti-aliasing filter, effectively removing any high-frequency components of the signal that may cause aliasing, while still allowing the system to accurately capture relevant frequency components. The inclusion of the R_L resistor at the end of the filter is vital for the proper operation of the circuit. According to the datasheet, the output of the IC is designed to drive signals around $\pm\ 5\ \mathrm{V}$ when connected to a load greater than $1.2\ \mathrm{k\Omega}$. By adding a resistor with a value of $1.2\ \mathrm{k\Omega}$ as the load, the output signal is ensured to fall within the required range. This load resistor restricts the output current of the filter, allowing it to function within the specified parameters, especially when connected to a low-impedance acquisition device.

To analyze the behavior of the amplification and filtering scheme, the transfer function of the system is plotted in Figure 4.12. The experiment was performed using an Analog Discovery[1] to sweep through frequencies and an attenuator to prevent signal saturation in the first stage of amplification. This experiment was conducted at each step of the amplification chain: instrumental amplifier (1st Stage); non-inverting amplifier (2nd Stage); and output (LPF Filter).

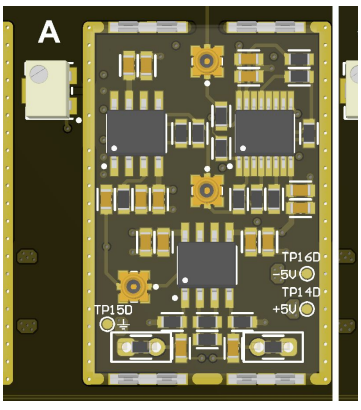


Figure 4.11: 3D view of the amplification scheme circuit in the PCB.

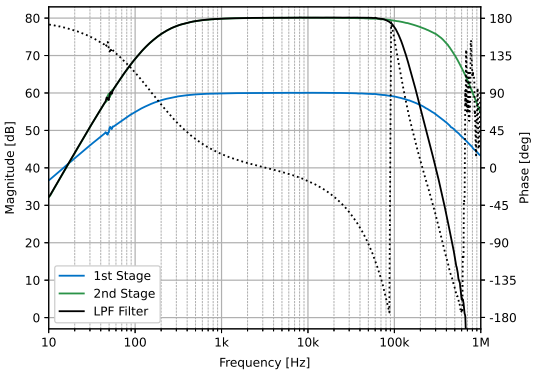


Figure 4.12: Amplification scheme bode diagram.

[1] Analog Discovery 2 system document can be found here.

As mentioned before, Figure 4.12 shows the transfer function of the amplification circuit. The blue trace represents the output of the instrumentation amplifier. It is expected a $20\ \mathrm{dB/dec}$ increase per decade due to the presence of a HPF RC input filter in the instrumentation amplifier. The gain starts to decrease as the frequency approaches $150\ \mathrm{kHz}$, accordingly to the GBWP. The voltage gain in the baseline is also in agreement with the gain defined by R_G, which is $1000\ \mathrm{V/V}$.

$$G_{U_1} = 20 \cdot \log 10\,(1000) = 60\ \mathrm{dB}$$

The green and black traces represent the output of the non-inverting amplifier and the filter output, respectively. With the addition of another filter to the A_1 amplifier input, which is also an HPF RC filter, a $40\ \mathrm{dB/dec}$ decrease is expected. In contrast, the black trace at $100\ \mathrm{kHz}$ shows an $80\ \mathrm{dB/dec}$ decrease compared to the green trace due to the 4$^{\text{th}}$ order LPF filter. The total system gain ($10000\ \mathrm{V/V}$) also matches the gain depicted in Figure 4.12.

$$G_{total} = 20 \cdot \log 10\,(1000 \cdot 10) = 80\ \mathrm{dB}$$

Figure 4.11 depicts the Three-Dimensional (3D) representation of the amplification schematic. This circuit bears resemblance to the one used in the previous version of the cytometer, but with improved debugging capabilities. Notably, each stage of the circuit now features a coaxial switch at its output, enabling the disconnection of the circuit at that specific point. This functionality proves highly valuable for noise measurements and overall circuit debugging purposes. To minimize electromagnetic interference from external sources or within the system, the module is securely enclosed within a shielding specifically designed for RFI.

Saturation Detector

The useful information present in the signal response of the sensors is AC, which is why there are HPF at the input of the differential amplifier to remove any DC components. However, during amplification by the first stage in the signal chain, the inherent noise of the amplification process is added to the signal. Furthermore, due to the very high gain of the differential amplifier, the system is highly sensitive to environmental interference. As a result, the output signal of the first stage can be prone to saturation, when the signal exceeds the output levels that the amplifier can provide. In either case, the amplifier's output becomes a DC signal with a voltage value of either V_{DD} or V_{EE}, depending on the scenario. If a signal becomes saturated and proceeds to the next stage, it will encounter another HPF, which can cause the complete removal of the signal – since saturation removes the AC component, while the filter removes the DC component. This can be misleading to the user, who is not aware of what has occurred and could assume that everything is functioning correctly, even though the signal has been lost. To alert

for this and avoid negative consequences, this will approach the circuit that has been developed to tackle this issue.

Figure 4.13 shows the circuit for the "Saturation Detector" block in Figure 4.10. The circuit can be divided into three segments: Comparator, Delay, and Shift. The previous cytometer interface only had the comparator segment, which was only capable of alerting the user when the differential amplifier was constantly saturating. This was due to the fact that saturation can occur in very short time intervals, making it difficult for the human eye to perceive the Light-Emitting Diode (LED) turning on. To address this issue, the delay segment was developed to keep the LED on for a period of time that is perceivable to the human eye. In addition, the shift block was also created to allow the signal to be used in digital processing.

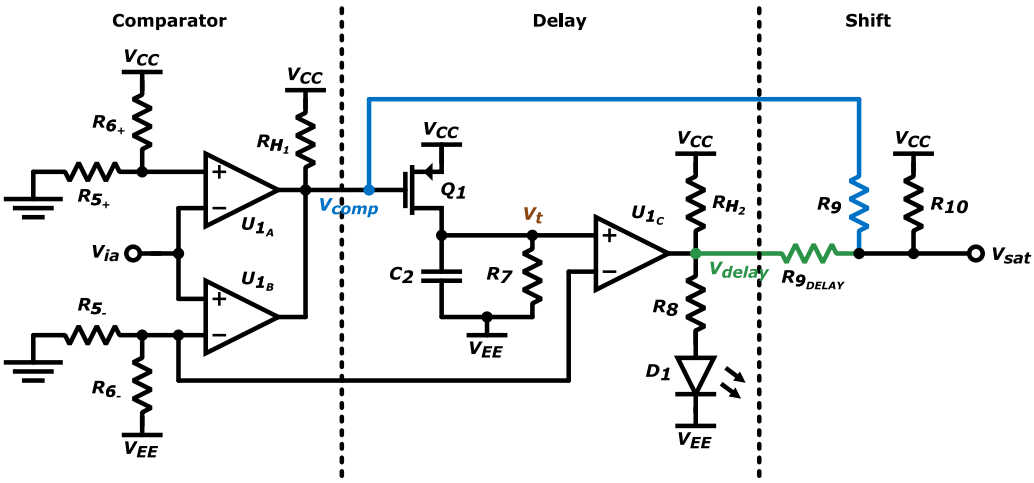


Figure 4.13: Saturation detector circuit (for more details refer to Appendix A).

The saturation block takes the output of the instrumentation amplifier (v_{ia}) as input to identify unreliable signals. One of the comparator terminals is connected to a voltage reference set by the voltage divider R_5 and R_6, and the other is connected to the input voltage being compared v_{ia}. When the input voltage is higher than the reference voltage, the output of the comparator saturates to the negative supply voltage, indicating a low output state. Conversely, when the input voltage is lower than the reference voltage, the output of the comparator saturates to the positive supply voltage, indicating a high output state. There are two comparators, one for each rail of the amplifier. In summary, the behavior of the comparator segment can be defined by Equation 4.8.

$$v_{comp} = \begin{cases} V_{EE} & , v_{ia} > \frac{R_{5_+}}{R_{5_+}+R_{6_+}} \cdot V_{CC} \\ V_{CC} & , \frac{R_{5_-}}{R_{5_-}+R_{6_-}} \cdot V_{EE} < v_{ia} < \frac{R_{5_+}}{R_{5_+}+R_{6_+}} \cdot V_{CC} \\ V_{EE} & , v_{ia} < \frac{R_{5_-}}{R_{5_-}+R_{6_-}} \cdot V_{EE} \end{cases} \quad [\mathrm{V}] \tag{4.8}$$

The main objective of this complementary circuit is to minimize its size while fulfilling its purpose. There-

fore, the choice of the comparator was based on the number of comparators present in the IC. As shown in Figure 4.13, this circuit requires three comparators: two for the comparator segment and one for the delay segment. The $\mathrm{LM2901}$ was selected because it has four comparators and requires the same supply voltage as the other ICs used in this circuit. The $\mathrm{LM2901}$ output consists of an open-collector transistor, which requires a pull-up resistor to drive the output. Thus, a pull-up resistor (R_{H_1}) was placed in the output of U_{1_A} and U_{1_B}. For the reference voltage, R_5 and R_6 resistors were set to $10\ \mathrm{k\Omega}$ and $11\ \mathrm{k\Omega}$, respectively, resulting in a voltage of $\pm 2.38\ \mathrm{V}$ fed into the comparator. The specific voltage polarity depends on the purpose of the comparator. This reference voltage was chosen because the input signal (v_{ia}) is typically in the hundreds of mV range (at that amplification stage), so the reference voltage is significantly different from the signal values, allowing for efficient saturation detection.

In the delay segment, the purpose is to, as the name implies, delay the period where the signal is saturating and provide some visual feedback of the saturation happening to the user, via a LED. This delay feature can be achieved using a capacitor that charges rapidly when the output of the comparators goes low, and slowly discharges when it goes back to the high default state. However, to make this possible, a switch is required that only charges the capacitor when the v_{comp} signal goes to V_{EE}. A P-channel transistor (Q_1) can be used as a switch, with the v_{comp} signal connected to the gate and V_{CC} connected to the source. When $V_{SG} > V_{TH}$, the switch "closes," and the voltage at the source appears on the drain, allowing the capacitor to charge almost instantly, as R_{on} of the transistor is really low. The output of the delay segment comparator is determined by the voltage divider formed by R_{H_2} and R_8, only when the positive input of the comparator (v_t) is greater. This leads to an anode voltage higher than the cathode of D_1, turning the LED on. In contrast, when the negative input is greater, the output is pulled down to V_{EE}, and the LED remains off since no current flows through it. When v_{comp} is no longer in low-state, the switch Q_1 turns off and the capacitor starts discharging through resistor R_7.

$$v_{delay} = \begin{cases} V_{CC} \cdot \frac{R_8}{R_8+R_{H_2}} + V_{EE} \cdot \frac{R_{H_2}}{R_8+R_{H_2}} & , v_{U_{1_C}+} > v_{U_{1_C}-} \\ V_{EE} & , v_{U_{1_C}+} < v_{U_{1_C}-} \end{cases} \quad [\mathrm{V}] \tag{4.9}$$

Equation 4.9 summarizes the output states of U_{1_C}, which were obtained by applying the superposition theorem to the comparator's high-state output voltage and despising the diode resistance. It is noteworthy that when R_8, the resistor that limits the current to D_1, and R_{H_2} have equal resistance values, the high-state output voltage is $0\ \mathrm{V}$. Therefore, v_{delay} is $-5\ \mathrm{V}$ when v_{ia} is not saturated, and $0\ \mathrm{V}$ when it is. The duration for which the LEDs stay on is determined by multiple factors, including the charging time of the capacitor (t_{charge}), the duration of signal saturation (t_{sat}), and the discharge time of the capacitor ($t_{discharge}$). These factors collectively influence the total duration of LED activation, as shown by Equation 4.10.

$$t_{LED_{on}} = t_{charge} + t_{sat} + t_{discharge} \quad [\mathrm{s}] \tag{4.10}$$

The charging time of the capacitor can be considered negligible, as it occurs almost instantaneously, as explained earlier. The duration of signal saturation can vary, but the discharge time of the capacitor remains constant and can be adjusted to achieve a longer duration for the LED to stay on ($t_{LED_{on}}$). By modifying the discharge time, the desired duration of LED activation can be extended. To increase the duration of the LED illumination, the negative reference voltage of the comparator segment is used. This enables U_{1_C} to stay high, for a longer period of the capacitor discharge time and a correspondingly longer on-time for the LED.

$$t_{discharge} = R_7 C_2 \cdot \ln\left(\frac{V_{CC} - V_{EE}}{\frac{R_{5\_}}{R_{5\_}+R_{6\_}} \cdot V_{EE} - V_{EE}}\right) \quad [\mathrm{s}] \tag{4.11}$$

Equation 4.11 provides the time required for the capacitor to discharge based on the values of resistor R_7 and capacitor C_2. This equation was derived by solving the differential equation that describes the voltage across the capacitor as a function of time, and then applying it to the specific voltages in the circuit. By analyzing the equation, one can determine the relationship between the discharge time and the values of R_7 and C_2. Adjusting these component values allows for controlling the duration of LED activation.

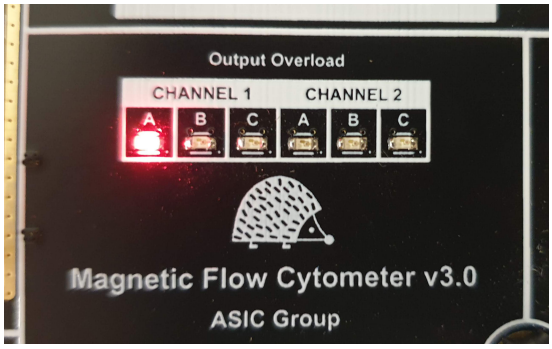


Figure 4.14: Saturation detector LED display with channel 1-A saturating.

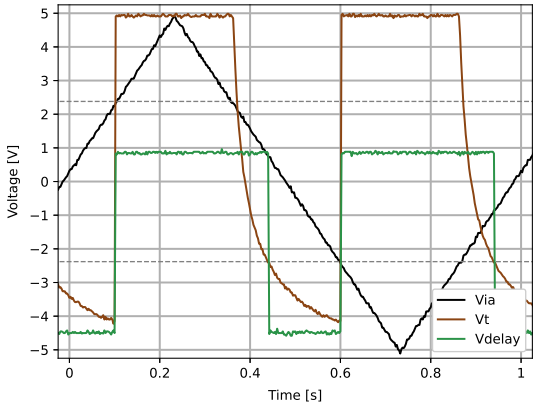


Figure 4.15: Saturation detector functional test.

Figure 4.15 illustrates the functionality of the delay segment designed to increase the duration of the illuminated state of the LED. The trace names and colors correspond to the voltages shown in Figure 4.13. From the graph, it is evident that the signal v_{ia} remains in a saturated state for approximately $0.25\ \mathrm{ms}$ (t_{sat}). The grey dashed lines represent the positive and negative reference voltage levels, which are set at $\pm 2.38\ \mathrm{V}$. When the black trace is above these reference levels, it indicates saturation. The signal v_{delay} extends the high state beyond the saturation period, as explained earlier. This is achieved through the manipulation of the capacitor discharge time, which increases the signal duration by approximately $60\ \mathrm{ms}$, independently of the saturation time. To achieve this, the resistor R_7 was set to $20\ \mathrm{k\Omega}$,

and the capacitor C_2 was chosen to be $10\ \mu\text{F}$, according to Equation 4.11. The graph demonstrates the effectiveness of this segment in prolonging the illuminated state of the LED, displayed in Figure 4.14. Additionally, it is worth noting that the v_{delay} signal does not actually range from $-5\ \text{V}$ to $0\ \text{V}$ as initially expected. This deviation is attributed to the presence of the forward voltage drop (V_{on}) across the diode D_1, which introduces a small offset in the signal.

The last segment of the circuit is the "Shift", which is responsible for changing the range of the signal to make it suitable for digital processing. This is achieved through a voltage divider formed by one of the R_9 resistors and R_{10}. It is important to note that for the v_{sat} signal to operate correctly, only one of the R_9 resistors should be present in the circuit, either R_9 or $R_{9_{delay}}$. If both resistors are used simultaneously, it can lead to erroneous results due to conflicting signals. In order to obtain accurate digital measurements, it is recommended to use the signal originating from v_{comp}, which has not undergone any delay. This signal should be used as the reference for determining when the input signal is saturated. It is worth noting that the delayed signal should only be used for visual feedback purposes and not for digital processing. This is because the delayed signal has undergone a significant delay and does not accurately represent the input signal. The following equation represents the v_{sat} output signal, concerning v_{comp} signal.

$$v_{sat} = v_{comp} \cdot \frac{R_{10}}{R_9 + R_{10}} + V_{CC} \cdot \frac{R_9}{R_9 + R_{10}} \quad [\text{V}] \tag{4.12}$$

Equation 4.12 describes the output voltage, v_{sat}, of the saturation detector circuit in terms of the resistors R_9 and R_{10} and the signal v_{comp}. However, if these two resistors have equal values, v_{sat} can be simplified to either V_{CC} or $0\ \text{V}$, depending on the state of v_{comp}. Specifically, when the circuit's output is low, the differential amplifier is saturating, and v_{sat} is $0\ \text{V}$. Conversely, when v_{sat} is high, the differential amplifier is functioning correctly and there are no errors in the results.

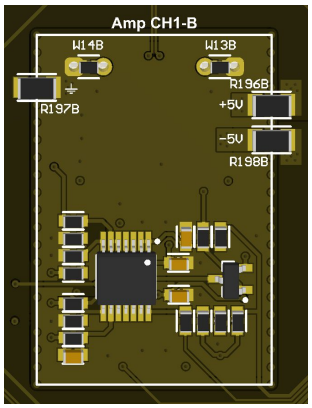


Figure 4.16: 3D view of the saturation detector circuit in the PCB.

Figure 4.16 shows the saturation module integrated into the PCB. This module has been meticulously

designed to maintain a small and compact form factor without compromising the overall functionality of the platform. Its primary function is to identify potential errors within the acquired samples, which couldn't be detected at stages beyond the first amplification stage. Hence, the circuit has been positioned behind the amplification scheme, effectively utilizing space on the bottom layer without compromising the routing on the top layer while serving its intended purpose.

4.2 Sensor Addressing

The chip, housing the highly sensitive MR sensors essential for this application, has been designed and manufactured at INESC-MN. The chip comprises a total of 28 sensors, arranged across 8 microfluidic channels, ensuring optimal coverage. To facilitate seamless integration with different chip batches, the chip is wire-bonded to a PCB developed by Eng. Ruben Afonso. This custom-designed PCB, an integral part of the cytometer platform, plays a crucial role in providing stable electrical connections and mounting support for the chip. A key objective of the sensor addressing module is to simplify the process of acquiring signals from the 28 individual sensors housed within the chip. To achieve this, the module circuit incorporates digitally controlled multiplexers as a gateway between the sensor PCB and the AFE. The sensor addressing module not only optimizes the functionality of the cytometer platform but also offers the flexibility to adapt to various experimental requirements.

In the previous cytometer platform, the sensor selection process involved soldering $0\ \Omega$ resistors to act as switches. This platform has only 2 analog channels, so the resistors on the top layer controlled one channel, while the resistors on the bottom layer controlled the other. Additionally, there were only 7 resistors available on each side of the board, limiting the selection to only one column of the sensor's PCB on each side. As a result, users had to physically orientate the board to access different columns, which posed a constraint. As this application requires multidisciplinary work, the previous method required researchers to have soldering skills and knowledge of interpreting schematics to change the sensor. The reliance on manual soldering and technical understanding added an additional layer of complexity and potential challenges for users operating the cytometer platform. To address these limitations and enhance user convenience, the sensor addressing module has been designed and implemented.

The circuit design for the sensor addressing module is simple and efficient. It utilizes 6 multiplexers, with each multiplexer dedicated to one analog channel on the board. To meet the requirements outlined in the previous chapter, each multiplexer should be capable of switching between at least 3 sensors. Most multiplexer ICs have a number of inputs that are multiple of two. This allows to effectively switch between four sensors using just one IC without increasing the circuit space in the board. Since the amplification is performed differently and the sensors are arranged as a differential pair, the IC must have a minimum of 8 inputs to accommodate the multiplexing of 4 sensors. Regarding internal configuration,

the switches inside the IC can be arranged as a 2x4:1 or an 8:8 structure. In addition to the appropriate configurations, it is crucial to select a multiplexer IC with a low on-resistance for the switches. This ensures that the resistance value of the sensors is minimally impacted by the multiplexer circuitry, thereby maintaining accurate and reliable measurements. Regarding the supply voltage for the IC, it is important to consider the biasing topology and the output characteristics of the sensors. In this case, as the sensor is referenced to the ground, the sensor's output voltage never goes below zero. As a result, the supply voltage for the multiplexer IC can be either single or double.

Table 4.2: Multiplexer ICs for the sensor addressing circuit.

IC	Ron $[\Omega]$	Configuration		Supply $[\mathrm{V}]$		Comm. Protocol		
		4:1	8:8	Single	Double ($\pm$)	I2C	SPI	Bits
ADG1609	4.5	x		3.3 – 16	3.3 – 8			x
MAX4639	3	x		1.8 – 5	2.5			x
ADG739	2.5	x		2.7 – 5.5			x	
ADG71(4/5)	2.5		x	2.7 – 5.5	2.5	x	x	
ADGS1414D	1.5		x	12	5 – 15		x	
MAX14662	0.5		x	1.6 – 5.5	5.5	x	x	x

Table 4.2 presents the various candidate multiplexer ICs considered for integration into the circuit. Upon reviewing the table, the $\mathrm{MAX14662}$ IC emerged as the most suitable choice due to its versatile configuration options and communication protocol compatibility. Furthermore, it exhibited the lowest on-resistance (R_{on}) among the options listed. However, despite its favorable characteristics, the $\mathrm{MAX14662}$ IC presented a drawback in terms of noise introduction. The level of noise generated by this IC was deemed high, rendering it impractical for use in the circuit. The $\mathrm{ADGS1414D}$ also emerged as an interesting choice for integration into the circuit. This IC is particularly appealing due to its design catering to large system channel density. Notably, the $\mathrm{ADGS1414D}$ offers the advantage of route-through pins for digital signals and power supplies. This feature significantly simplifies the routing process, especially when using a 4-layered PCB. Unfortunately, the $\mathrm{ADGS1414D}$ price was found to be extremely high, making it economically unviable for the intended application. Furthermore, it is worth mentioning that two other potential options, the $\mathrm{ADG714}$ and $\mathrm{ADG739}$ multiplexer ICs, were unfortunately out of stock at the time of design. These ICs were considered due to their compatibility with the communication protocol used in the reference voltage circuit. After considering the available options, the final decision was made between $\mathrm{ADG1609}$ and $\mathrm{MAX4639}$. The $\mathrm{ADG1609}$ was ultimately selected due to its greater diversity in terms of supply voltage options. This feature enables further studies and experimentations in the biasing topology, particularly for scenarios that may require a wider supply range.

In order to provide each channel with access to every sensor within the chip, a switch matrix circuit would be required. However, the implementation of such a circuit, with a large number of rows and columns, poses significant challenges in terms of routing in discrete electronics. Additionally, the ap-

proach used in the previous platform, employing $0\ \Omega$ resistors as switches, would not be feasible for the current system, as the number of channels has tripled. Considering these factors, the most suitable solution was to utilize several multiplexer ICs. This allows each analog channel to select between 4 SV sensors.

Table 4.3: Addressable sensors per analog channel.

Channel		MR Sensors			
1	A	1	8	15	22
	B	2	9	16	23
	C	3	10	17	24
2	A	4	11	18	25
	B	5	12	19	26
	C	6	13	20	27

Table 4.3 displays the allocation of sensors for each analog channel within the system. It is evident from the table that out of the total 28 sensors available, only 24 can be utilized. Unfortunately, sensors number 7, 14, 21, and 28 are not accessible through any of the analog channels. This limitation should be acknowledged as a drawback that the chip design team at INESC-MN must take into account when designing future batches of chips.

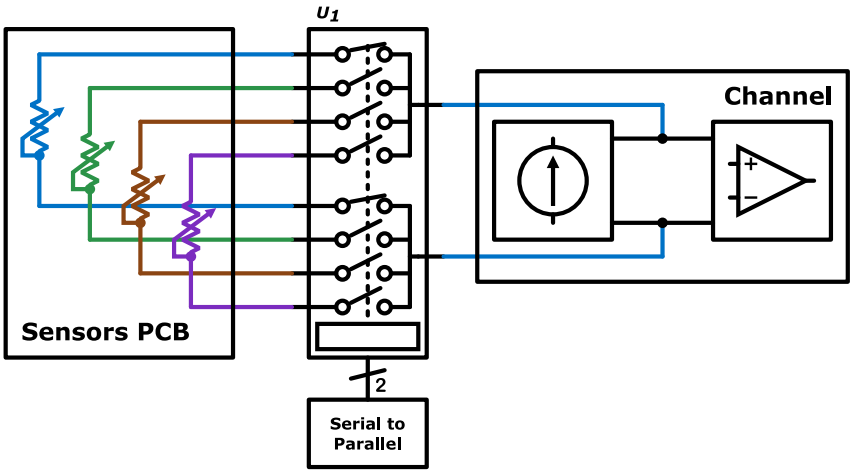


Figure 4.17: Sensor addressing module (for more details refer to Appendix A).

Figure 4.17 provides an illustration of the schematic diagram of the IC used in the module and demonstrates how it integrates into the cytometer system. As depicted, the first inputs of either outputs are selected, indicated by the closed switch. This results in the blue sensor being routed to the output of the multiplexer, which then connects to the output of the biasing topology and the input of the amplification scheme. The previous sections of the document have elaborated on these circuits, which encompass a sub-channel. While the figure only displays four sensors on the sensor PCB for simplicity, it is important to note that the actual PCB houses a total of 28 sensors. Each multiplexer within the

module is responsible for assigning a specific sensor to one of the six sub-channels present in the two main channels. The purpose of the serial to parallel block shown in Figure 4.17 will be further discussed in the document.

Figure 4.19 serves as evidence of the circuit's successful operation. The diagram was generated by utilizing an Arduino to control both the voltage reference and the addressing of the sensor circuits. The objective of this graph is to validate the module's functionality by measuring the voltage drop at the output terminals of the biasing topology, with v_{sen} corresponding to the voltage depicted in Figure 4.4. To accentuate the changes and highlight the circuit's performance, a sensor PCB was employed. However, instead of the chip typically present on the PCB, resistors with values well within the capabilities of the biasing circuit were utilized. This allowed for a clearer demonstration of the desired modifications. For the purpose of this test, the voltage reference was meticulously controlled to provide a fixed reference voltage, thereby ensuring a consistent current flow through the multiplexer terminals. The current was precisely set at $1\ \mathrm{mA}$ by adjusting the value of R_{sen} in the biasing topology. As the sensor load resistor R_L held no relevance for this specific test scenario, it was adjusted to $0\ \Omega$. The resistors used to simulate the sensors in this setup had specific resistance values assigned to them, namely $500\ \Omega$, $1\ \mathrm{k}\Omega$, $1.5\ \mathrm{k}\Omega$, and $2\ \mathrm{k}\Omega$. According to Ohm's law, these resistance values correspond to voltage values of $0.5\ \mathrm{V}$, $1\ \mathrm{V}$, $1.5\ \mathrm{V}$, and $2\ \mathrm{V}$ respectively at the v_{sen} node. This test validates the functionality of the module and demonstrates its effectiveness in controlling sensor addressing.

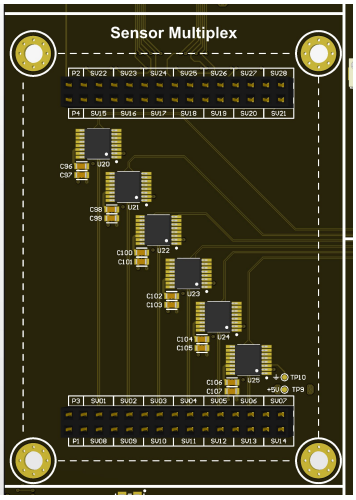


Figure 4.18: 3D view of the sensor addressing circuit in the PCB.

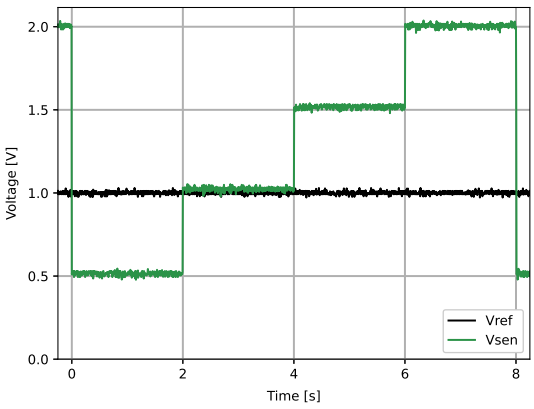


Figure 4.19: Sensor addressing functional test.

The use of multiplexers at the input stage offers opportunities for further exploration, whereby only one amplification scheme is required for multiple sensors. In this scenario, the input signals are multiplexed, reducing the overall size of the PCB as a single amplification circuit suffices. However, incorporating input multiplexing introduces an additional layer of complexity, as the gains, settling times, and

cut-off frequencies need to be adjusted accordingly. The $\mathrm{ADG1609}$ multiplexer used in this project has a settling frequency of $12.5\ \mathrm{MHz}$, enabling the multiplexing of sensors at this frequency. Consequently, the HPF at the inputs of the differential amplifier needs to be removed to accommodate the settling time of the signal. While this feature could have potential advantages in specific applications, it is not practical in the current context due to the influence of nominal resistance mismatch on the DC component of the signal. The removal of the HPF means that the DC component, which is significantly higher than the AC component, is not eliminated. As a result, there is a risk of saturation due to the amplified DC component exceeding the amplifier's capabilities.

Figure 4.18 illustrates the routing of the sensor addressing module. While only the traces on the top layer are visible, it should be noted that this module extensively utilizes all 4 layers for signal routing due to the significant number of different signals involved. The spacing between the headers has been carefully calculated to accommodate the attachment of the PCB with the sensor chip to those headers.

Serial to Parallel Converter

In this work, multiplexers play a crucial role in addressing multiple sensors by enabling the selection of one input from multiple options and routing it to the desired output. However, during the development of this project, the availability of different multiplexing ICs was significantly limited due to a semiconductor shortage. As a result, the project had to utilize the $\mathrm{ADG1609}$ multiplexer IC.

The $\mathrm{ADG1609}$ device employs parallel communication, which means that data is transmitted simultaneously on multiple lines or bits. Consequently, the communication within the addressing module occurs through bits. To access a specific sensor, the multiplexers in the module receive binary signals as selection inputs. These signals determine which sensor is being accessed by setting the appropriate combination of bits.

Parallel communication through bits provides an advantage in terms of speed. However, it also introduces certain considerations regarding the number of inputs required to control each multiplexer. In the case of the chosen multiplexer IC, the $\mathrm{ADG1609}$, it can only choose between 4 inputs. This means that to control each multiplexer, two control bits are needed in addition to the enable bit of the IC. Considering that the addressing module comprises six multiplexers, with one dedicated to each channel, it results in a total of 18 inputs required to address and control all the sensors. This count includes the control bits and the enable bit for each multiplexer. However, it is worth mentioning that the enable bit may not be considered when counting the necessary inputs because the $\mathrm{ADG1609}$ IC does not retain the configuration when enable is off. Thus, in practical terms, the addressing system would require a minimum of 12 inputs (6 multiplexers x 2 control bits), excluding the enable bit, to effectively control the multiplexers and access the desired sensor data.

Considering the specific requirements of your application, where high communication speeds in the selection of sensors are not crucial, it is feasible to optimize the addressing module by reducing the

number of inputs. The reference voltage tuning module communicates using SPI. By integrating the addressing module and the reference voltage tuning module, only one communication protocol needs to be programmed in the system software to control both modules. This simplifies the overall system architecture and eases the control process. The following solution uses shift registers to translate the SPI information into parallel format.

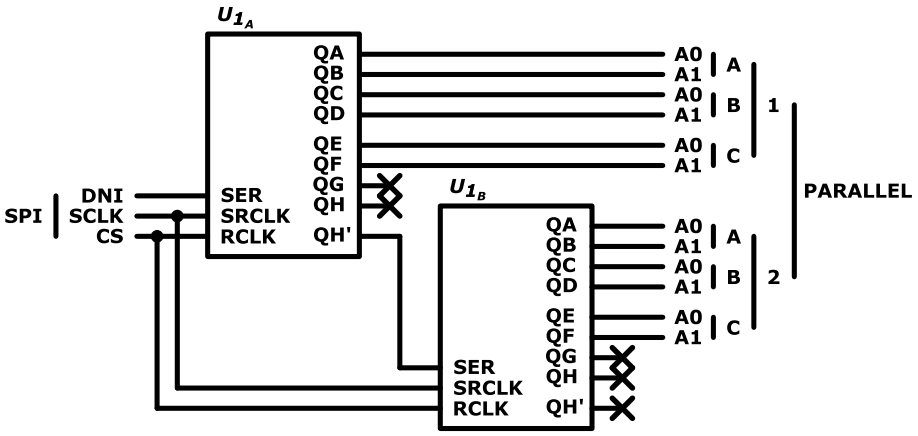


Figure 4.20: Serial to parallel circuit (for more details refer to Appendix A).

The circuit depicted in Figure 4.20 demonstrates the implementation of the serial to parallel module, which serves the purpose of converting the serial communication protocol, specifically SPI, into a parallel format suitable for controlling the multiplexers. One of the advantages of this conversion is that it reduces the number of inputs required to control the multiplexers. In the SPI format, only 3 inputs are needed to control the multiplexers, as these inputs are converted into 12 outputs, meeting the requirements of the 6 multiplexers. To achieve this conversion, the circuit utilizes shift registers. The shift registers effectively store and shift the incoming serial data bits (SER), allowing for the generation of parallel output signals ($Q_{A...H}$) that correspond to the desired sensor selections. The shift register clock ($SRCLK$) and the storage register clock ($RCLK$) are two essential signals in the operation of the circuit. The $SRCLK$ signal is responsible for controlling the shifting of data between the flip-flops within the IC. When the $SRCLK$ signal transitions from one state to another, it triggers the sequential movement of data from one flip-flop to the next, effectively shifting the data along the shift register. On the other hand, the $RCLK$ signal is used to control the storage of the data present in each flip-flop into the output of the IC. When the $RCLK$ signal changes state, it causes the outputs of the flip-flops to be latched into the storage register. The choice of the specific IC used in the circuit design was not critical, and the widely popular $74\mathrm{HC}595$ shift register IC was selected for the task. However, since the $74\mathrm{HC}595$ IC only has 8 output pins available, it was necessary to utilize two of these ICs to meet the requirements of the parallel communication. To address this limitation, the $74\mathrm{HC}595$ IC incorporates a dedicated output pin ($Q_{H'}$) that is directly connected to the last flip-flop output within the shift register chain. This pin allows for

cascading multiple devices together, expanding the available output capacity. In this configuration, the $Q_{H'}$ of the first IC should be connected to the SER pin of the second IC. The previous explanation can be summarized in Figure 4.21, which depicts the block diagram of the level shifters.

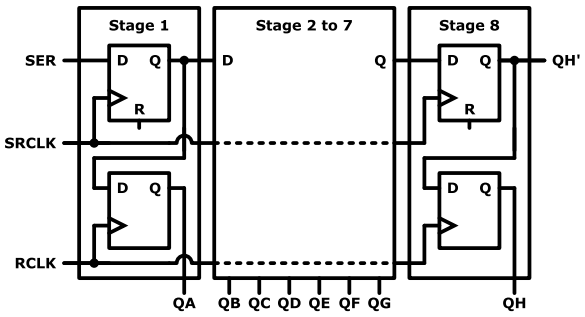


Figure 4.21: Shift register functional block diagram.

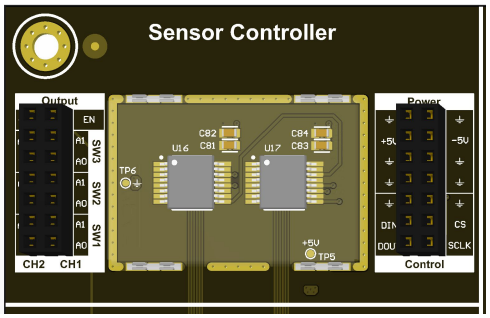


Figure 4.22: 3D view of the serial to parallel circuit in the PCB.

Figure 4.22 presents the 3D representation of the serial to parallel circuit module. This module is positioned near the sensor addressing circuit, as its sole purpose is to convert serial communication into parallel form, enabling the functionality of the sensor multiplexer. In future versions of the cytometer platform, if the semiconductor shortage subsides and a wider range of multiplexer ICs becomes available, it is recommended to use new multiplexers that can be controlled via SPI and meet the specified requirements. In such cases, this module would become obsolete and should be removed to reduce board size. For consistency, this module is also shielded in line with other modules.

4.3 Communication Translator

The board designed in this work has been carefully equipped with multiple inputs and outputs to facilitate the seamless operation of the cytometer platform. Recognizing the importance of compatibility with various controlling or data acquisition systems that may interface with the PCB, a circuit utilizing level shifters has been implemented. This design consideration ensures that the board can be effortlessly integrated into any system that requires control or data exchange. While this project specifically caters to a known system, it is worth noting that the level shifter circuit is not restricted solely to the DE-10 Standard FPGA used as a real-time DSP device. Its versatility allows for easy interfacing with other devices, as demonstrated by numerous tests conducted using an Analog Discovery or an Arduino. Therefore, regardless of the specific system or platform, the level shifter circuit can be readily employed to establish effective communication between components operating at different voltage levels, ensuring smooth and reliable functionality.

Level shifters, also known as voltage level translators, play a crucial role in providing signal separation between the device, specifically the FPGA used in this work (DE-10 Standard), and the cytometer

platform. The FPGA operates at a voltage level of $3.3\ \mathrm{V}$, while the platform requires signals at either $5\ \mathrm{V}$ or $2.5\ \mathrm{V}$. In Figure 4.23, the level shifter circuit is visually depicted as an integral part of the system. The figure provides a comprehensive overview of all the signals involved in transmitting or gathering information from the PCB. Additionally, it illustrates the corresponding General-Purpose Input/Output (GPIO) pins that each signal represents for the DE-10 FPGA. This graphical representation serves as a reference for understanding the signal flow and the role played by the level shifter circuit in maintaining signal integrity and compatibility between the FPGA and the cytometer platform.

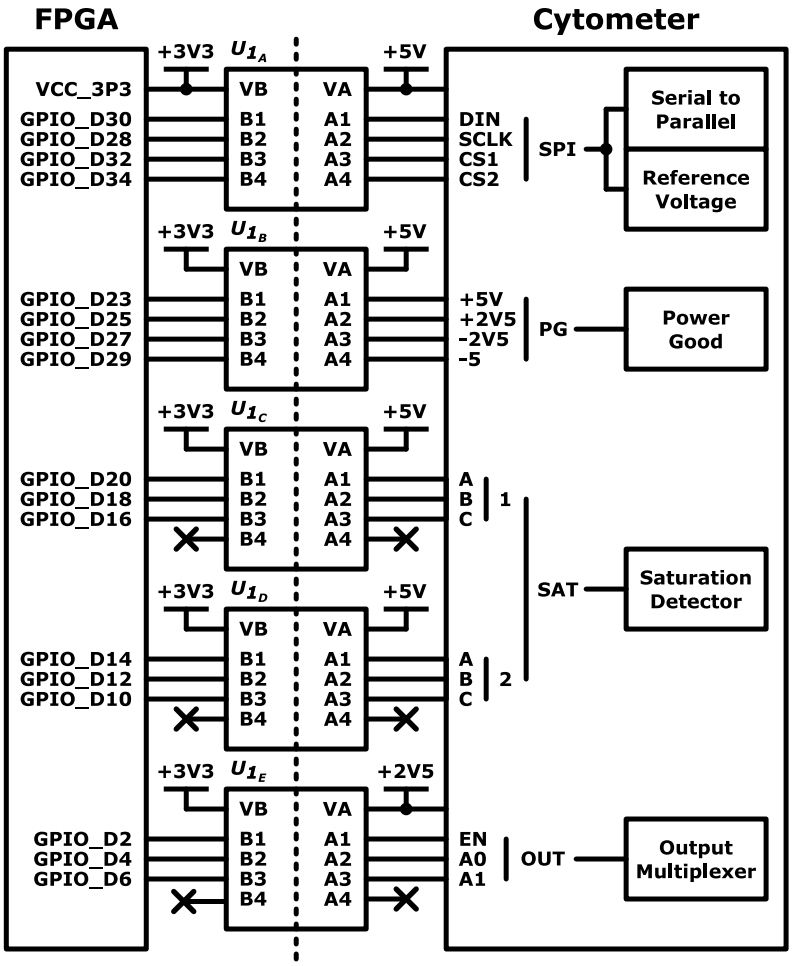


Figure 4.23: Level shifters circuit (for more details refer to Appendix A).

Figure 4.23 illustrates all the signals present on the PCB. It is important to note that the voltage on side B of the level shifters is supplied by the interfaced device. In the depicted case, the $3.3\ \mathrm{V}$ voltage is provided by the FPGA, while the other voltages are supplied by the cytometer. The SPI communication protocol will be utilized by two circuit blocks: the serial-to-parallel block and the reference voltage block. Each block operates with a distinct chip-select signal ($CS1$ and $CS2$). The serial-to-parallel block is responsible for converting the serial protocol into a set of bits that can be understood by the multiplexers

in the sensor addressing circuit. Although the power good block has not been introduced yet, its purpose is to assess whether the supply rails have sufficient voltage to ensure the proper functioning of all the ICs dependent on those rails. The FPGA can utilize this information to verify if the cytometer is ready to receive instructions. The saturation detector block is designed to provide valuable information for the real-time DSP. It allows the identification of a saturated signal during the amplification scheme, ensuring that such samples are not considered in subsequent processing steps. In the upcoming section, the output multiplexer module, which requires parallel communication to alternate between the channels' outputs, will be explained in detail.

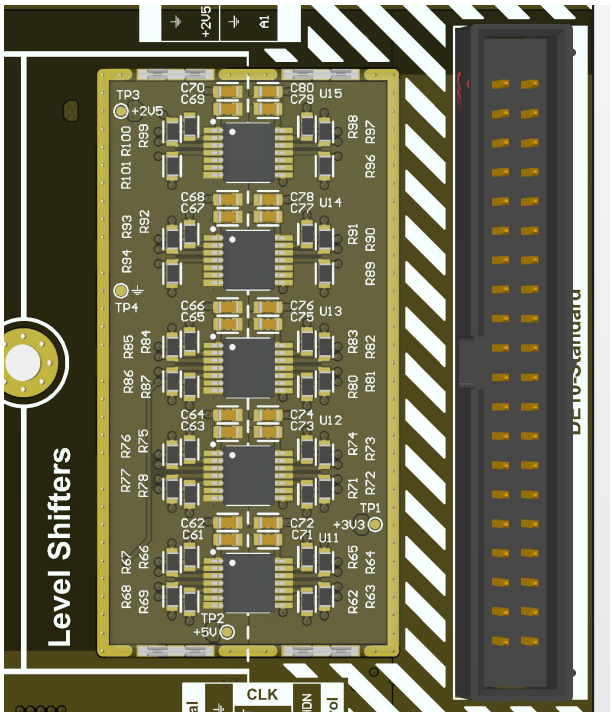


Figure 4.24: 3D view of the level shifter circuit in the PCB.

Figure 4.24 showcases the level shifter circuit integrated into the platform. This circuit comprises 5 level shifts housed within a larger RFI shield, ensuring effective isolation from other modules. Although the PCB does have a specific signal for all the 40 pins in the header, it is designed to be compatible with the DE-10 Standard GPIO header. This compatibility simplifies the process of connecting the cytometer platform to the digital interface, eliminating the need for individual signal wiring.

4.4 Output Multiplexing

As mentioned earlier, the cytometer platform system was designed to ensure compatibility with a specific FPGA, the DE-10 Standard FPGA. However, the FPGA itself lacks ADCs necessary for signal acquisi-

tion. To address this limitation, a dedicated daughter board called the THDB-ADA was bought to provide a DSP solution for the DE-series FPGAs. This external module is also referred to as the ”A/D and D/A Development Kit”. The THDB-ADA card comes in two versions: one utilizing High-Speed Mezzanine Connector (HSMC), and the other utilizing GPIO. Since the GPIO header is already in use for information exchange between the platform and the FPGA, the THDB-ADA card with the HSMC connection was chosen. It's worth noting that both versions of the card are similar in functionality; their main difference lies in the type of connection header used. Although the kit includes both ADCs and DACs, only the ADCs are relevant for the specific application at hand. The purpose of the ADCs is to capture the output signal generated by the analog channels, which will then undergo real-time DSP. However, it should be noted that the card has a significant limitation in terms of the number of available ADCs. While there are 6 different analog channels, the THDB-ADA itself only features 2 ADCs. To address this challenge, a dedicated circuit was developed to multiplex the 6 channels into 2 outputs, effectively mitigating the issue.

Since the THDB-ADA card is equipped with 2 ADCs and there are 2 primary channels, the most straightforward approach is to employ 1 multiplexer for each channel. These multiplexers will alternate between the outputs of 3 sub-channels that collectively encompass the main channel. The kit utilizes the $\mathrm{AD9248}$ ADCs, known for their sampling rate of $65\ \mathrm{MSPS}$ and a $2\ \mathrm{V}$ peak-to-peak range. To ensure that the sampling rate limitation is imposed by the FPGA and not the cytometer platform, it is necessary to employ multiplexers with a switching time faster than the sampling period of the ADCs. Considering that these ADCs will be shared among three sub-channels, the maximum achievable sampling rate per channel in this configuration is $(^{65}/_{3}) \approx 21\ \mathrm{MSPS}$. However, it's important to note that there may also be scenarios where only one sub-channel is being acquired. In such cases, the sampling period is as low as $15\ \mathrm{ns}$. When selecting the IC, it is crucial to prioritize the scenario where only one sub-channel is being acquired to fully leverage the capabilities and benefits offered by the ADC.

Table 4.4: Multiplexer ICs for the output multiplexing circuit.

	Switching Time t_{on} [ns]	On Resistance R_{on} [Ω]	Dual Supply [V]
ADG409	85	40	± 15
MC74HC4052A	59	100	± 6
ADG709	14	3	± 2.5
ADG759	14	3	± 2.5

Table 4.4 illustrates the available multiplexers at the time of selection, taking into account the semiconductor shortage previously mentioned in the sensor addressing module. The presented multiplexers in the table are chosen for their minimal switching time. Since speed is a critical factor for this circuit, the communication protocol used to control the multiplexers is not relevant. Therefore, all of the multiplexers are controlled using parallel communication. Additionally, the supply voltage needs to be considered

since the signal is no longer referenced to the ground due to the removal of the DC component in the sensor response signal. Among the options, the $\mathrm{ADG409}$ and $\mathrm{MC74HC4052A}$ appeared promising as their supply voltage matched the power lines required for each IC on the board. However, their switching times were not fast enough, and not even the scenario where all 3 sub-channels are acquired simultaneously, sampling period of $46\ \mathrm{ns}$, would fully benefit from the ADCs' potential. As a result, the choice was narrowed down to the $\mathrm{ADG709}$ and $\mathrm{ADC759}$, both offering identical performance. The selection was primarily based on the footprint, and the $\mathrm{ADG709}$ had the most commonly used footprint, making it easier to replace with another IC if needed. One drawback of using this multiplexer is that the power circuit needs to be designed to accommodate additional supply rails to power this IC. The output multiplexing circuit, employing these multiplexers, is depicted as follows:

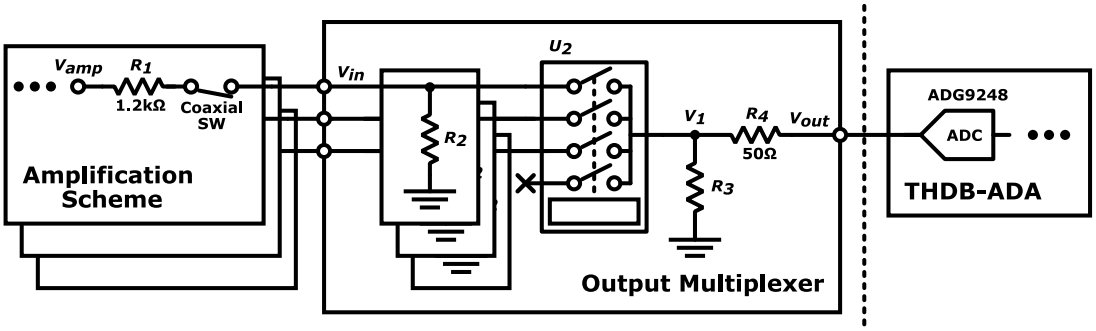


Figure 4.25: Output multiplexer circuit (for more details refer to Appendix A).

The circuit depicted in Figure 4.25 showcases the implementation of output multiplexing in the developed cytometer platform. It is worth noting that the picture only represents a single channel, but it should be understood that this circuit is replicated twice to cater to the presence of two channels in total. Moreover, the $\mathrm{ADG709}$ features an input voltage protection mechanism. If any of the inputs surpasses the maximum or minimum supply voltage, the IC will activate clamping, effectively shutting down. In such a scenario, crosstalk may occur between the selected channel and the input signal that exceeded the supply voltage due to clamping. Hence, it is essential for the circuit to ensure that the input signals do not exceed the range of $\pm\ 2.5\ \mathrm{V}$, and the output should not exceed $\pm\ 1\ \mathrm{V}$ range. This output limitation is necessary because the FPGA ADC is not capable of handling higher voltages, as specified before. The voltage reduction is achieved within this module, and not considered in the amplification scheme gain. This design approach allows for compatibility with the previous version of the cytometer, utilizing the same ADC and ensuring broader compatibility beyond just FPGA usage. The voltage reduction is achieved through a two-step process using voltage dividers. Equations 4.13 and 4.14 represent the specific calculations for this reduction.

$$v_{in} = \frac{R_2}{R_1 + R_2} \cdot v_{amp}\ (< \pm\ 2.5\ \mathrm{V}) \quad [\mathrm{V}] \tag{4.13}$$

$$v_{out} = \frac{R_2//R_3}{R_1 + R_2//R_3} \cdot v_{amp} \ (< \pm 1 \text{ V}) \quad [\text{V}] \tag{4.14}$$

Both Equations 4.13 and 4.14 are referenced to v_{amp}, which represents the signal obtained from the amplification scheme immediately after the filter stage. As previously mentioned, the filter can't drive a signal higher than ± 4.5 V. The voltage divider takes into account the minimum load resistance (R_1) required by the LPF. In Equation 4.14, the calculation despises the impact of the R_{on} of the multiplexer and the impedance matching resistor (R_4). These resistances are relatively low, and their effect on the result is negligible. The voltage divider to address the specified limitations, employees resistors R_2 and R_3, both with a value of $680\ \Omega$. The functionality of these resistors and the role of the multiplexing circuit can be illustrated in Figure 4.27.

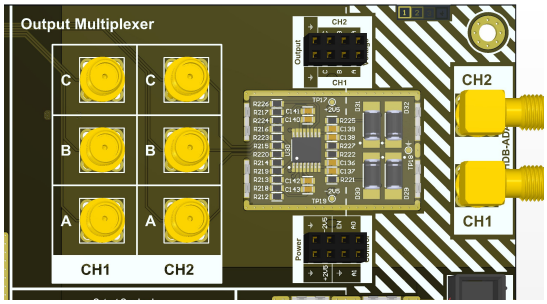


Figure 4.26: 3D view of the output multiplexer circuit in the PCB.

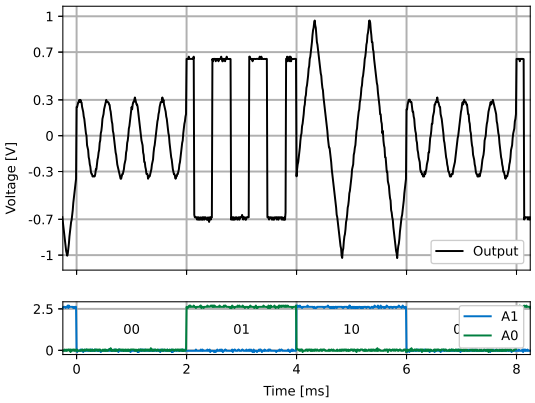


Figure 4.27: Output multiplexer functional test.

Figure 4.27 illustrates a test conducted to evaluate the performance of the circuit in multiplexing three known signals, simulating the behavior of the sensors. This test was performed using an Analog Discovery device and an oscilloscope. During the test, a sine wave with a frequency of $2\ \text{kHz}$ and amplitude of ± 1.5 V was generated by the oscilloscope and connected to the first input of the circuit, represented by the word "00". Additionally, a square signal with a frequency of $1.5\ \text{kHz}$ and amplitude of ± 3 V, was applied to the second input, represented by the word "01". Furthermore, a triangular signal with a frequency of $1\ \text{kHz}$ and amplitude of ± 4.5 V was fed into the third input, represented by the word "10". A resistor with $1.2\ \text{k}\Omega$ value, was also added in series to the input signals to mimic (R_1). The control sequence was generated using Analog Discovery. The circuit is confirmed to be functional as the signals applied at the input are observed at the output, with the expected reduction in amplitude. The amplitude reduction can be calculated using Equation 4.14.

$$v_{out1_{max}} = \frac{680//680}{1.2k + 680//680} \cdot 1.5 \approx 0.33 \text{ V} \ ; \quad v_{out2_{max}} \approx 0.66 \text{ V} \ ; \quad v_{out3_{max}} \approx 0.99 \text{ V}$$

Figure 4.26 showcases the output multiplexer circuit as a module that has been integrated into the

cytometer PCB. This module is designed to function independently, with inputs being connected through SMA connectors. The amplification scheme can be detached from this circuit using the coaxial switches mentioned in the relevant section. This unique feature allows this module to be utilized as a mini-board for other applications or even with the previous cytometer platform, which can be cascaded for redundant measurements. In such a scenario, the FPGA or other DSP interfaces can be employed for data processing.

4.5 Power Supply

In the realm of electronic circuits, all the circuitry explained in this chapter relies on a reliable and adequate power supply to ensure proper functioning. Power is of utmost importance in electronic circuits as it provides the necessary energy for the correct operation of circuit components, enabling the generation and propagation of desired electrical signals and functionalities. This section focuses on the critical aspect of power in electronic circuits. In the upcoming sections, a detailed exploration of power circuits will be undertaken. A comprehensive understanding of power circuits is vital for achieving optimal performance, reliability, and longevity of the electronic system.

To ensure the proper functioning of the cytometer platform, four supply rails are required. The board must be capable of providing the following voltages: $+5\,\mathrm{V}$, $+2.5\,\mathrm{V}$, $-2.5\,\mathrm{V}$, and $-5\,\mathrm{V}$. In order to enhance flexibility, the circuit was designed to accommodate multiple power sources. The first power source utilized is batteries, which were also employed in the previous platform. Battery power offers reliability, minimal noise introduction, and portability, making it an ideal choice for experiments and field use. This enables the system to be self-contained and independent of external power sources. As an alternative to batteries, a laboratory DC power supply can be used. However, it is important to note that this power supply may introduce higher levels of noise compared to batteries. Additionally, the portable aspect is compromised, as the system becomes reliant on a stationary power source. The third power source is the FPGA itself. The cytometer platform is designed to be compatible with the DE-10 Standard FPGA, simplifying the setup process and the required equipment. By utilizing the power supply provided by the FPGA, the system benefits from a streamlined configuration and reduced complexity. Lastly, USB power can also serve as a power source for the cytometer platform. This allows for the use of power banks or even direct connections to a computer running the cytometer software. USB power is convenient as a computer is required to configure and control all necessary parameters prior to usage. By accommodating these three power sources, the cytometer platform offers flexibility and adaptability to different operating scenarios. Users can choose the most suitable power source based on their specific needs.

Figure 4.28 illustrates the block diagram showcasing the transformation of power sources into the

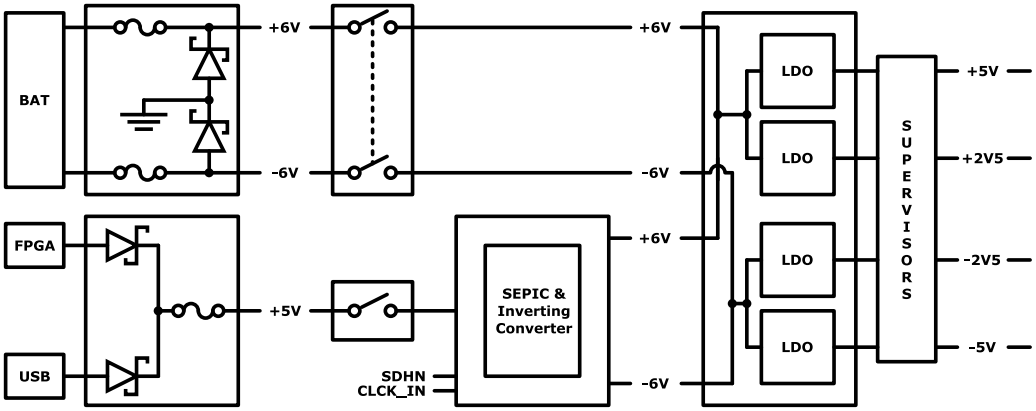


Figure 4.28: Power circuit diagram (for more details refer to Appendix A).

necessary power rails for the PCB. Several measures are implemented to ensure the safe and efficient utilization of these power sources. To protect against mistakes when connecting the battery, a power protection circuit is employed. This circuit safeguards the subsequent ICs by preventing damage, and in case of any fault, only a fuse needs to be replaced. To prevent current flow between the FPGA and USB power supplies when both are connected, a Schottky diode is utilized. This diode ensures the isolation of the power sources, avoiding potential issues that may arise from simultaneous connection. Since the FPGA and USB power sources provide a fixed DC voltage, a DC/DC is necessary. In this application, a Single-Ended Primary-Inductor Converter (SEPIC) and inverting circuit is used to boost the signal to ensure proper functionality of the following circuitry. Additionally, its inverting feature generates an inverted voltage, resulting in two power rails. The outputs of the SEPIC and inverting converter circuit mimic the battery power supply, providing $\pm 6\ \mathrm{V}$ rails. Lastly, an Low-DropOut (LDO) regulator circuit is employed to adjust the input voltage to meet the specific requirements of the PCB. This ensures a stable and reliable power supply for the circuit components. By implementing these power conversion and protection mechanisms, the PCB can efficiently utilize the available power sources and provide the necessarily regulated voltages for the proper functioning of the circuitry.

Table 4.5 provides a rough overview of the power consumption for each individual IC within the various modules of the platform. Upon observation, it can be noted that the new features have a relatively low impact on the supply current. However, the most significant factor contributing to the increased current demand is the expanded number of analog channels, which is three times greater than that of the previous platform. These values were obtained from the respective datasheets of each component. To ensure the proper functioning of the system, it is important to consider the worst-case scenario where all components are operating at their maximum power consumption. In order to meet the power demands of the system, the LDO regulator circuit must be designed to provide the required supply current, in that scenario.

Table 4.5: Supply current requirements of the components in the cytometer platform.

Module	Component	Quantity	Supply Current [mA]	
			Typical	Maximum
Bias Topology	LT1677	6	2.6	3.4
	Mirror Branch	12	1	5
Reference Voltage	ADR444	1	3	3.75
	AD5676	1	1.1	1.26
	AD8429	6	6.7	7
Amplification Scheme	LT1677	6	2.6	3.4
	LTC1563-2	6	15	23
Saturation Detector	LM2901	6	2.5×10^{-2}	2.5×10^{-1}
Sensor Addressing	ADG1609	6	1×10^{-6}	1×10^{-3}
Serial to Parallel	74HC595	2	1×10^{-7}	1×10^{-4}
Communication	LSF0204-Q1	5	2.5×10^{-3}	5×10^{-3}
Power Supervisors	TLV809	4	1.6×10^{-2}	1.7×10^{-2}
		Total:	178	288

Low-Dropout Regulators

The LDO regulators circuit was designed to ensure the stability of power rails throughout the platform's electronic circuits. The inclusion of LDO regulators is essential for maintaining a consistent and precise output voltage, regardless of variations in the input voltage or changes in the load. Additionally, LDO regulators, as the name implies, have a low dropout voltage. This characteristic denotes the minimum voltage difference between the input and output voltages at which the regulator can maintain proper regulation. The low dropout voltage enables LDO regulators to operate efficiently even when the input voltage is close to the desired output voltage. As a result, power utilization is maximized, and the circuits can perform optimally. One of the key advantages of LDO regulators is the built-in filtering and noise reduction mechanisms. These features effectively suppress high-frequency noise and ripple present in the input power source, ensuring a cleaner and more reliable output voltage for sensitive components. By mitigating noise interference, LDO regulators contribute to improved performance and enhanced reliability of the circuits. Their design and integration into the circuitry are relatively simple, making them a practical choice for power rail stabilization.

Due to the limited availability of LDO regulator ICs, the selection process for the appropriate IC was primarily based on the required supply current, which needed to exceed $288\ \mathrm{mA}$ as indicated in Table 4.5. Additionally, the chosen IC had to be capable of providing the necessary voltages of $+5\ \mathrm{V}$, $+2.5\ \mathrm{V}$, $-2.5\ \mathrm{V}$, and $-5\ \mathrm{V}$. To streamline the design and enhance simplicity, an IC with adjustable output voltage was preferred, allowing for the possibility of using the same IC and circuit configuration to fulfill all the required voltage specifications. The LDO regulators from Analog Devices, specifically the $\mathrm{LT3045\text{-}1}$ IC for $+5\ \mathrm{V}$ and $+2.5\ \mathrm{V}$ and the $\mathrm{LT3094}$ IC for $-5\ \mathrm{V}$ and $-2.5\ \mathrm{V}$, were chosen for this purpose. These regulators not only fulfilled the voltage requirements but also featured ultra-low noise, a $500\ \mathrm{mA}$ output

current that could be limited, adjustable output voltages, and programmable power good functionality. Since the selected LDO regulators provided significantly more current than required, the $5\ \mathrm{V}$ rails were limited to $350\ \mathrm{mA}$ and the $2.5\ \mathrm{V}$ rails to $50\ \mathrm{mA}$ to ensure efficient operation within the desired limits.

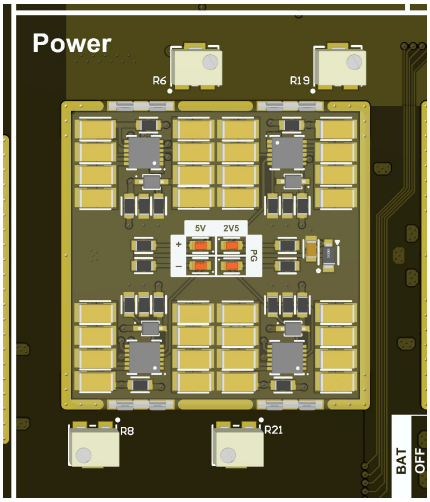


Figure 4.29: 3D view of the LDO regulators circuit in the PCB.

Figure 4.29 depicts the routing of the LDO regulators circuit, showcasing the separation of each power rail. The implementation of the power good feature can be observed, denoted by the centrally positioned LEDs. These LEDs serve to indicate when the voltage drops below predefined thresholds, such as $1.55\ \mathrm{V}$ for the $2.5\ \mathrm{V}$ rails and $4.05\ \mathrm{V}$ for the $5\ \mathrm{V}$ rail. Although this feature is redundant given the presence of a supervisor circuit, which will be discussed later in the document, it was incorporated within the design to utilize the available space within the RFI shield. Furthermore, the circuit features potentiometers located on the sides, enabling precise adjustment of the output voltage.

SEPIC and Inverting Converter

The LDOs are commonly used in situations where the voltage difference between the input and output is small. In these cases, the input voltage must be higher than the output voltage to ensure proper regulation. However, this requirement becomes a limitation when the power supplies are derived from the FPGA or the USB, which provide a fixed $+5\ \mathrm{V}$ voltage. To overcome this limitation, a SEPIC converter circuit is implemented. This particular type of DC/DC converter enables stepping up the input voltage obtained from these sources, addressing the issue effectively. In addition to the required voltage boost, the LDOs circuit also relies on a negative voltage. Thus, besides the SEPIC circuit, an inverting circuit is also required. These types of circuits, as the name implies, are able to generate a negative voltage from a positive input voltage. The purpose of this module is to combine both these DC/DC converters to mimic the batteries' power supply.

To simplify the circuitry in this module, the $\mathrm{LT8582}$ DC/DC converter was chosen. This converter

offers the desired functionalities, serving as a SEPIC by generating an output voltage higher than the input while also providing the capability to invert the polarity of the input. As a result, it facilitates the provision of two boosted power rails with inverted polarity, thereby meeting the requirements of the system. The integration of this IC significantly streamlined the overall design process. The output voltage of the LT8582 converter is adjustable, relying on the nominal values of the components used. The equations necessary to achieve the desired output voltage can be found in the datasheet of the IC, providing flexibility in configuring the output to meet specific requirements. In order for the LT8582 to generate the desired output voltages, it requires a clock signal. The IC offers the option to either generate an internal clock or utilize an external clock source. However, it's worth noting that using the internal clock may introduce additional noise to the output voltage. To mitigate this noise and ensure a cleaner power supply, it is recommended to utilize an external clock signal that should be synchronous or even shared with the ADCs acquisition clock. This synchronization helps to minimize the impact of ripple noise on the system, leading to improved overall performance.

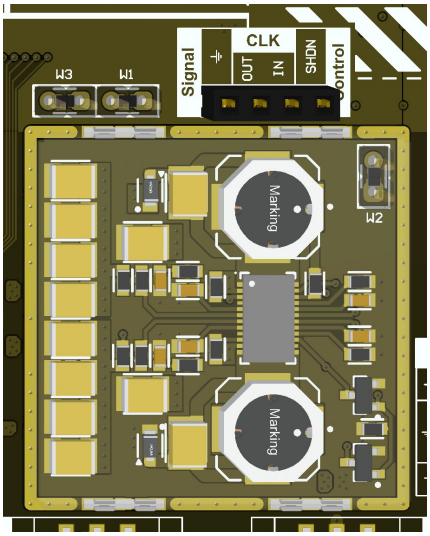


Figure 4.30: 3D view of the SEPIC and inverting converter circuit in the PCB.

Figure 4.30 illustrates the 3D model of the implemented SEPIC and inverting converter circuit. The routing of this module was executed with simplicity, following the guidelines provided in the IC datasheet. The clear documentation and recommendations in the datasheet greatly facilitated the routing process, ensuring an efficient, reliable and compact layout inside the RFI shield. In addition to the primary functionalities, the LT8582 converter incorporates a shutdown pin. This pin offers the convenience of controlling the cytometer platform through software, eliminating the need for manual switch operation. By utilizing the shutdown pin, the system can be easily powered on or off as required, providing enhanced user control.

Power Supervisors

Given the vital role of power in any hardware equipment, it is essential to incorporate a circuit that constantly monitors the voltage levels of power supplies. This circuit serves to detect under-voltage and over-voltage conditions, enabling the user to ensure that the voltage remains within the specified range. Maintaining the voltage within the proper range is critical for the reliable operation of sensitive electronic components, preventing malfunctions or damage caused by insufficient or excessive voltage. To address this requirement, a power supervisor circuit was implemented in the cytometer platform PCB. This circuit offers valuable features such as fault detection for over-current, short circuits, and thermal issues. By promptly identifying and addressing faults, the power supervisor circuit enhances the safety and integrity of the system. Additionally, it provides important feedback to users or system controllers, relaying vital information about power supply status and diagnostics. The power supervisor circuit in the cytometer platform PCB adds an extra layer of protection and user awareness, ensuring that power supply conditions are monitored and potential issues are detected in a timely manner.

The circuit implemented in this work shares similarities with the previous design, as it utilizes the same family of supervisor ICs for monitoring the power rails. However, there are notable differences in this iteration. Instead of using a supervisor IC with an open-drain output, a push-pull output version is employed, eliminating the need for an additional pull-up resistor. Moreover, due to the increased number of power rails in the system, a greater quantity of supervisor ICs is now required. The chosen supervisor IC, the $\mathrm{TLV809}$, offers a wide range of threshold voltage options. However, it is important to note that the threshold voltage cannot be adjusted. Therefore, careful consideration is necessary to choose the appropriate IC with the desired threshold voltage that aligns with the system requirements.

Although not deemed mandatory for the overall functionality of the cytometer, the power supervisor module still holds significance. While not extensively studied, the same ICs were utilized in this module, as they effectively detect under-voltage conditions. In this particular case, threshold voltages of $4.55\ \mathrm{V}$ and $2.25\ \mathrm{V}$ were employed. However, for future iterations of the board, the circuitry in this module could be further improved to encompass the detection of both under-voltage and over-voltage scenarios. Nonetheless, given the multitude of new features implemented in this work's board, this particular feature was considered non-critical at this stage.

Figure 4.32 showcases the functionality of the supervisor circuit by providing valuable feedback to users through the LEDs indicators. It is worth highlighting that the signals indicating which LED (green or red) is illuminated are also accessible to the system operating the cytometer platform (e.g., FPGA). This feature allows the cytometer software to wait for the ICs to receive sufficient supply voltage before sending instructions, ensuring optimal performance. A notable observation from the figure is that the $-2.5\ \mathrm{V}$ power rail is experiencing an issue. By deliberately adjusting the output voltage of this LDO rail to a value above $-2.25\ \mathrm{V}$, the supervisor IC is triggered. This configuration demonstrates the circuit's functionality in detecting and indicating deviations from the desired voltage range.

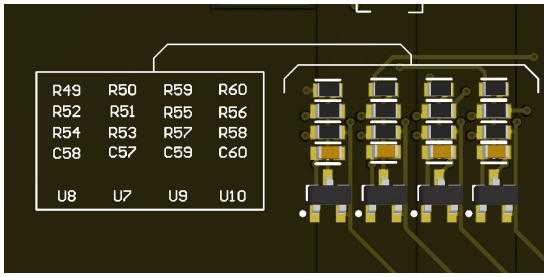


Figure 4.31: 3D view of the power supervisors circuit in the PCB.

Figure 4.32: Power supervisors LED display with -2.5 V rail under threshold voltage.

The 3D routing and placement of the components in this module can be observed in Figure 4.31. The module was positioned on the bottom layer of the PCB, directly underneath the LED display depicted in Figure 4.32.

4.6 Discussion and Results

This chapter offers a comprehensive exploration and analysis of the circuitry employed in the cytometer platform. The current study incorporates a range of novel features designed to overcome limitations identified in the previous platform. By conducting rigorous testing and evaluation, the results obtained provide valuable insights into the enhanced performance and effectiveness of the cytometer platform. This section delves into a detailed discussion, highlighting the achieved accomplishments, while also presenting overall results related to system performance in terms of noise and magnetic field detection.

The analog path in the current platform follows a similar design to the previous iteration. In order to induce changes in resistance when exposed to a magnetic field, the passive sensors require a biasing current. This current is generated by the biasing architecture, which incorporates two distinct topologies within the same module. The first topology involves placing the sensors outside the feedback loop (open-loop), a configuration commonly employed in various other platforms. The second topology entails placing the sensors inside the feedback loop (closed-loop), enabling the op-amp to eliminate noise introduced by the components. It is worth noting that while the implementation of the closed-loop topology falls outside the scope of this thesis, it presents an avenue for future studies. Each of these topologies possesses its own characteristics. The open-loop topology offers a current independent of the sensor's resistance, making it easier to stabilize and allowing for the branching of current into multiple sensors. On the other hand, the closed-loop topology exhibits a current dependent on the sensor's load resistance, making stabilization more challenging. However, it offers a significant advantage in effectively canceling out noise from various sources, except for the reference voltage and the op-amp. The biasing

architecture in both topologies relies on a reference voltage that determines the current supplied to the sensors. In this version, a DAC is implemented to provide the reference voltage, allowing for software control instead of manual adjustment using a potentiometer. In addition to the biasing architecture, the analog path includes an amplification scheme that plays a crucial role in reducing quantization noise associated with digital conversion. This module amplifies the signal from the hundreds of $\mu\mathrm{V}$ to the units of V range, thereby maximizing the dynamic range of the ADCs. Furthermore, this module incorporates a filter to prevent aliasing in the digital signal. The filter's primary purpose is to eliminate undesired frequency components that could distort or corrupt the signal during the analog-to-digital conversion process.

The MR sensors utilized in this study were fabricated at INESC-MN, resulting in a chip containing 28 different MR sensors. To effectively utilize the capabilities of these sensors, a sensor addressing circuit was developed. The purpose of this module is to enable each of the six analog channels to select from a pool of four sensors available on the chip. This provides various opportunities for experimentation and analysis. For example, consider a scenario where two sensors within the same microfluidic channel are utilized for redundant measurements. If a magnetic particle induces a resistance change in both sensors simultaneously, it can be inferred that a particle has indeed passed through the channel, as opposed to being an external interference. Furthermore, envision a situation where three sensors are employed, with one placed in a microfluidic channel that does not have any sample flowing through it, serving as a reference channel. By utilizing the common noise present in all three sensors, optimal particle detection can be achieved by effectively removing the noise component. One limitation of this module relates to the communication requirements for controlling the multiplexers responsible for sensor selection through software. Due to the constraints imposed by the semiconductor shortage during the time of this work, the parallel control of the multiplexers requires an excessive number of inputs. However, to address this issue, a communication translator to SPI was employed. This translator effectively reduced the number of inputs required while ensuring compatibility with the communication protocol used by the reference voltage module.

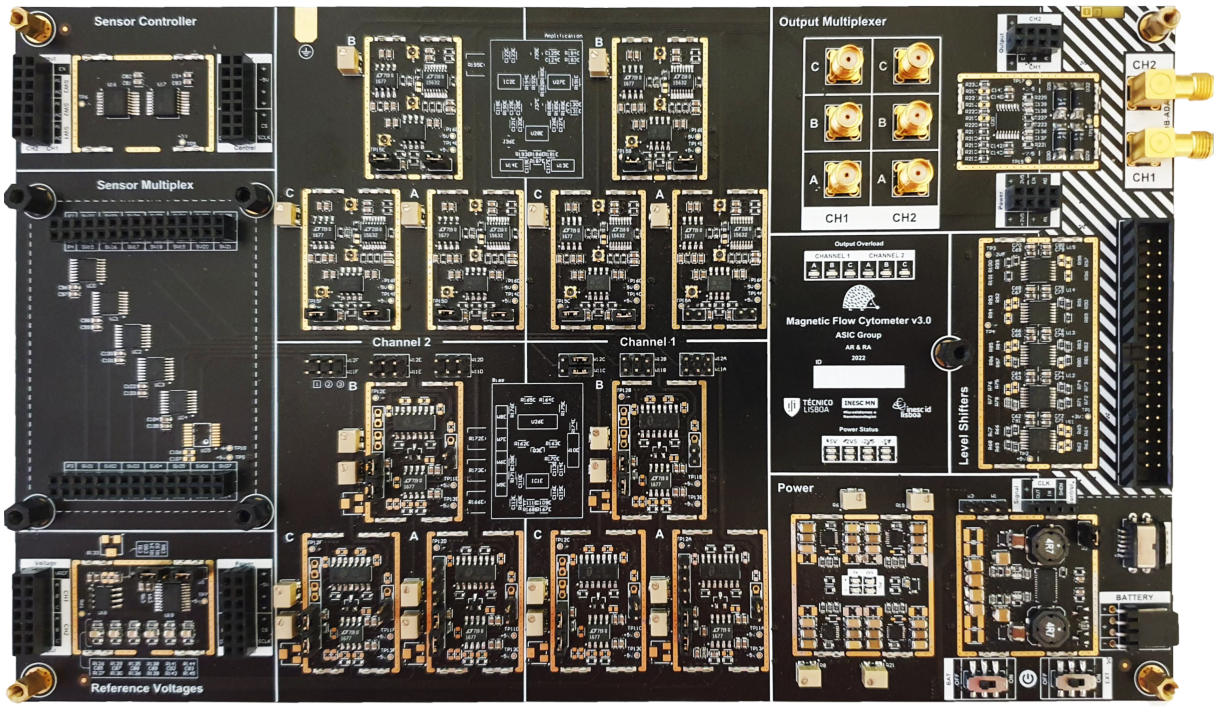
In addition to the analog path, the design of the frontend interface also considered the digital path. Even though, the digital aspect falls beyond the scope of this thesis and is addressed in another thesis that utilizes a THDB-ADA card for signal acquisition and a DE-10 Standard FPGA for real-time signal processing. To overcome the limitations of the ADCs on the card, the outputs of the six channels are attenuated and multiplexed into two outputs. This module carefully considers the sampling rate of the ADCs, allowing to improve the SNR during the DSP. Furthermore, to accommodate the voltage limitation of the FPGA, the input and output signals of the cytometer platform are converted into a voltage range that the FPGA can safely read or write. This conversion ensures compatibility and seamless communication between the cytometer platform and the FPGA.

The power supply configuration of the board underwent a redesign to accommodate the increased supply current demand resulting from the higher number of analog channels. In order to enhance the flexibility of the board, new supply sources were taken into consideration. The board now offers the option to be powered by the FPGA or even by the Jetson Nano via USB connection. To accommodate these new supply sources, an additional circuit had to be implemented to boost and invert the supply voltage. This allows circuit emulates the batteries supply source. To regulate the supply voltages to appropriate power rails for the board's operation a LDO regulator circuit was developed.

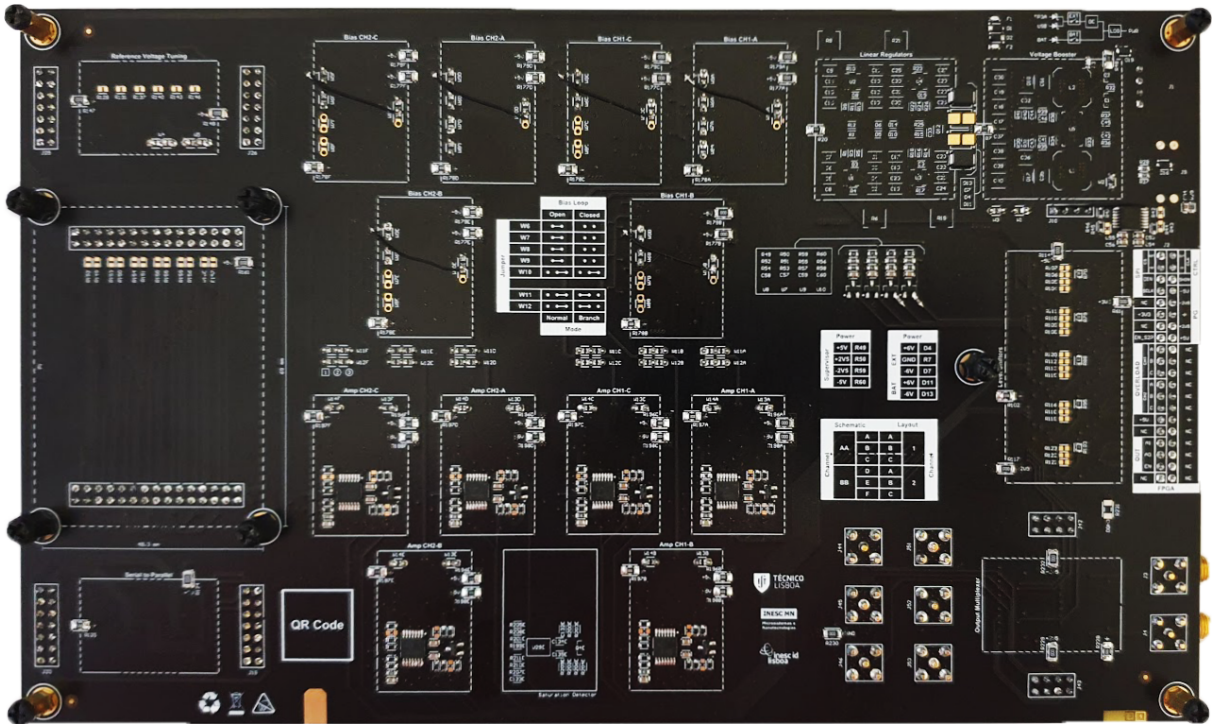
The resulting PCB from this work is displayed in Figure 4.33, illustrating its considerable size due to the absence of space constraints. However, there is potential for easy compaction by separating the modules into distinct PCBs and integrating them together. This board represents the culmination of the 3D models showcased throughout this chapter. In addition to module design and layout considerations, the board design also prioritized the separation of analog and digital signals. A star grounding scheme was implemented, keeping the digital and analog grounds separate and connecting them in the power supply circuit. This design feature effectively minimizes noise and interference, ensuring the integrity and reliability of the signals. Given that digital signals are prone to generating noise and electrical disturbances due to their rapid transitions and high-frequency components, this separation is essential. The star grounding technique effectively reduces ground loop issues, crosstalk, and electromagnetic interference. The work conducted in this thesis also involved the soldering and debugging of the board, addressing some manageable issues that required hotfixes. Figure 4.33a provides a front view of the board, highlighting the key modules, while Figure 4.33b offers a back view, showcasing minor modules such as the saturation detect and power supervisors. It is important to note that all the newly featured modules were designed with contingency plans in case of module failure or malfunction, demonstrating a proactive approach to ensure system robustness and reliability.

Noise Measurements

MR sensors are specifically designed to detect minute changes in magnetic fields by measuring variations in their resistance. These sensors generate extremely small electrical signals in response to magnetic field changes. However, due to the small amplitude of these signals, they are highly susceptible to the presence of noise. Despite their high sensitivity to magnetic fields, MR sensors are also vulnerable to external noise sources. Real-world environments often expose MR sensors to various forms of electromagnetic interference, including power lines, electromagnetic radiation, and nearby electronic devices. These interferences can introduce errors and distort the sensor signals, compromising the accuracy of the measurement results. To ensure reliable and precise measurements, it is of utmost importance that the noise introduced by the interface system is kept significantly lower than the inherent noise of the MR sensors. By minimizing noise-induced fluctuations, the accuracy of magnetic field measurements can be preserved. Therefore, implementing an ultra-low noise interface is essential in order to mitigate the



(a) PCB front-view.



(b) PCB back-view.

Figure 4.33: Cytometer platform version 3.0 PCB.

impact of noise and interference, allowing the MR sensors to perform optimally and providing accurate detection of magnetic field changes.

For the SV sensors used in this application, the two primary sources of noise are flicker noise (also known as pink noise or $1/\mathrm{f}$ noise) and thermal noise (also known as Johnson noise) [13]. In addition to the inherent noise of the sensors themselves ($e^2_{n_{sen}}$), the interface circuitry also contributes to the overall noise level. This includes the biasing architecture($e^2_{n_{bias}}$), sensor addressing ($e^2_{n_{addr}}$), amplification scheme ($e^2_{n_{amp}}$), and output multiplexing ($e^2_{n_{mux}}$). The noise introduced prior to the first amplification stage is particularly significant. As explained before, according to Friis' formula, the total noise figure of each stage is divided by the gain of all preceding stages. Since the first stage has the highest gain, the majority of the system's overall noise is attributed to this initial stage. Noise is characterized as an unwanted disturbance caused by random electrical fluctuations within a device. The total noise of the measurement can be quantified using Equation 4.15.

$$e^2_{n_{total}} = e^2_{n_{sen}} + e^2_{n_{addr}} + e^2_{n_{bias}} + e^2_{n_{amp}} + e^2_{n_{mux}} \quad \left[\frac{V^2}{Hz}\right] \tag{4.15}$$

By carefully designing and optimizing the interface circuitry, it becomes possible to mitigate noise contributions and enhance the SNR. This improvement in SNR leads to enhanced accuracy and reliability of the measurements. To evaluate and quantify the overall noise, a Baseband Signal Analyzer was employed. The analysis involved conducting tests in three different scenarios: shorting the sensor terminal, using a resistance with known thermal noise, and utilizing a MR sensor introducing both thermal and flicker noise. In the first scenario, only the noise from the amplification scheme and output multiplexing is considered, as the inputs of the differential amplifier are shorted. When a resistance is introduced, it incorporates the noise from the biasing, addressing, and thermal components. In the third scenario, the main difference observed should be the presence of a higher flicker noise. Additionally, the system's gain was measured using an Analog Discovery. The results of these measurements are depicted in the figure below:

The measurements presented in Figure 4.34 offer valuable insights into the noise characteristics and gain of the system. The graph displays the measurements for both platforms, with the thicker line representing the interface developed in this work and the thinner line representing the previous interface developed by Eng. Ruben Afonso. Interestingly, despite the incorporation of additional features such as sensor addressing and output multiplexing in this version, the noise was successfully reduced compared to the previous version. This outcome is noteworthy, as the introduction of these features could potentially introduce additional noise. Thus, it was expected to observe similar or higher levels of noise in this version. However, the measurements demonstrate a significant improvement in noise reduction, emphasizing the effectiveness of the design optimizations implemented in this work. This result can be attributed to the biasing architecture, as evidenced by the comparable noise levels observed when the

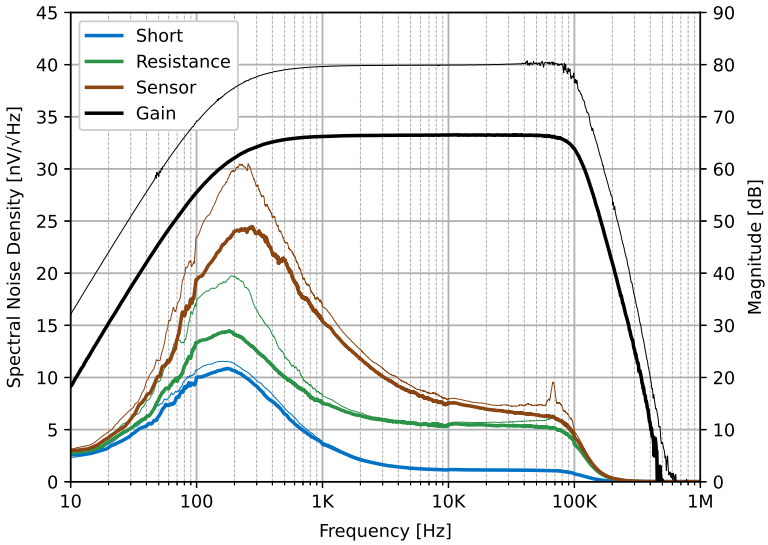


Figure 4.34: Noise measurements – Comparison between the old platform and the one presented in this work.

terminals are shorted. The noise introduced by the sensors addressing is minimal and primarily influenced by the thermal noise of the Ron resistances of the multiplexers. Given that the biasing topology remains similar between the two platforms, the primary difference lies in the reference voltage module. Specifically, the implementation of an XFET reference in the new platform has proven advantageous, offering superior noise performance compared to the previous use of buried Zener references. This successful implementation has effectively reduced the overall noise, even with the addition of additional features. As expected, the flicker noise in the scenario involving the sensor was higher, while the baseline noise should have remained the same in both the resistance and sensor scenarios. However, an incongruous result was obtained where the baseline noise was also higher in the sensor scenario. This unexpected outcome can be attributed to the mismatch in resistance values used for the test. Specifically, the resistance employed had a value of $1\ \mathrm{k\Omega}$, whereas the sensor had a nominal value of $1.2\ \mathrm{k\Omega}$. The difference in gain between the two interfaces can be attributed to the implementation of the output multiplexer circuit. This circuit incorporates voltage dividers to ensure that the output signal adheres to the $2\ \mathrm{V}$ peak-to-peak limitation set by the FPGA ADCs. By using voltage dividers, the signal is properly scaled to match the input range of the ADCs, thus accounting for the disparity in gain observed between the interfaces.

In conclusion, the implemented strategies and circuitry optimizations successfully reduced the noise introduced by the system. Through careful design, noise-reducing techniques, and advanced noise management, the SNR was significantly improved. These efforts resulted in a more robust and reliable interface, enabling accurate measurements in the presence of external noise sources.

Magnetic Field Measurements

In order to conduct thorough testing of the cytometer platform and fulfill its intended purpose, the inclusion of MR sensors was crucial. The platform relies on the presence of a magnetic field to detect and measure changes in the MR sensor resistance. Therefore, it was necessary to generate a magnetic field to stimulate the sensors and evaluate their performance within the cytometer system.

To generate the required magnetic field for the testing of the cytometer platform, a system developed by Eng. Fabian Näf was utilized. This system consists of two coils and a driver power op-amp. The driver power op-amp serves the purpose of amplifying a known sinusoidal waveform, which is then injected into the coils. As per the Biot-Savart law, the current flowing through the coils creates a magnetic field. The configuration of the two coils is crucial to achieve the desired magnetic field characteristics. They are positioned with a specific distance between them in order to create a nearly uniform magnetic field. This specific configuration is commonly referred to as a Helmholtz coil pair, providing a consistent and controlled environment for the MR sensors. By utilizing Fabian's system, comprised of the coils and the driver power op-amp, it was possible to generate the necessary magnetic field to stimulate the MR sensors. This allowed for accurate and reliable testing of the platform's performance and validation of its intended functionality.

One of the performance tests that can be conducted using Fabian's system is the evaluation of harmonic distortion in the cytometer platform. Harmonics are additional frequencies that were not present in the original signal and alter the waveform shape, a common occurrence in electronic systems and circuits. However, in many cases, harmonics are undesirable and can be considered as noise or distortion. When harmonics are present in a system, they have the potential to interfere with the desired signal and introduce distortion or degradation in signal quality. This can lead to inaccurate signal representation or the presence of unwanted artifacts. Therefore, it becomes crucial to manage harmonic distortion by attenuating these unwanted harmonic components. By ensuring appropriate harmonic attenuation, signal integrity can be maintained, and distortion can be minimized. This is particularly important in the context of the cytometer platform, a sensitivity application, that requires an accurate and reliable signal detection and analysis.

Figure 4.35 depicts the results of the harmonic performance analysis of the system. The test involved two experiments, each utilizing a magnetic field with different frequencies. The blue trace represents the $1\ \mathrm{kHz}$ frequency, while the green trace represents the $10\ \mathrm{kHz}$ frequency. In the blue trace, it is evident that the system exhibits an impressive attenuation of approximately $70\ \mathrm{dB}$ between the 2$^{\text{nd}}$ harmonic and the 1$^{\text{st}}$ harmonic at a fundamental frequency of $1\ \mathrm{kHz}$. This level of attenuation is especially desirable in this sensitive application, as it ensures precise signal reproduction and minimizes distortion. Achieving such a high level of attenuation is crucial for maintaining signal integrity and fidelity. The attenuation observed in the green trace is lower than the blue trace, but this is primarily attributed to the frequency response characteristics of the Helmholtz coil driver rather than the platform itself. The coil

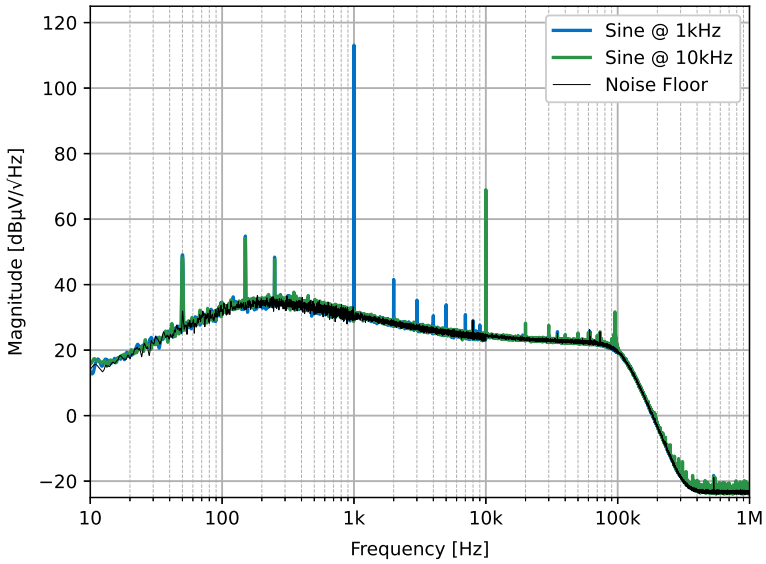


Figure 4.35: Magnetic field measurements.

driver operates based on voltage, and the voltage value was adjusted to maximize the dynamic range of the system, reaching a peak-to-peak voltage of $2\ \mathrm{V}$. However, it is important to note that the magnitude of the magnetic field is determined by the current flowing through the coil, not the voltage. As the frequency increases, the reactance of the coil, also known as the ”coil resistance,” begins to rise. The used Helmholtz coil has an inductance of $538\ \mu\mathrm{H}$, which results in a reactance of $3.38\ \Omega$ at $1\ \mathrm{kHz}$ and 33.8Ω at $10\ \mathrm{kHz}$. Since the voltage remains constant, the current flowing through the coil is reduced to compensate for the increasing resistance. Consequently, the magnitude of the magnetic field produced by the coil decreases at higher frequencies. The observed decrease in the magnetic field magnitude at higher frequencies is a consequence of the interplay between the coil resistance, voltage, and current.

The harmonic performance results demonstrate the system’s capability to effectively suppress undesired harmonic components and preserve the integrity of the desired signal. These findings highlight the system’s suitability for applications requiring accurate and distortion-free signal processing.

5

Conclusion

Preamble

This chapter offers a concise and formal overview of the research conducted. It includes a comprehensive review of the main findings and important observations made throughout the study. Critical remarks are provided, addressing any limitations and challenges encountered. Additionally, the future work section outlines potential areas for further exploration and improvement, providing a roadmap for future studies. Overall, this chapter serves as a conclusive summary, offering valuable insights and guiding future advancements in the field.

Contents

5.1 Review and Remarks

The research described in this dissertation consists of an discrete electronics system for interfacing MR sensors, featuring a fully analog path, from the sensor bias to digital conversion. However, the new platform has to consider the specifications defined for the early cancer diagnosis application. The noise generated within the analog path is propagated to the output, degrading the overall quality of the measurement. Thus, it was required to develop an ultra-low noise state-of-the-art interface. The cytometer platform conceived in this dissertation enriched an existing MFC prototype developed in INESC.

Significant changes were introduced to the biasing architecture, impacting various aspects, including the reference voltage used throughout the system. The ability to digitally and effortlessly adjust the reference voltage was incorporated into the design, providing flexibility and control. Furthermore, the biasing topology was carefully engineered to seamlessly switch between two distinct configurations. These configurations differ in the placement of the sensor relative to the feedback loop. One configuration involves positioning the sensor inside the feedback loop, while the other maintains the sensor outside the loop. The intention behind implementing two different topologies was to explore potential improvements in reducing noise introduced by the biasing architecture. However, as this represents a novel approach, the effectiveness of the sensor placement within the feedback loop has yet to be substantiated by empirical evidence. In the event that the new topology fails to meet expectations, the previous configuration, with the sensor positioned outside the feedback loop, can serve as a fallback option. This alternative ensures the continuity of the system's functionality and mitigates risks associated with unproven methodologies. Additionally, apart from these significant changes, the architecture also tackled noise-related concerns through the utilization of an alternative reference voltage generator. This modification aimed to further enhance the system's performance and minimize noise interference.

The amplification scheme, which played a crucial role in enhancing the signal response of the sensors, remained unchanged in terms of the circuit design. However, certain modifications were made to incorporate specific switches that facilitate noise measurement and enable potential tests within the circuit. This enhancement further contributes to the overall understanding and refinement of the amplification scheme's performance within the system. In addition to these changes, the saturation detector circuit of the first amplification stage has been improved. This fix allows for not only computer-based detection but also visual identification of saturation, regardless of the duration of the saturation event. By incorporating this fix, the means of detecting saturation have expanded, providing a comprehensive approach to monitor and address potential signal saturation issues.

A new circuit was developed to cater to the majority of sensors within the sensor chip. This enables each of the 6 analog channels to select at least 4 distinct sensors. This capability is particularly valuable since the chip houses a total of 28 sensors, organized across 8 microfluidic channels. While this new feature is undoubtedly important and beneficial, it does come with the minor drawback of requiring an

additional circuitry module to control the multiplexers used for this purpose. The introduction of this new circuit represents a significant advancement in sensor integration and utilization. By expanding the selection options for each analog channel, the system gains versatility in addressing different sensors within the chip. This flexibility allows for a more comprehensive analysis of various samples, enhancing the overall capabilities of the platform.

In order to seamlessly integrate the interface within the larger MFC system, supplementary circuits were developed to accommodate the limitations of the subsequent systems, particularly the FPGA. As a result, careful considerations were made regarding the digital path of the interface. To overcome the limitations imposed by the number of available ADCs and their input voltage range, a gain reduction multiplexing circuit was implemented. This module was specifically designed with the intention that the bottleneck lies on the FPGA side rather than the interface itself. By implementing this circuit, the interface can effectively optimize the usage of ADCs, ensuring efficient utilization of resources and maximizing the system's overall performance. Additionally, to facilitate compatibility with not only the FPGA but also other potential control systems, level shifters were employed for all the required inputs and outputs of the interface. This enables seamless communication and interaction between the interface and various external systems, ensuring compatibility and ease of integration.

In response to the heightened demand for supply current resulting from the increased number of analog channels, the power supply configuration of the board underwent a thorough redesign. This redesign aimed to effectively accommodate the higher power requirements and ensure optimal performance. In addition to addressing the increased demand, the redesign also aimed to enhance the flexibility of the board by considering new supply sources. The board now offers expanded options for powering, including the FPGA or a USB connection as a power source. These additions provide greater versatility and convenience in powering the board, alongside the previous power source from batteries. By incorporating these improvements to the power supply configuration, the board gains enhanced flexibility, ensuring compatibility with different power sources and providing users with more options for powering the system. This optimization supports efficient operation and contributes to the overall usability of the board in diverse settings.

In conclusion, the research presented in this dissertation has made significant contributions to the development of a robust and advanced discrete electronics system for interfacing MR sensors. The proposed improvements and advancements in circuit design, biasing architecture, amplification scheme, sensor integration, digital system integration, and power supply configuration lay the foundation for further advancements in the MFC system. The comprehensive understanding gained through this document enables to delve deeper into the intricacies of MR sensor interfacing and leverage the advancements made to drive further breakthroughs in early cancer diagnosis and related applications.

5.2 Future Work

This section outlines potential future work that can build upon the achievements and advancements made in this thesis. While significant progress has been made in developing a robust electronics system for interfacing MR sensors, there are still opportunities for further exploration and improvement. The following paragraphs provide an overview of potential areas for future research and development, including interface tests, application tests, and future interface versions.

A specific focus on testing the ”closed-loop” bias topology and the new supply features, it is essential to highlight the significance of evaluating their noise performance. By conducting thorough tests and analyses, researchers can gain insights into the effectiveness of these features in reducing noise interference. The biasing topology with the sensor outside the biasing feedback loop allows the op-amp to mitigate some of the noise the topology introduces. Additionally, synchronizing the acquisition clock signal with the SEPIC and inverting circuit can contribute to minimizing the impact of ripple noise on the system. These areas warrant further investigation to optimize the noise characteristics of the system and ensure its robust performance in practical applications.

In addition to conducting interface tests, it is crucial to carry out real experiments involving magnetic fields generated by magnetic nanoparticles. These experiments will serve as concrete evidence of the effectiveness of the developed interface in fulfilling its intended purpose. Furthermore, the results obtained can be compared with those obtained using the previous platform, allowing for an evaluation of the overall benefits of the new system. Additionally, it is essential to integrate the findings and developments from other theses conducted concurrently with this work. This integration will provide a comprehensive assessment of the desired MFC system and enable a thorough understanding of its potential advantages and contributions.

In future iterations of the cytometer platform, the anticipated resolution of the semiconductor shortage opens up opportunities for improvement. The selection of alternative multiplexers that align with the interface objectives becomes crucial. The current multiplexers used in the sensor addressing circuit introduce unnecessary complexity due to their communication protocol and the excessive number of inputs. Additionally, the power rail requirements of the multiplexers in the output multiplexing circuit differ from other ICs, necessitating the generation of two additional power rails. Therefore, exploring alternative multiplexer options is essential for future platform versions. Despite the absence of space constraints, the developed interface remains relatively large. However, the modular design allows for a seamless transition to a more compact system if desired. Partitioning the current platform into multiple boards, like the previous platform, enables flexibility and scalability. Another idea for reducing space further is to implement analog channels on small PCBs with gold fingers, facilitating their insertion similar to a memory stick in a computer.

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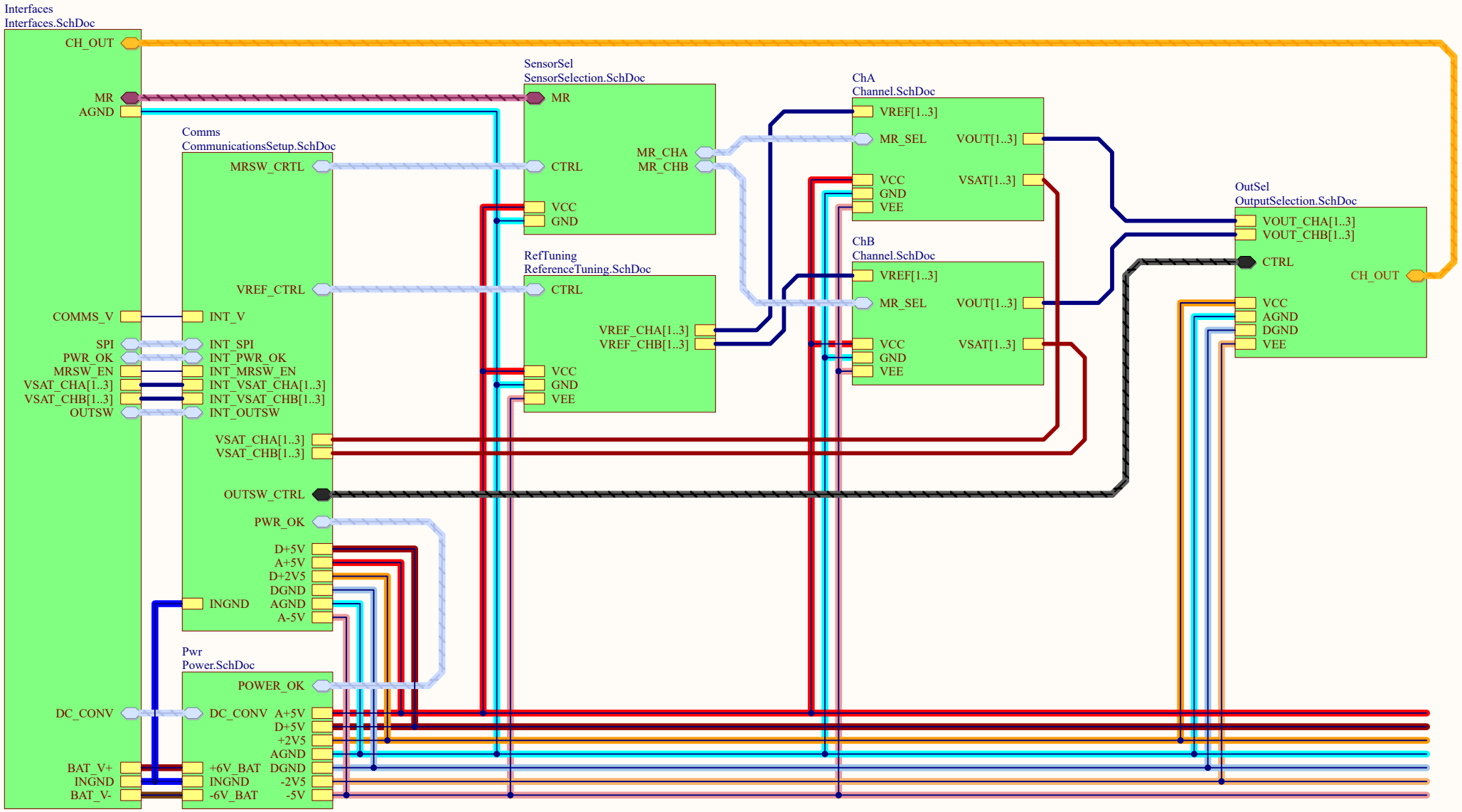
Circuit Schematics



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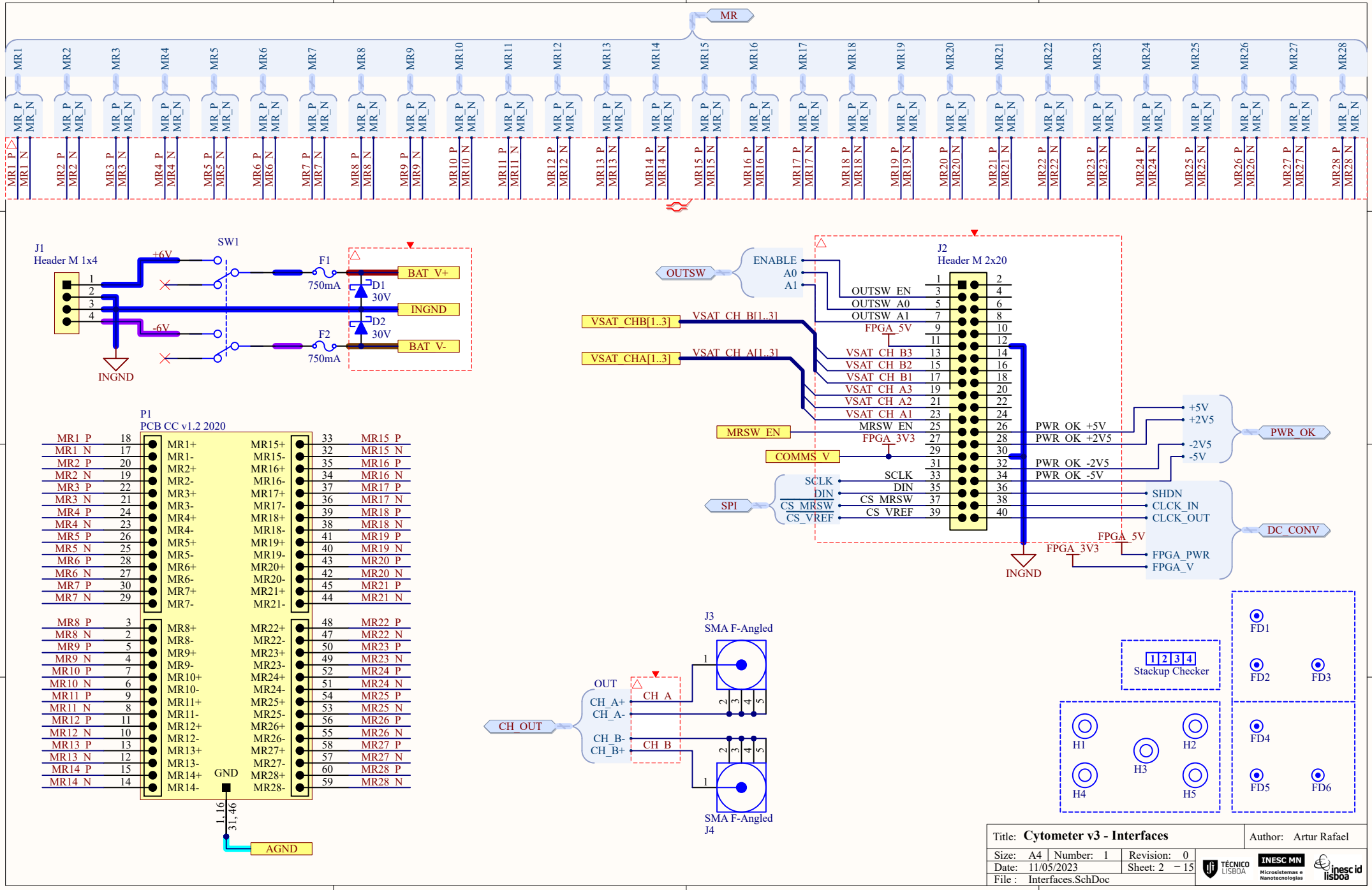

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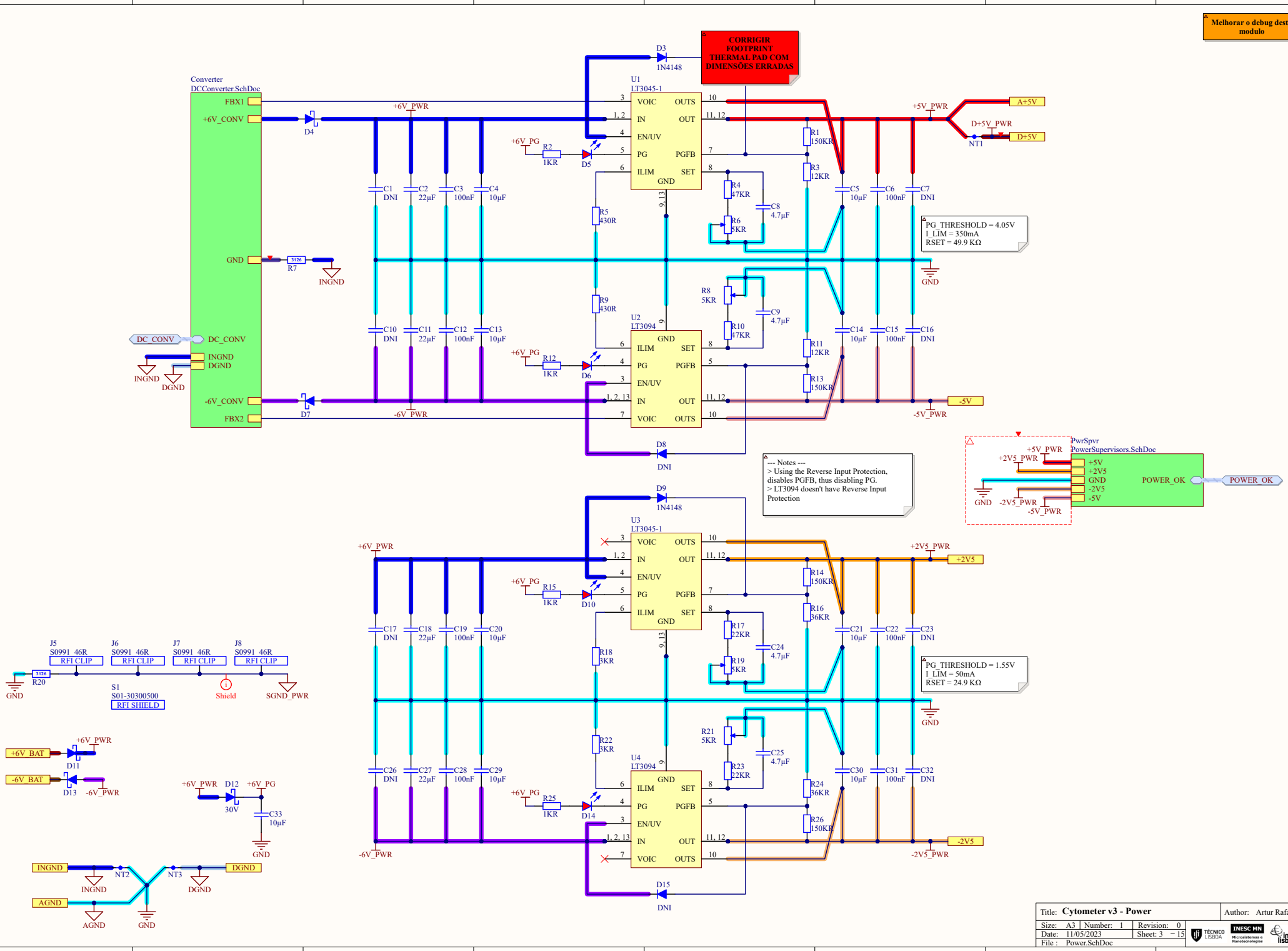
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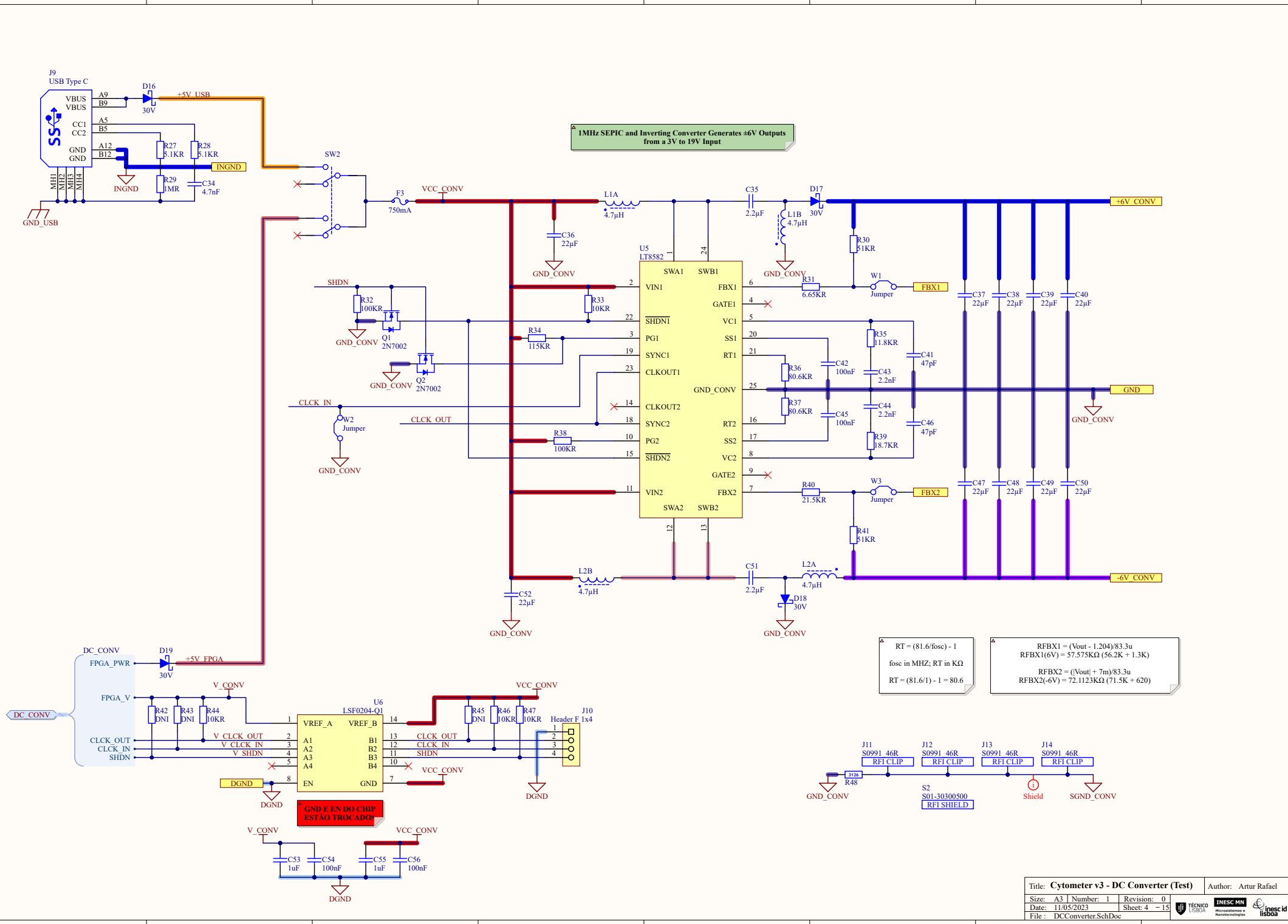
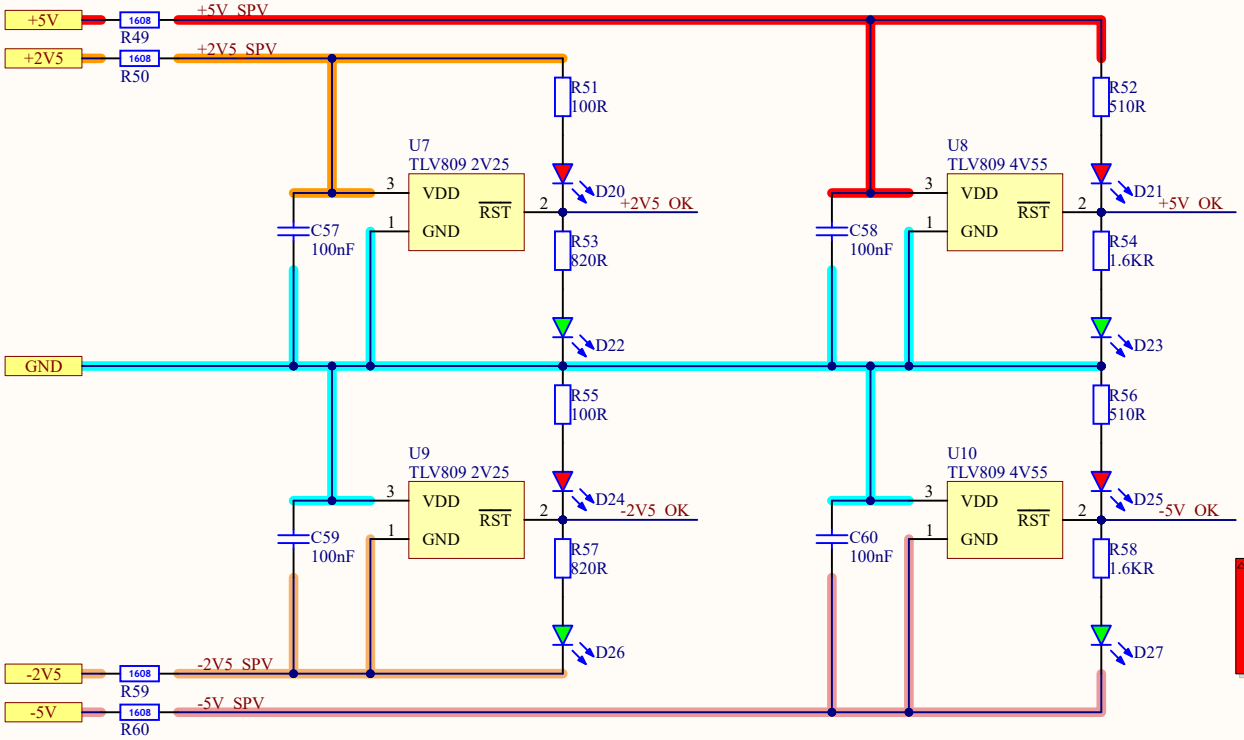
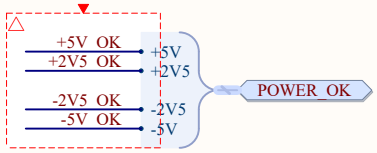
RSET = 49.9 KΩ
PG_THRESHOLD = 1.55V
I_LIM = 50mA
RSET = 24.9 KΩ
--- Notes ---
> Using the Reverse Input Protection, disables PGFB, thus disabling PG.
> LT3094 doesn't have Reverse Input Protection
PwrSpvr
PowerSupervisors.SchDoc
POWER_OK
J5
J6
J7
J8
S0991_46R
RFI CLIP
S1
S01-30300500
RFI SHIELD
Shield
SGND_PWR
+6V_BAT
-6V_BAT
INGND
DGND
AGND
NT2
NT3
Title: Cytometer v3 - Power
Author: Artur Rafael
Size: A3
Number: 1
Revision: 0
Date: 11/05/2023
Sheet: 3 – 15
File : Power.SchDoc



Title:	Cytometer v3 - DC Converter (Test)	Author:	Artur Rafael
Size:	A3	Number:	1
Revision:	0		
Date:	11/05/2023	Sheet:	4 – 15
File :	DCConverter.SchDoc		

Arranjar uns supervisors que vejam um intervalo de voltagens, em vez de apenas a tensão acima de um valor (como é o caso destes)





LEDS VERMELHOS NÃO ACENDEM COM OS LEVEL SHIFTERS SOLDADOS PORQUE TÊM UM SISTEMA DE PROTEÇÃO DE INPUTS, É NECESSÁRIO TRANSFORMAR O SINAL DE RST A VARIAR ENTRE 0 E 5 VOLTS

Title: Cytometer v3 - Power Supervisors			Author: Artur Rafael
Size: A4	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 5 – 15	
File : PowerSupervisors.SchDoc			

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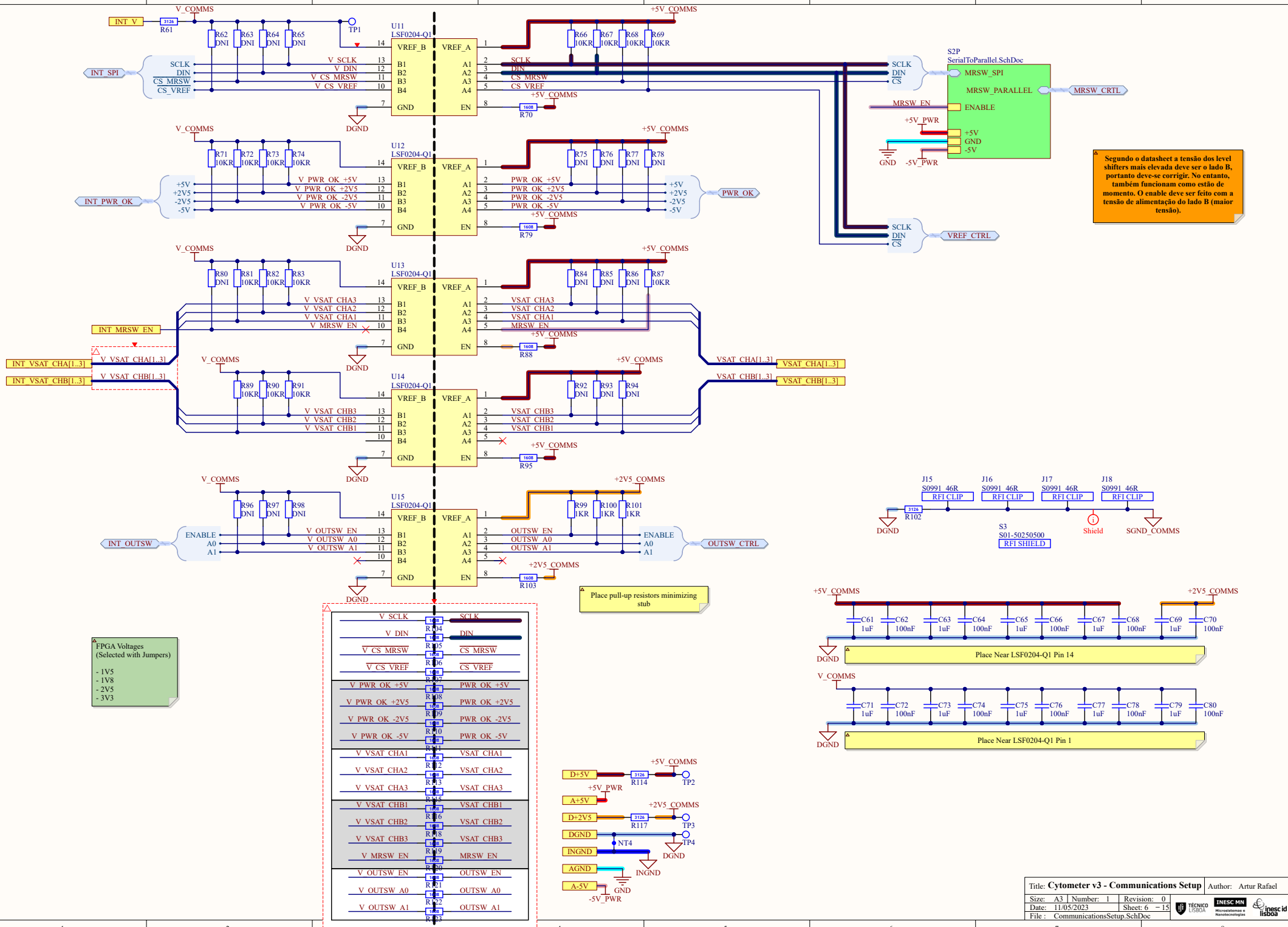
V_COMMS
INT_V
R61
TP1
R62 DNI
R63 DNI
R64 DNI
R65 DNI
U11
LSF0204-Q1
VREF_B
VREF_A
INT_SPI
SCLK
DIN
CS_MRSW
CS_VREF
V_SCLK
V_DIN
V_CS_MRSW
V_CS_VREF
GND
EN
DGND
+5V_COMMS
R66 10KR
R67 10KR
R68 10KR
R69 10KR
R70
S2P
SerialToParallel.SchDoc
MRSW_SPI
MRSW_PARALLEL
MRSW_CRTL
MRSW_EN
ENABLE
+5V_PWR
+5V
GND
-5V
-5V_PWR
U12
R71 10KR
R72 10KR
R73 10KR
R74 10KR
INT_PWR_OK
+5V
+2V5
-2V5
-5V
V_PWR_OK_+5V
V_PWR_OK_+2V5
V_PWR_OK_-2V5
V_PWR_OK_-5V
PWR_OK_+5V
PWR_OK_+2V5
PWR_OK_-2V5
PWR_OK_-5V
R75 DNI
R76 DNI
R77 DNI
R78 DNI
PWR_OK
R79
SCLK
DIN
CS
VREF_CTRL
Segundo o datasheet a tensão dos level shifters mais elevada deve ser o lado B, portanto deve-se corrigir. No entanto, também funcionam como estão de momento. O enable deve ser feito com a tensão de alimentação do lado B (maior tensão).
U13
R80 DNI
R81 10KR
R82 10KR
R83 10KR
INT_MRSW_EN
INT_VSAT_CHA[1..3]
INT_VSAT_CHB[1..3]
V_VSAT_CHA[1..3]
V_VSAT_CHB[1..3]
V_VSAT_CHA3
V_VSAT_CHA2
V_VSAT_CHA1
V_MRSW_EN
VSAT_CHA3
VSAT_CHA2
VSAT_CHA1
MRSW_EN
R84 DNI
R85 DNI
R86 DNI
R87 10KR
R88
VSAT_CHA[1..3]
VSAT_CHB[1..3]
U14
R89 10KR
R90 10KR
R91 10KR
V_VSAT_CHB3
V_VSAT_CHB2
V_VSAT_CHB1
VSAT_CHB3
VSAT_CHB2
VSAT_CHB1
R92 DNI
R93 DNI
R94 DNI
R95
U15
R96 DNI
R97 DNI
R98 DNI
INT_OUTSW
ENABLE
A0
A1
V_OUTSW_EN
V_OUTSW_A0
V_OUTSW_A1
OUTSW_EN
OUTSW_A0
OUTSW_A1
+2V5_COMMS
R99 1KR
R100 1KR
R101 1KR
OUTSW_CTRL
R103
Place pull-up resistors minimizing stub
J15 S0991_46R RFI CLIP
J16 S0991_46R RFI CLIP
J17 S0991_46R RFI CLIP
J18 S0991_46R RFI CLIP
R102
S3
S01-50250500
RFI SHIELD
Shield
SGND_COMMS
FPGA Voltages
(Selected with Jumpers)
- 1V5
- 1V8
- 2V5
- 3V3
R104
R105
R106
R107
R108
R109
R110
R111
R112
R113
R115
R116
R118
R119
R120
R121
R122
R123
D+5V
R114
TP2
+5V_PWR
A+5V
D+2V5
R117
TP3
NT4
TP4
INGND
AGND
A-5V
C61 1uF
C62 100nF
C63 1uF
C64 100nF
C65 1uF
C66 100nF
C67 1uF
C68 100nF
C69 1uF
C70 100nF
Place Near LSF0204-Q1 Pin 14
C71 1uF
C72 100nF
C73 1uF
C74 100nF
C75 1uF
C76 100nF
C77 1uF
C78 100nF
C79 1uF
C80 100nF
Place Near LSF0204-Q1 Pin 1
Title: Cytometer v3 - Communications Setup
Author: Artur Rafael
Size: A3
Number: 1
Revision: 0
Date: 11/05/2023
Sheet: 6 – 15
File: CommunicationsSetup.SchDoc
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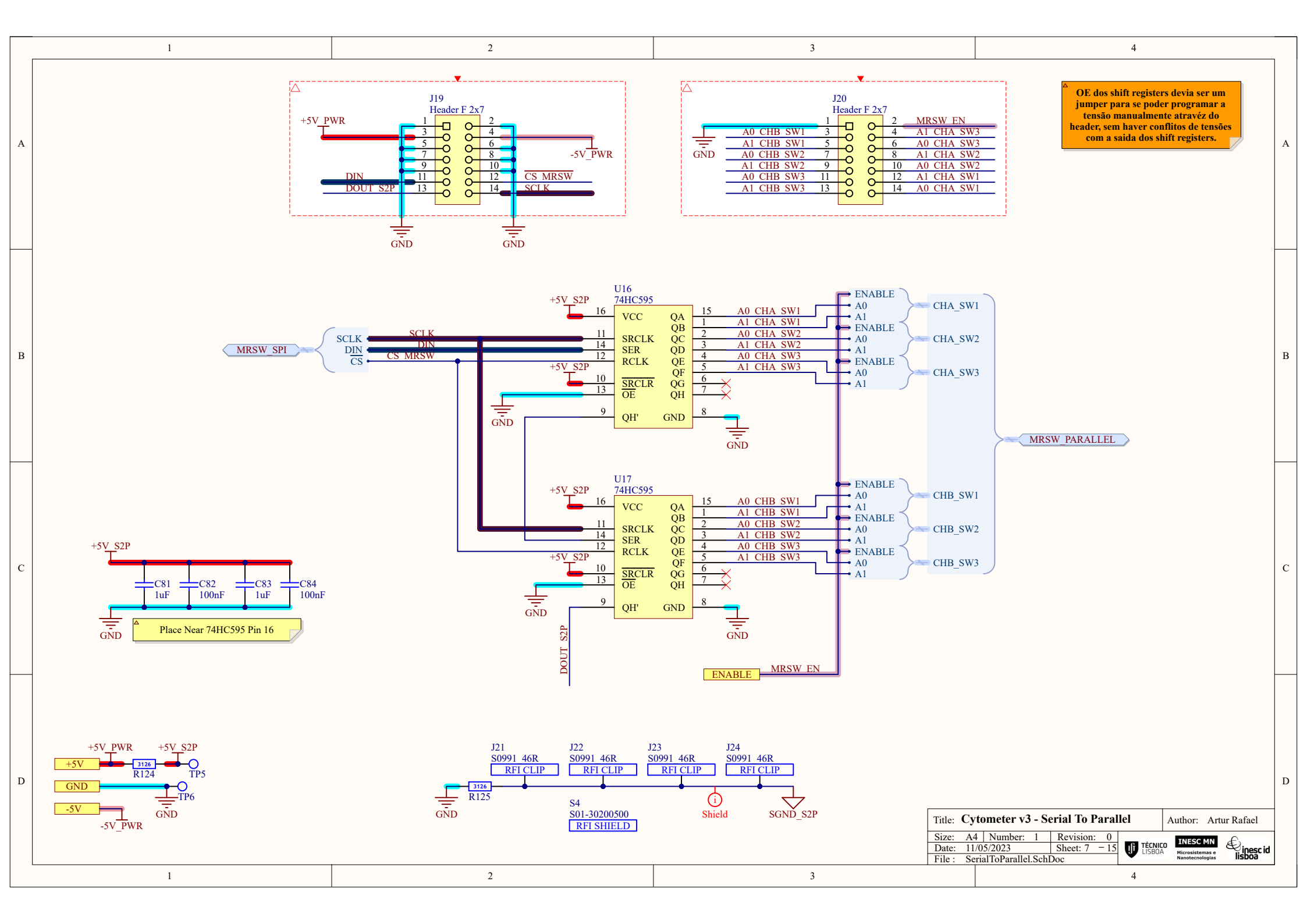
J19
Header F 2x7
+5V_PWR
-5V_PWR
DIN
DOUT_S2P
CS_MRSW
SCLK
GND
J20
Header F 2x7
MRSW_EN
A0_CHB_SW1
A1_CHB_SW1
A0_CHB_SW2
A1_CHB_SW2
A0_CHB_SW3
A1_CHB_SW3
A1_CHA_SW3
A0_CHA_SW3
A1_CHA_SW2
A0_CHA_SW2
A1_CHA_SW1
A0_CHA_SW1
OE dos shift registers devia ser um jumper para se poder programar a tensão manualmente atravéz do header, sem haver conflitos de tensões com a saida dos shift registers.
U16
74HC595
U17
74HC595
VCC
SRCLK
SER
RCLK
SRCLR
OE
QH'
QA
QB
QC
QD
QE
QF
QG
QH
GND
+5V_S2P
MRSW_SPI
SCLK
DIN
CS
CS_MRSW
ENABLE
A0
A1
CHA_SW1
CHA_SW2
CHA_SW3
CHB_SW1
CHB_SW2
CHB_SW3
MRSW_PARALLEL
MRSW_EN
C81
1uF
C82
100nF
C83
1uF
C84
100nF
Place Near 74HC595 Pin 16
+5V_PWR
+5V
GND
-5V
-5V_PWR
R124
3126
TP5
TP6
J21
J22
J23
J24
S0991_46R
RFI CLIP
R125
S4
S01-30200500
RFI SHIELD
Shield
SGND_S2P
Title: Cytometer v3 - Serial To Parallel
Author: Artur Rafael
Size: A4
Number: 1
Revision: 0
Date: 11/05/2023
Sheet: 7 – 15
File : SerialToParallel.SchDoc
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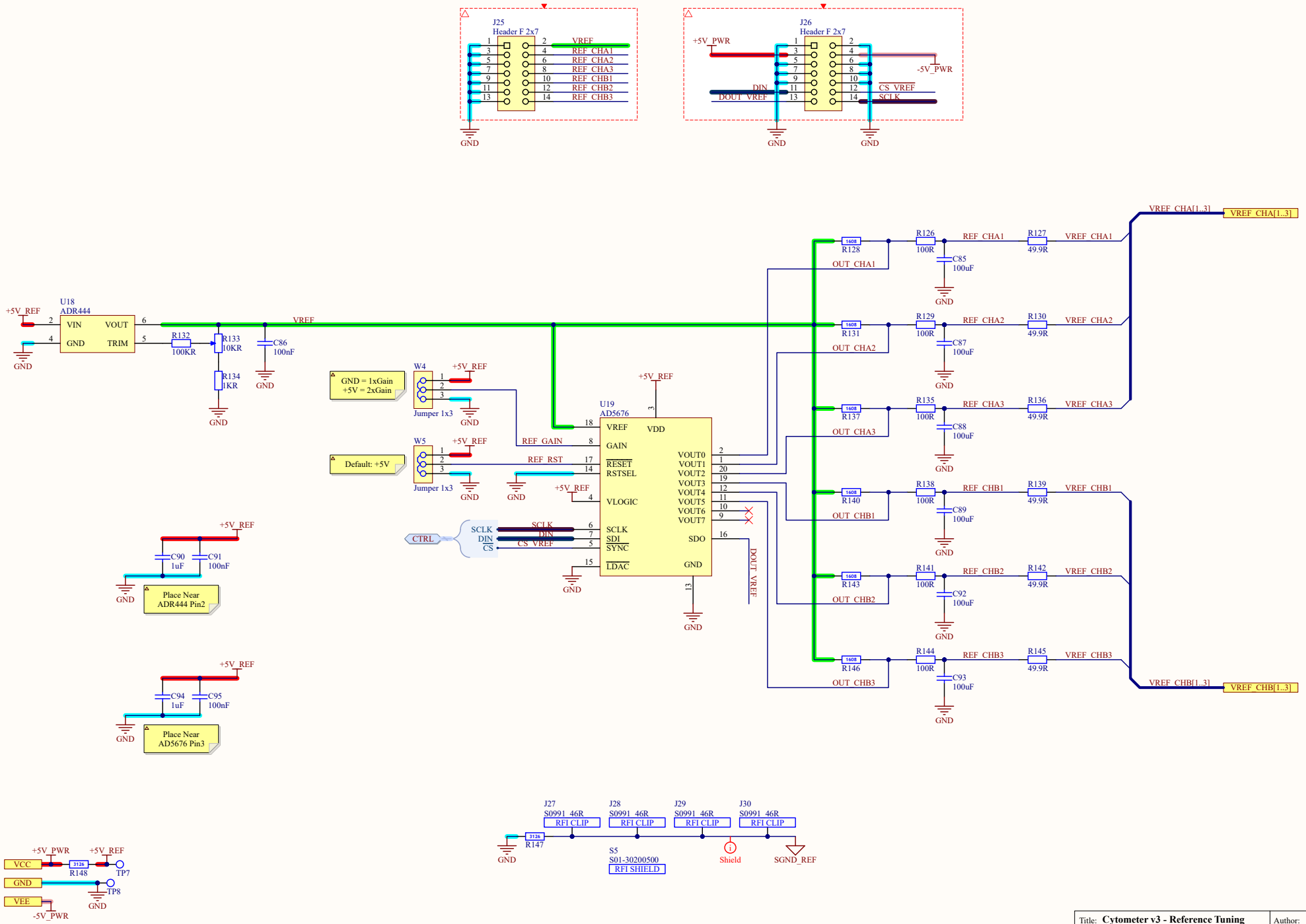
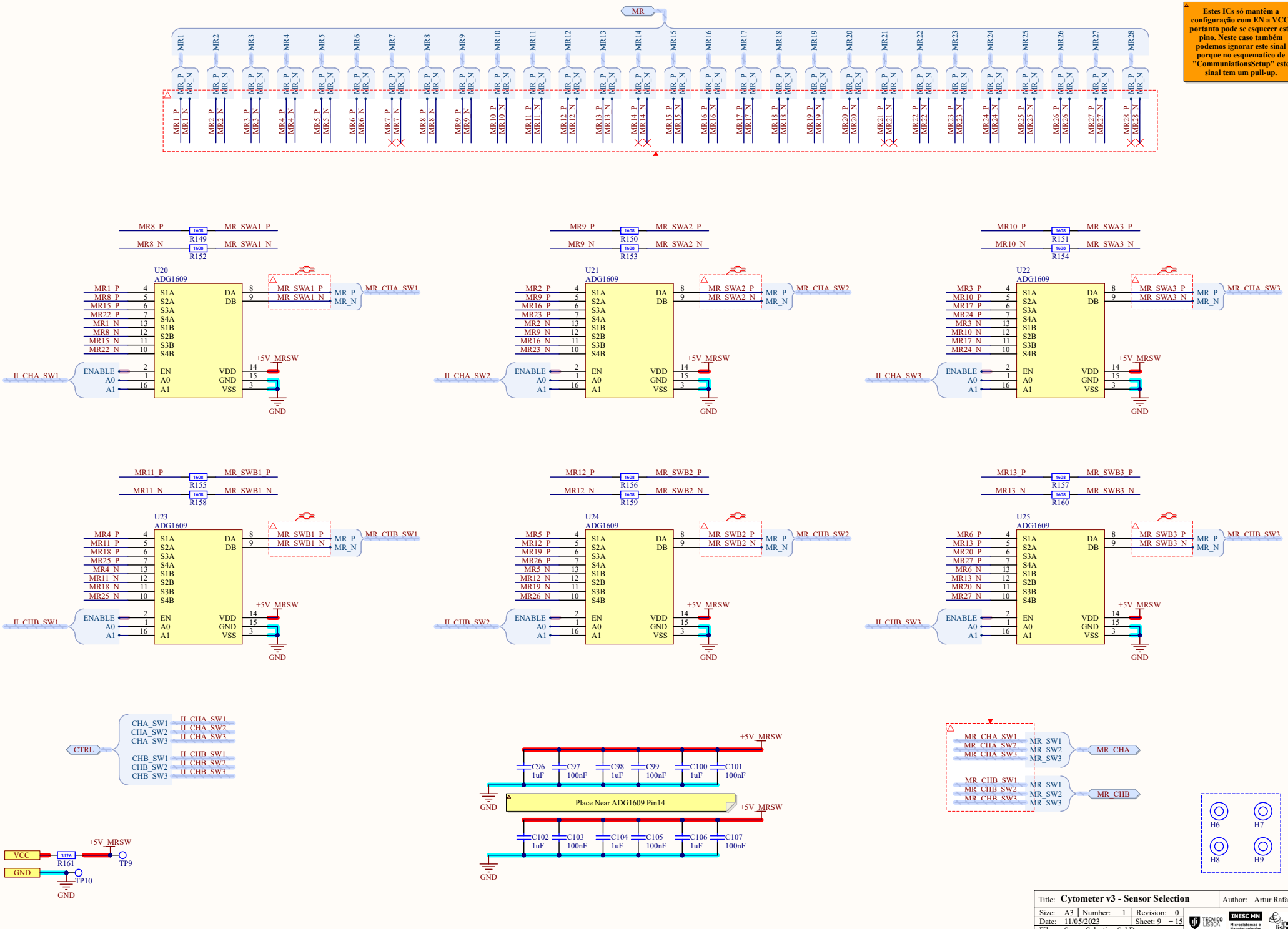


Title:	**Cytometer v3 - Reference Tuning**		Author: Artur Rafael
Size: A3	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 8 – 15	
File : ReferenceTuning.SchDoc			


MR
MR1 MR2 MR3 MR4 MR5 MR6 MR7 MR8 MR9 MR10 MR11 MR12 MR13 MR14 MR15 MR16 MR17 MR18 MR19 MR20 MR21 MR22 MR23 MR24 MR25 MR26 MR27 MR28
MR_P MR_N
MR1_P MR1_N MR2_P MR2_N MR3_P MR3_N MR4_P MR4_N MR5_P MR5_N MR6_P MR6_N MR7_P MR7_N MR8_P MR8_N MR9_P MR9_N MR10_P MR10_N MR11_P MR11_N MR12_P MR12_N MR13_P MR13_N MR14_P MR14_N MR15_P MR15_N MR16_P MR16_N MR17_P MR17_N MR18_P MR18_N MR19_P MR19_N MR20_P MR20_N MR21_P MR21_N MR22_P MR22_N MR23_P MR23_N MR24_P MR24_N MR25_P MR25_N MR26_P MR26_N MR27_P MR27_N MR28_P MR28_N
Estes ICs só mantêm a configuração com EN a VCC, portanto pode se esquecer este pino. Neste caso também podemos ignorar este sinal porque no esquematico de "CommuniationsSetup" este sinal tem um pull-up.
MR8_P MR8_N R149 R152 MR_SWA1_P MR_SWA1_N
U20 ADG1609
MR1_P MR8_P MR15_P MR22_P MR1_N MR8_N MR15_N MR22_N
S1A S2A S3A S4A S1B S2B S3B S4B DA DB
MR_SWA1_P MR_SWA1_N MR_P MR_N MR_CHA_SW1
II_CHA_SW1 ENABLE A0 A1 EN A0 A1 VDD GND VSS +5V_MRSW GND
MR9_P MR9_N R150 R153 MR_SWA2_P MR_SWA2_N
U21 ADG1609
MR2_P MR9_P MR16_P MR23_P MR2_N MR9_N MR16_N MR23_N
MR_SWA2_P MR_SWA2_N MR_P MR_N MR_CHA_SW2
II_CHA_SW2 +5V_MRSW GND
MR10_P MR10_N R151 R154 MR_SWA3_P MR_SWA3_N
U22 ADG1609
MR3_P MR10_P MR17_P MR24_P MR3_N MR10_N MR17_N MR24_N
MR_SWA3_P MR_SWA3_N MR_P MR_N MR_CHA_SW3
II_CHA_SW3 +5V_MRSW GND
MR11_P MR11_N R155 R158 MR_SWB1_P MR_SWB1_N
U23 ADG1609
MR4_P MR11_P MR18_P MR25_P MR4_N MR11_N MR18_N MR25_N
MR_SWB1_P MR_SWB1_N MR_P MR_N MR_CHB_SW1
II_CHB_SW1 +5V_MRSW GND
MR12_P MR12_N R156 R159 MR_SWB2_P MR_SWB2_N
U24 ADG1609
MR5_P MR12_P MR19_P MR26_P MR5_N MR12_N MR19_N MR26_N
MR_SWB2_P MR_SWB2_N MR_P MR_N MR_CHB_SW2
II_CHB_SW2 +5V_MRSW GND
MR13_P MR13_N R157 R160 MR_SWB3_P MR_SWB3_N
U25 ADG1609
MR6_P MR13_P MR20_P MR27_P MR6_N MR13_N MR20_N MR27_N
MR_SWB3_P MR_SWB3_N MR_P MR_N MR_CHB_SW3
II_CHB_SW3 +5V_MRSW GND
CTRL
CHA_SW1 CHA_SW2 CHA_SW3 CHB_SW1 CHB_SW2 CHB_SW3
II_CHA_SW1 II_CHA_SW2 II_CHA_SW3 II_CHB_SW1 II_CHB_SW2 II_CHB_SW3
VCC GND R161 TP9 TP10 +5V_MRSW GND
+5V_MRSW
C96 C97 C98 C99 C100 C101 1uF 100nF 1uF 100nF 1uF 100nF
GND
Place Near ADG1609 Pin14
+5V_MRSW
C102 C103 C104 C105 C106 C107 1uF 100nF 1uF 100nF 1uF 100nF
GND
MR_CHA_SW1 MR_CHA_SW2 MR_CHA_SW3 MR_CHB_SW1 MR_CHB_SW2 MR_CHB_SW3
MR_SW1 MR_SW2 MR_SW3 MR_CHA MR_CHB
H6 H7 H8 H9
Title: Cytometer v3 - Sensor Selection
Author: Artur Rafael
Size: A3 Number: 1 Revision: 0
Date: 11/05/2023 Sheet: 9 – 15
File : SensorSelection.SchDoc
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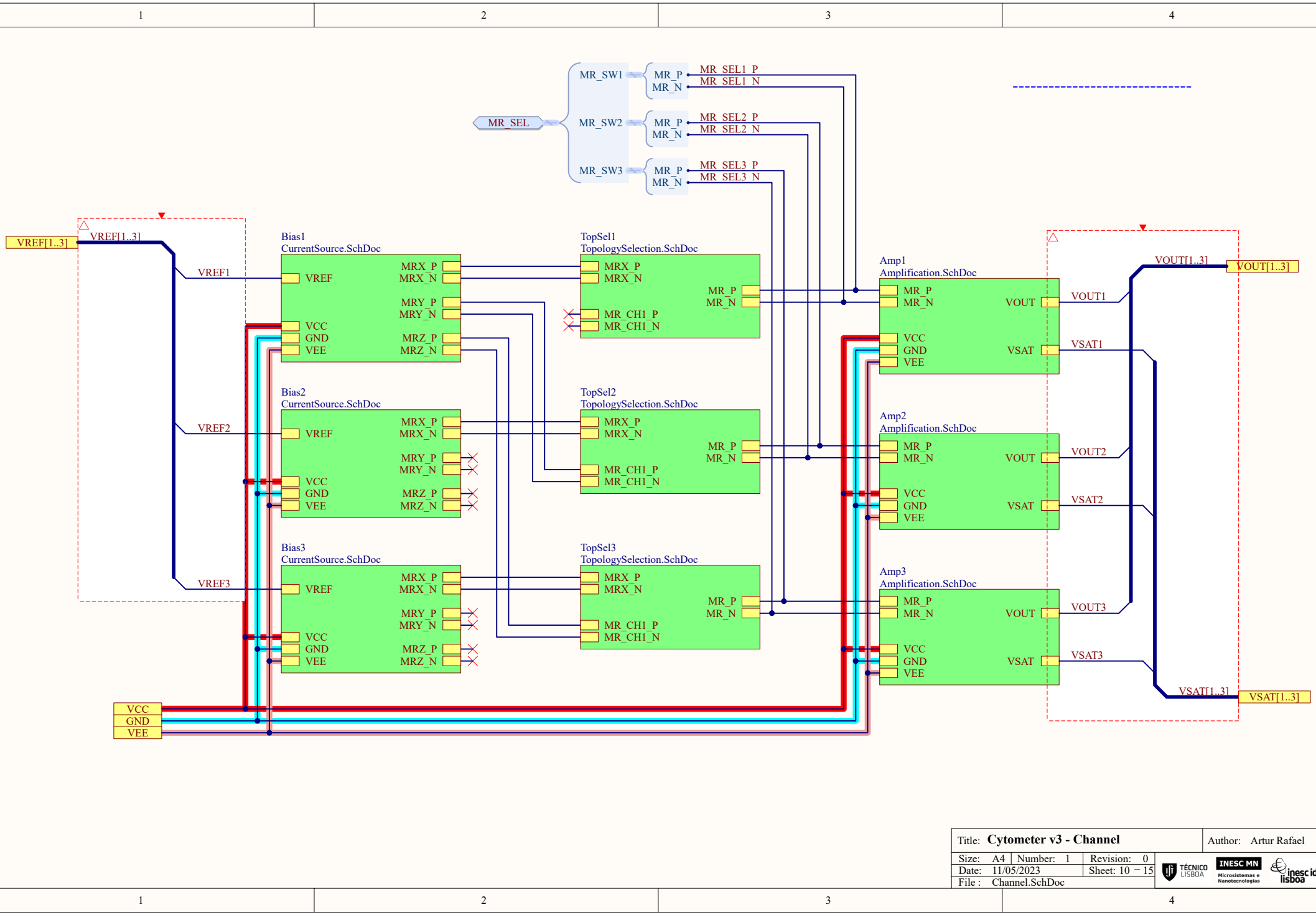
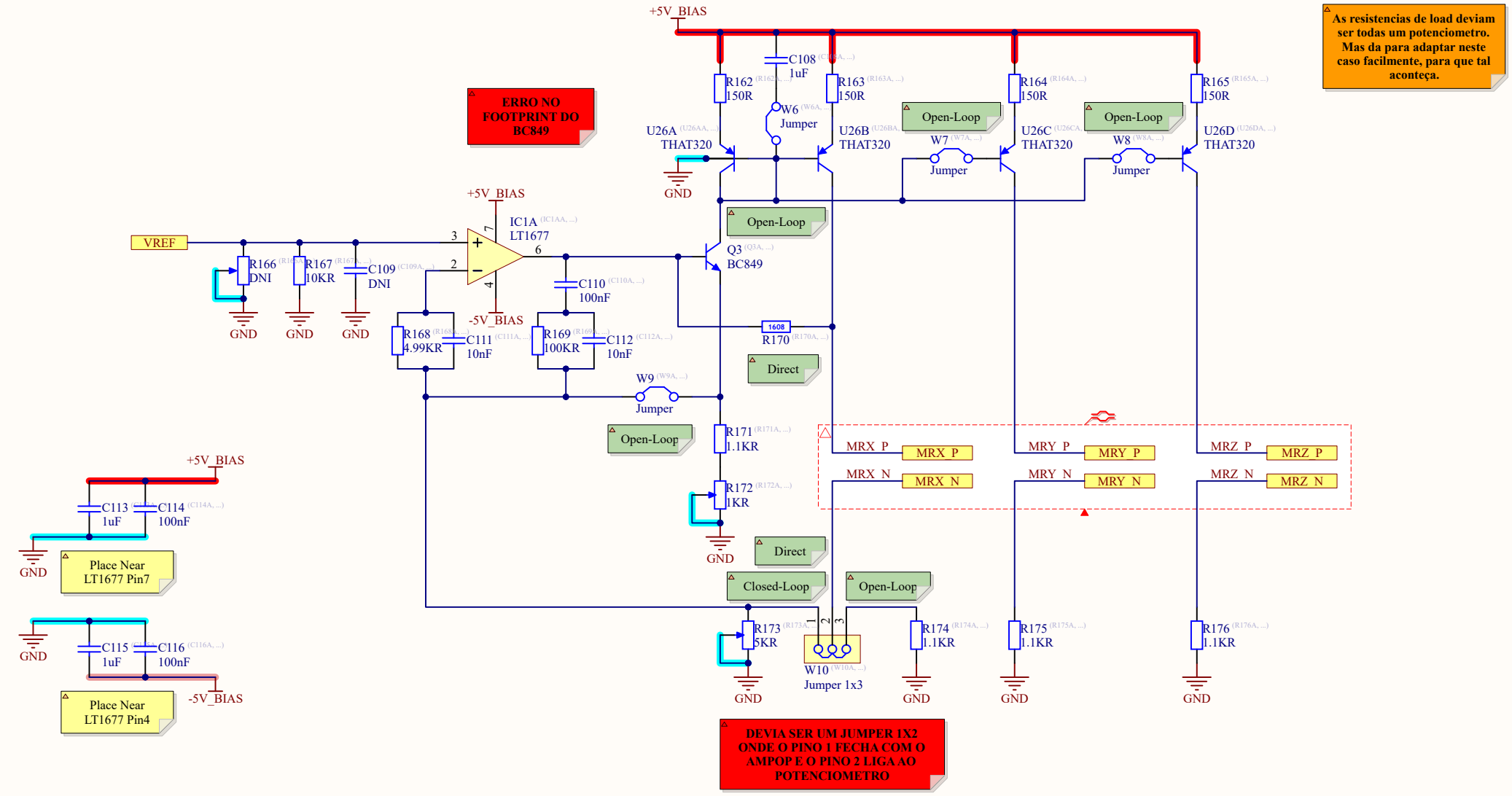


Title:	**Cytometer v3 - Channel**		Author: Artur Rafael
Size: A4	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 10 − 15	
File : Channel.SchDoc			



Title:	**Cytometer v3 - Current Source**		Author: Artur Rafael
Size: A4	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 11 − 15	
File : CurrentSource.SchDoc			

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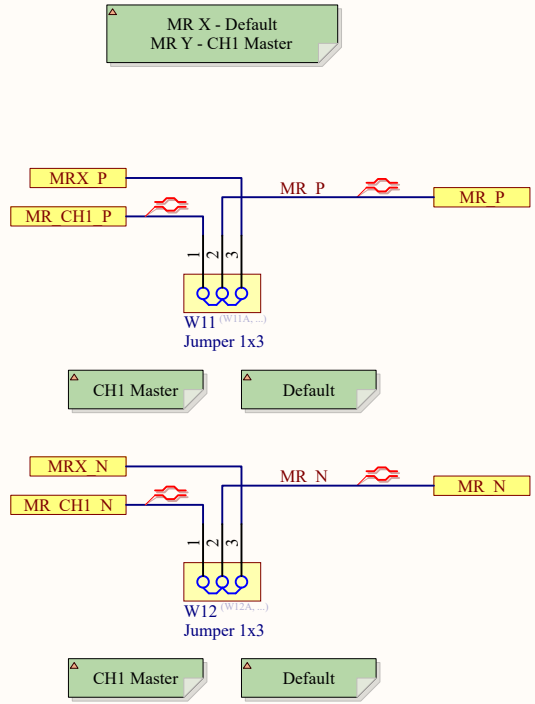
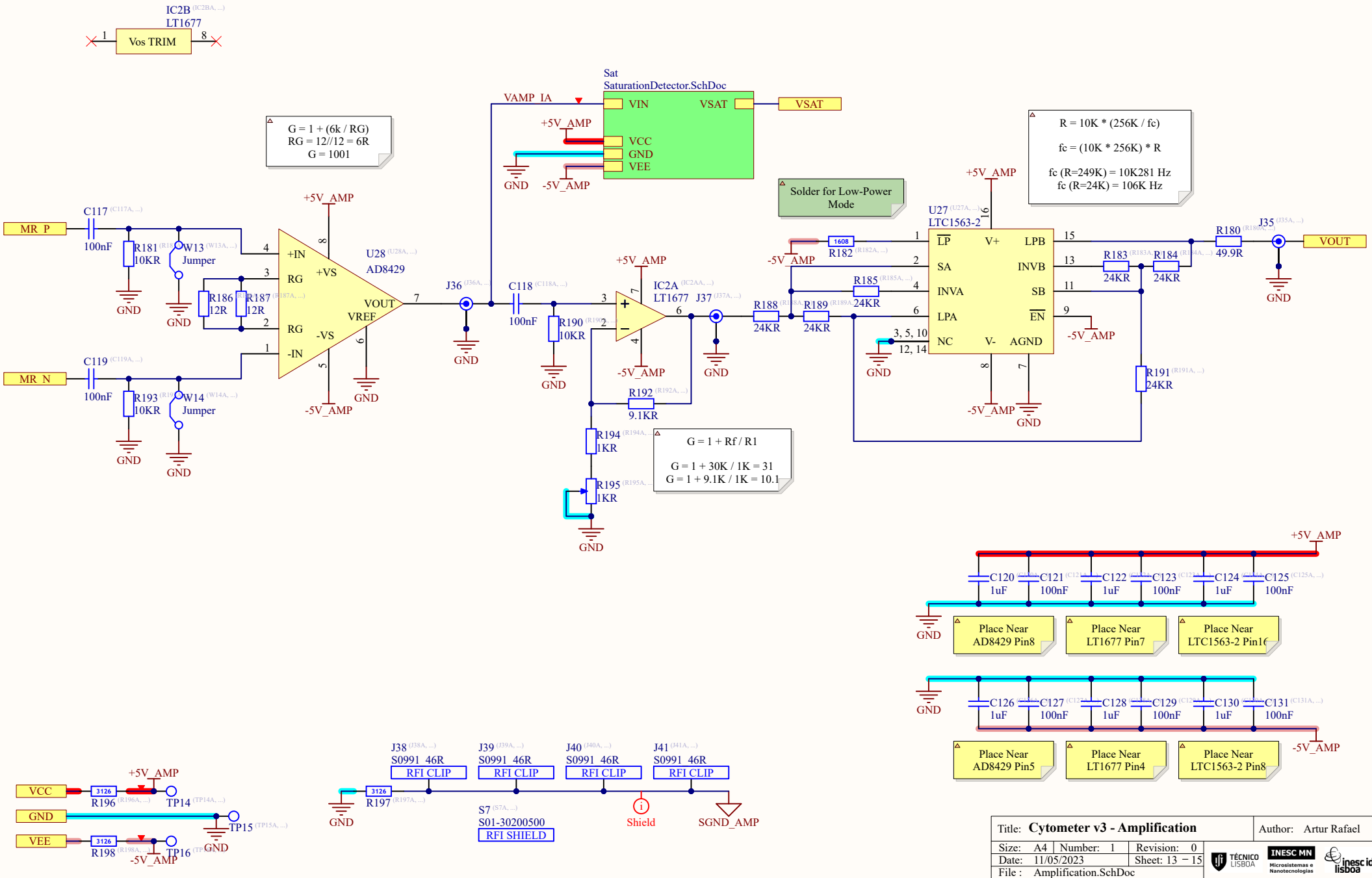
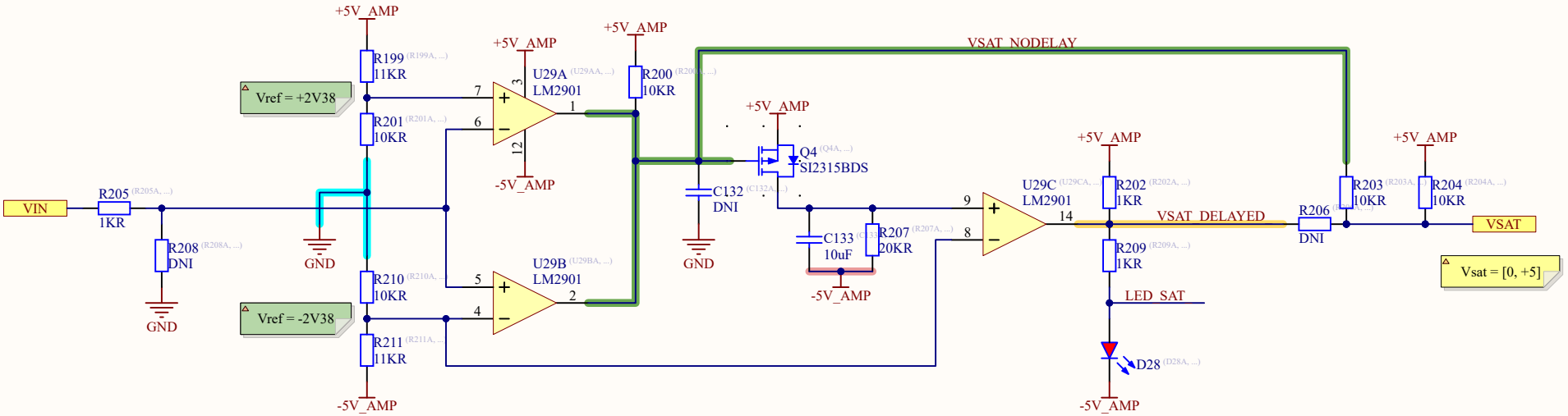
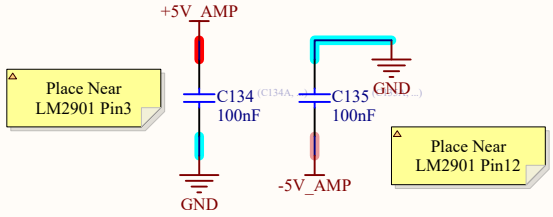


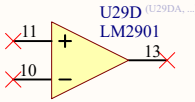
Title: **Cytometer v3 - Topology Selection**			Author: Artur Rafael
Size: A4	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 12 − 15	
File : TopologySelection.SchDoc			

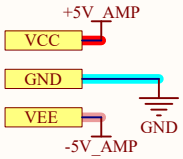


Title:	**Cytometer v3 - Amplification**		Author: Artur Rafael
Size: A4	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 13 − 15	
File : Amplification.SchDoc			









Title: **Cytometer v3 - Saturation Detector**			Author: Artur Rafael
Size: A4	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 14 − 15	
File : SaturationDetector.SchDoc			

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DNI Res 50 Ohms

VOUT_CHA1 VOUT_CHA2 VOUT_CHA3
R212 DNI R213 DNI R214 DNI
MGND

VOUT_CHB1 VOUT_CHB2 VOUT_CHB3
R215 DNI R216 DNI R217 DNI
MGND

J42
Header F 2x4
+2V5_PWR
OUTSW_A1
OUTSW_EN
OUTSW_A0
-2V5_PWR
MGND MGND

J43
Header F 2x4
VOUT_CHA3 VOUT_CHA2 VOUT_CHA1
VOUT_CHB3 VOUT_CHB2 VOUT_CHB1
MGND MGND

MUX - ADG709

- Differential 4-to-1 Mux
- +- 2.5V dual-supply rails
- Ron 3 Ohms
- Ton 14 ns

1/14ns = 71MHz/3 = 23.6MHz

ATENÇÃO É PRECISO UM DIVISOR RESISTIVOS

VOUT_CHA[1..3] VOUT_CHA[1..3]
VOUT_CHA1 R218 100R
VOUT_CHA2 R219 100R
VOUT_CHA3 R220 100R
VOUT_CHB1 R223 100R
VOUT_CHB2 R224 100R
VOUT_CHB3 R226 100R
VOUT_CHB[1..3] VOUT_CHB[1..3]

+2V5_OUTSW

U30
ADG709
S1A S2A S3A S4A S1B S2B S3B S4B
VDD DA DB VSS GND
EN A0 A1

R222 300R C136 15pF C137 10pF
R227 300R C138 15pF C139 10pF
MGND

R221 49.9R R225 49.9R
D29 770mV D30 770mV D31 770mV D32 770mV
CH_A- CH_A+ CH_B+ CH_B-

FPGA - Cyclone V
Dev Kit A/D&D/A - THDB-ADA
ADC - AD9248

AD9248:
- 14 Bit Resolution
- 65 MSPS
- 2V p-p Input Range

CH_OUT

CTRL
ENABLE OUTSW_EN
A0 OUTSW_A0
A1 OUTSW_A1

-2V5_OUTSW

J44 J45 J46
SMA F-Straight
VOUT_CHA1_1 VOUT_CHA2_1 VOUT_CHA3_1
MGND

J51 J52 J53
SMA F-Straight
VOUT_CHB1_1 VOUT_CHB2_1 VOUT_CHB3_1
MGND

J47 J48 J49 J50
S0991_46R
RFI CLIP
R228 3126
S8
S01-30200500
RFI SHIELD
Shield
SGND_OUTSW
MGND

+2V5_OUTSW
C140 1uF C141 100nF
MGND
Place Near ADG709 Pin14

C142 1uF C143 100nF
MGND
-2V5_OUTSW
Place Near ADG709 Pin3

+2V5_PWR +2V5_OUTSW
VCC R229 3126 TP17
AGND R230 3126 TP18
DGND R231 3126 MGND
VEE R232 3126 TP19
-2V5_PWR -2V5_OUTSW

Title:	**Cytometer v3 - Output Selection**		Author: Artur Rafael
Size: A3	Number: 1	Revision: 0	
Date: 11/05/2023		Sheet: 15 – 15	
File : OutputSelection.SchDoc			

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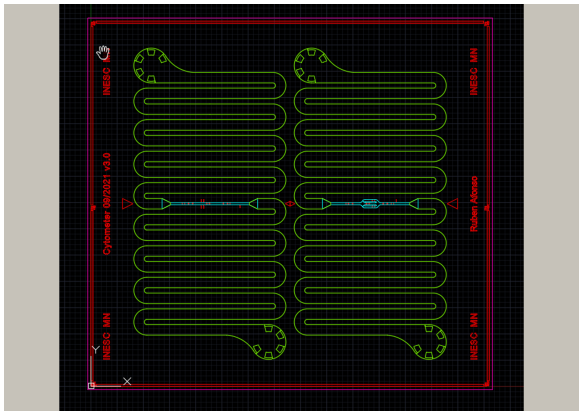
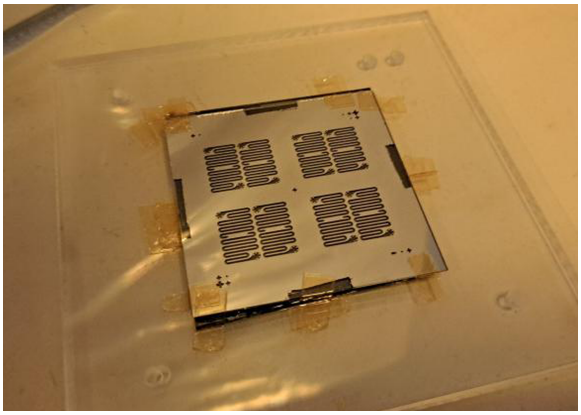
B

Microfluidics Internship

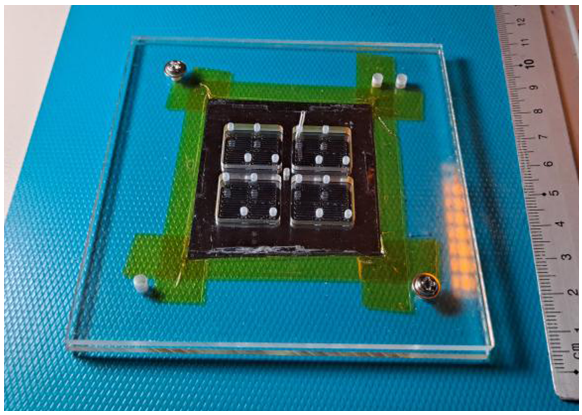
This appendix presents the microfluidics internship conducted in parallel with the development of this thesis. Both the MR sensors and microfluidic channels utilized in this application were fabricated at INESC-MN. During the internship, I had the valuable opportunity to observe and engage in a portion of the microfluidic channel fabrication process. This firsthand experience provided valuable insights and complemented the development of the interface, enhancing the overall understanding and integration of the project.



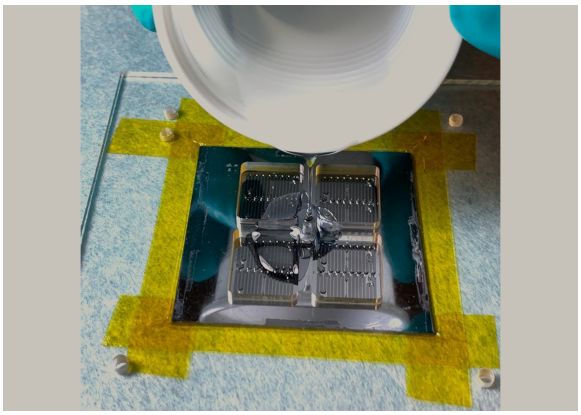
(a) Mask – developed by Eng. Ruben Afonso.



(b) Hard-mask



(c) Acrilic mold.

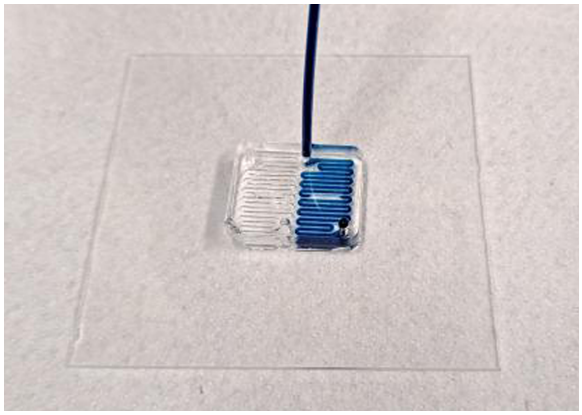


(d) PDMS pouring into the mold.

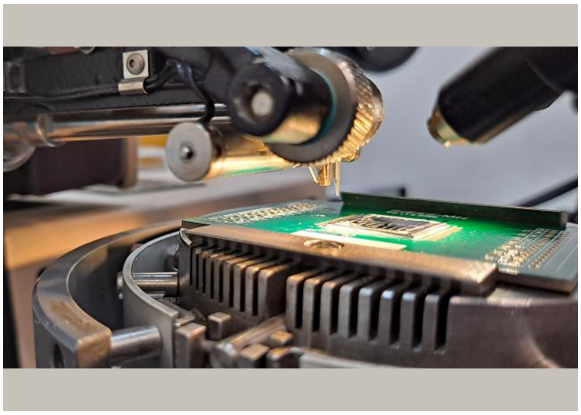
Figure B.1: Microfluidic channel fabrication process.

During my internship, I collaborated closely with Eng. Ruben Afonso and Eng. Beatriz Borges. When I joined the project, the hard-mask (Figure B.1b) responsible for defining the format of the microfluidic channel, through which the samples flow, had already been fabricated. Therefore, my involvement mainly focused on the fabrication of the Polydimethylsiloxane (PDMS) material and the channels themselves. The PDMS serves as the structural component of the channels. One specific channel (Figure B.1a) design that Eng. Ruben Afonso wanted to test was the incorporation of a serpentine shape. The objective behind this unique design was to maximize the utilization of space within the sensor chip

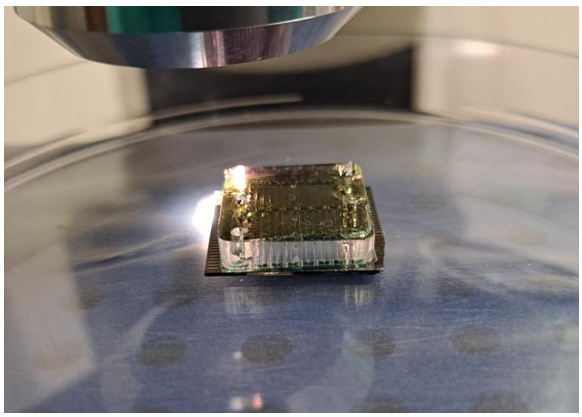
for storing the samples to be analyzed. The serpentine shape functions like a reservoir, enabling the samples to pass through the extremely narrow central channel multiple times. This repeated passage through the channel, where the sensors are located, allows for redundant measurements, ultimately enhancing the reliability and accuracy of the results. In addition to the hard-mask, an acrylic mold (Figure B.1c) was also a necessary component for the fabrication process. While the hard-mask defines the shape of the microfluidic channel, the acrylic mold is responsible for shaping the PDMS material. The acrylic mold was precisely cut at INESC-MN and required careful alignment with the hard-mask to ensure accurate replication. Once the alignment was achieved, the PDMS preparation was poured into the mold, Figure B.1d. It is essential to shape the inlets and outlets of the channels using tubes that allow the insertion of samples. Afterward, the PDMS preparation is cured, and the microfluidic channels are ready to be extracted.



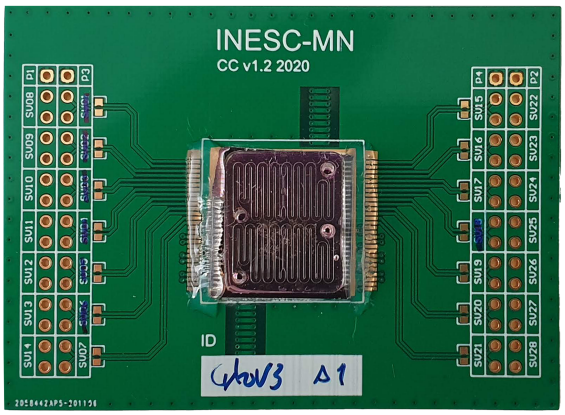
(a) Testing of the PDMS channels.



(b) Wire-Bonding – Sensor chip to PCB.



(c) Bonding – Microfluidic channel to sensor chip.



(d) Result – PCB, MR sensors and microfluidic channels.

Figure B.2: Microfluidic channel integration in the system.

After the fabrication of the PDMS microfluidic channels, the batch undergoes testing (Figure B.2a) using a sample composed of water and food coloring. This test aims to ensure that the channels are

not clogged. The channels are bonded to a glass substrate for this purpose. Once the batch passes the testing phase successfully, the microfluidic channels are ready to be bonded to a sensor chip (Figure B.2c) that has been wire-bonded (Figure B.2b) onto the PCB beforehand. The resulting assembly, depicted in Figure B.2d, is then ready to be integrated with the interface developed in this work.