11.7b Time-to-Digital Converter with 0.82ps resolution in 130nm CMOS Technology

Rodrigo Granja, Jorge Guilherme, Nuno Horta  
Instituto de Telecomunicações, Instituto Superior Técnico Lisboa, Portugal

r.granja.20@gmail.com; jorge.guilherme@ipt.pt; nuno.horta@lx.it.pt

Abstract—This paper describes a high-resolution 11.7b Time-to-Digital Converter (TDC) designed with pure digital CMOS 130nm technology. The target architecture comprises a looped delay-line based on an inverter-based pulse-shrinking technique. The proposed technique can achieve a 0.82ps resolution with a dynamic range of 2.918ns, an integral nonlinearity (INL) of -2.4 to 2.11 and a differential nonlinearity (DNL) of -0.91 to 0.87 LSB. In addition, it occupies a low area of 0.148 mm².

Index Terms—Time-to-Digital Converter, loop delay-line, inverter Pulse-Shrinking technique, high resolution and dynamic-range, low area and power consumption, simple and versatile structure.

I. INTRODUCTION

Advances in CMOS technologies are always geared by the optimization of digital circuits, therefore analog approaches are continuously losing their advantage and benefits. Technology scaling results in the decrease of the voltage power supply. Hence, voltage-mode circuits, defined by the ratio of the minimum detectable voltage (typically set by the noise floor) and the maximum available Voltage, become deeply affected, scaling poorly with technology. The shrinking of the voltage headroom will lead to a decrease in the Signal-to-Noise ratio (SNR), meaning that the devices become much more susceptible to receiving noise, which in turn leads to an inability to obtain a proper signal processing [1,2].

Digital circuits on other hand, do not present these disadvantages, having the capability of implementing their functions in a much smaller area, with lower power consumption, lower susceptibility in obtaining noise (caused by the increase in the operation speed, and even from the type of signal itself), and robustness to process variations. They cannot develop or represent any type of information in the analog domain, but they achieve very high resolution in the time domain, due to the consecutive gate delay reduction, offering exceptional time accuracy surpassing voltage resolutions in analog/mixed-signal approaches [3]. As stated in [2], in a deep-submicron CMOS process, the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of an analog signal.

A time variable possesses a unique duality characteristic. It is an analog variable, with a continuous amplitude represented by its pulse duration. However, it is also digital signal because it only has two distinct values [2]. This characteristic enables it to conduct analog signal processing in a digital environment. Considering the last statements, time-mode circuits could be the answer to performing analog signal processing in the digital domain in deep-submicron technology not only because the performance of these circuits scales well with technology, offering full programmability, low-power consumption, high-speed performance, but also the detrimental effect of technology scaling on the voltage-mode analog circuit processing disappears. [3,2,4]

Time-to-Digital Converters, TDCs, are one of the most well-known time-mode circuits. They represent nothing more than a precise stopwatch that converts continuous time domain information into a digital representation, providing a bridge between time domain and the digital world. Therefore, it should be noted that only full digital TDC’s get real advantage of time domain improvements provided by technology scaling.

With growing interest in the development of this technology, various new architectures are emerging, increasing the resolutions, dynamic ranges, and lowering the power consumption and conversion times.

This paper is organized as follows: Section II briefly addresses the conventional principles and TDCs techniques, Section III presents the converter architecture, Section IV presents, the schematic, corners and extracted simulation results and the layout of the converter, and Section V draws the conclusion.

II. RELATED WORK

Precise results require advanced electronic techniques, leading to extremely high circuit resolutions. Basic TDC topologies have their maximum resolution limited to the gate delay of the technology that is being used. Nevertheless, there are some topologies that enables sub gate delay resolutions.

The operation principle of all delay-line based TDCs, is based on the behaviour of its basic block, the inverter and its time equations [5,6].

- Rise time, \( t_r \), represents the time for a waveform to rise from 10% to 90% of its steady-state value.

\[
    t_r = 2 \frac{C_i}{\beta} V_{dd}(1 - p) \left[ \frac{p - 0.1}{1 - p} + \frac{1}{2} \ln(19 - 20p) \right] 
\]  

(1)
The working principle behind this technique is described by the following equation,

\[ t_{pd} = p + g \cdot h \]  

(8)

where \( p \) is the parasitic delay, \( g \) the logic effort and \( h \) the fan-out of the gate, \( C_{\text{load}} \) is the output load capacitance and \( C_{\text{in}} \) is the input capacitance.

Hence, looking at equation 9, manipulating the \( h \) parameter will lead, theoretically, to any possible propagation delays [1,7]. The drawbacks that this topology face are related to the huge area consumption, the big offset, the possible parasitic effects that could lead to a change in the modulated capacitators, and mainly the balancing of the start signal net that need to get to all branches at the same time, making the layout construction a very critical process [3].

Vernier based TDC is known for its high capability to measure time intervals with very high resolution, huge versatility and a simple principle of operation. Consisting of two parallel buffer delay-lines, one to receive the start command and the other to receive the stop command, both lines have the same number of delay elements, but slightly different element sizes. Same as parallel scaled delay-line, the principle behind the Vernier topology is based on the change of the propagation delay of the element gates. However, in the Vernier concept, this variation is achieved by changing the transistor sizes of the elements in the two delay-lines, keeping the load capacitance equal in every node.

The stop chain is dimensioned to be faster than the start chain, therefore in each stage the stop command will catch up with the start command, \( T_1 - T_2 \) being the difference between both delay-lines and consequently the resolution of Vernier TDC, \( T_{LSB} \). The moment that the stop signal catches up with the start signal, it translates the end of the measurement.

The main drawback of this kind of topology, is the need of an extra delay line to work, leading to an increased power and area consumption. Additionally, the control effort behind this type of topology is higher. Another aspect is that the buffers need to be perfectly balanced, so that the gate delay will not suffer any changes. However, if PVT variations are considered, this will become quite difficult.

\[ p = \frac{V_{\text{pd}}}{V_{DD}} \]  

(2)

\[ \beta_p = \mu_p C_{\text{ox}} \frac{W}{L_p} \]  

(3)

where \( C_L \) is the inverter load capacitance, \( V_{DD} \) is the voltage power supply, \( V_{\text{pd}} \) is the threshold voltage of the pMOS transistor, \( \mu_p \) is the pMOS charge-carrier effective mobility, \( C_{\text{ox}} \) is the gate oxide capacitance per unit area, \( W_p \) the p-gate width and \( L_p \) is the p-gate length.

- Fall time, \( t_f \), represents the time for a waveform to fall from 90% to 10% of its steady-state value.

\[ t_f = 2 \cdot \frac{C_L}{\beta_p V_{DD} (1-n)} [n - 0.1 - \frac{1}{1-n} + \frac{1}{2} \ln(19 - 20n)] \]  

(4)

\[ n = \frac{V_{\text{in}}}{V_{DD}} \]  

(5)

\[ \beta_n = \mu_n C_{\text{ox}} \frac{W}{L_n} \]  

(6)

where \( V_{\text{in}} \) is the threshold voltage of the nMOS transistor, \( \mu_n \) is the nMOS charge-carrier effective mobility, \( W \) the n-gate width and \( L_n \) is the n-gate length.

- Propagation Delay, \( t_{PD} \), represents the time difference between input transition (50%) and the 50% output level.

\[ t_{PD} = \frac{t_{PLH} + t_{PHL}}{2} = \frac{t_r + t_f}{2} \]  

(7)

where \( t_{PHL} \) is the time for a high-to-low transition, and \( t_{PLH} \) is the time low-to-high transition.

Taking a closer look at the equations, it can be concluded that they are mainly affected by the capacitive load, transistor size, threshold Voltage and Supply Voltage.

Parallel scaled delay-line is one of the simplest mechanisms to achieve sub-gate resolution, highly increasing the resolution of the TDC, based on scaled capacitors connected to the output of parallel delay elements, changing its output load capacitance.

The working principle behind this technique is described by the following equation,

\[ t_{PD} = p + g \cdot h \]  

(8)

\[ h = \frac{C_{\text{load}}}{C_{\text{in}}} \]  

(9)

where \( p \) is the parasitic delay, \( g \) the logic effort and \( h \) the fan-out of the gate, \( C_{\text{load}} \) is the output load capacitance and \( C_{\text{in}} \) is the input capacitance.

The last proposed techniques are highly dependent on perfectly balanced elements, to achieve a good linear response. Pulse-Shrinking on the other hand makes use of unbalanced delay elements, in a controlled way, to perform extremely high resolutions. It could be seen as an improved version of a basic delay-line based on a Vernier concept. It uses the concept of a basic delay-line, with almost the same structure taking it through sub-gate resolution, and instead of using the time difference between the propagation delay of two different elements (Vernier principle), it uses the time difference between the rising and falling times of the same delay element.
The natural process variations that are in fact unwanted effects in other topologies, here can be used as an "advantage" and finally be profitable. It is not suggested that the variation effects do not disturb the pulse-shrinking TDC. But, if they are unavoidable, perhaps the system could possibly take some advantage of it.

The pulse-shrinking TDC consists in a chain of homogenous stages, where the elements present a similar rising and falling response, and inhomogeneous stages, where intentional asymmetries make the inverter possess different rising and falling times. In Fig. 1 - Pulse-Shrinking TDC Principle Fig. 1, each inhomogeneous stage, i, stands between two homogenous stages, i-1 and i+1. This mechanism allows the accurate control of the pulse shrinking performed.

To quantify the shrinking time made in the pulse, the falling and rising expressions of the inverters are considered. According to the equations, the capacitance load is in fact the input capacitance of the next element. Then, when the input pulse travel from the i-1 to i gate, assuming that NMOS and PMOS have the same threshold voltage, which is possible assuring that \( \tau_{\text{PHL},i-1} > \tau_{\text{PHL},i} \), when the input pulse travels from i-1 to i gate, the reduction in width of the pulse is given by, \( \Delta \tau_{(i-1)\to i} = \tau_{\text{PLH},i} - \tau_{\text{PHL},i-1} = \alpha C_i \left( \frac{2}{\beta_{p,i-1} - \beta_{n,i-1}} \right) \) (10)

where,

\[
\alpha = \frac{2V_f}{(V_{pd} - V_f)} + \frac{1}{V_{pd} - V_T} \ln \left( \frac{19V_{pd} - 20V_T}{V_{pd}} \right)
\] (11)

Looking at the second stage where the pulse crosses from the element i to the element i+1 it will have a similar expression, \( \Delta \tau_{(i\to i+1)} = \tau_{\text{PHL},i} - \tau_{\text{PHL},i+1} = -\alpha C_{i+1} \left( \frac{2}{\beta_{p,i} - \beta_{n,i}} \right) \) (12)

The total pulse-shrinking time is the result of the sum of both factors previously showed, \( T_{\text{LSB}} = \Delta \tau = \Delta \tau_{(i-1)\to i} + \Delta \tau_{(i\to i+1)} = \)

\[
= \alpha \left[ C_i \left( \frac{2}{\beta_{p,i-1} - \beta_{n,i-1}} \right) - C_{i+1} \left( \frac{2}{\beta_{p,i} - \beta_{n,i}} \right) \right]
\] (13)

So, with this simple structure, high resolutions can be achieved with a basic principle and without having a very complex control logic behind it.

The area and power consumption are much smaller when compared to the previous ones, achieving equivalent resolutions. However, it suffers from long conversion times, and it has a considerable offset time. This might not make it so appealing in measuring very short times in comparison to the propagation delay of the inverter.

III. TIME-TO-DIGITAL CONVERTER ARCHITECTURE

The proposed architecture block diagram is presented in Fig. 2. The built system will only use the most indispensable and essential components to make the circuit work properly, keeping the design simple and direct. This will lead to a lower area and power consumption.

The TDC Architecture is built around a loop structure with 6 main blocks:

a. Coupling Circuit – Responsible for the acquisition of the measurement pulse from an outside source.

b. Delay-Line – It is the core block, built in a loop structure featuring the pulse-shrinking delay elements.

c. Loop Counter – Enables the count of the number of loops that the pulse gave to the chain, delivering the Course measure word.

d. Control Logic – Responsible for the control and command of the system, from the insertion of the pulse into the chain, to its reset.

e. Thermometer-to-Binary-Decoder – Responsible for the acquisition and decoding of the output from the TDC chain. It delivers the Fine measure word.

f. Registers – Responsible for saving the result of the measurement performed and delivering it to a posterior circuit. Additionally, this circuit prevents lost data, due to its regenerative topology.

A. Coupling Circuit

This circuit, looking at the system’s description, represents the “Gateway” of the system receiving the input pulse from an outside source or from the end of the chain and (re)introducing it to the TDC delay-line. Additionally, it is also responsible for
the reset of the delay-line, cleaning and preparing it to a new measurement.

![Coupling Circuit Proposed](image)

Fig. 3 - Coupling Circuit Proposed

### B. Delay-Line

The entire system performance depends mainly on the behaviour of this block, so an extra effort was made to achieve the best performance behaviour possible.

In this paper, a new Looped Pulse-shrinking TDC is proposed, as it fulfils all the requirements, namely high resolution, low area and power consumption, simple design and implementation. Additionally, it will fill an existing gap in the traditional pulse-shrinking TDC techniques.

Pulse-shrinking TDCs are based on buffers delay-lines designs [11,12], and buffers are built with two inverters in series. So, the first step is to propose a looped delay-line, where the buffer delay elements are replaced by inverters, decreasing the area and power consumption, and increasing the maximum resolution.

Rewriting equation (13) in a simpler and understandable way,

\[ \Delta \tau = (t_{PLH,i} - t_{PHL,i}) - (t_{PLH,i+1} - t_{PHL,i+1}) \]  (14)

As referred to before, this last equation is the sum of the cumulative effects from both inverters in series, and therefore the effect of one buffer.

Hence, what is proposed is to divide the equation into 2 parcels, meaning that every single inverter will shrink its traveling pulse, at least doubling at least the resolution of the delay-line and decreasing the conversion time taken to get the result.

The following equations translate the working principle behind this concept,

\[ \Delta \tau_{i} = t_{PLH,i} - t_{PHL,i} \]  (15)

\[ \Delta \tau_{i+1} = t_{PHL,i+1} - t_{PHL,i} \]  (16)

Looking at both equations, they look symmetrical. However, for symmetrical rising and falling delays or for asymmetrical but equal inverters, the pulse width will not change; the shrink will be null. Considering equation (16), matching \( i \), delay elements in Fig. 4, in order to produce a shrink at the traveling pulse, it must be ascertained that \( \tau_{PLH,i} < \tau_{PHL,i} \). In the second equation, matching \( i+1 \) delay element, results in exactly the opposite. To produce a shrinking element the aim is \( \tau_{PLH,i} > \tau_{PHL,i} \). Considering equations (15) and (16) and the required relationships between rise and fall times, for the technology used the maximum resolution achievable will be 0.82ps.

After defining the parameters of the shrink elements, it is still necessary to define the length of the delay-line which will define the maximum time measurement that it can handle. Due to the final binary code representation, the number of delay-elements must be a \( 2^n \) multiple.

Looking at the waveform at the input and output of the inverter, Fig. 5, \( out_{i} \) (blue wave), \( out_{i+1} \)(red wave), the propagation-delay of each element, will be 22.8ps.

The Pulse-shrinking Looped delay-line was built with 128 elements, leading to a maximum Dynamic range of 2.918ns.

![Proposed Pulse-Shrinking Delay-Line](image)

Fig. 4 - Proposed Pulse-Shrinking Delay-Line

![Transient Response, Propagation-delay](image)

Fig. 5 - Transient Response, Propagation-delay

### C. Loop Counter

The loop counter enables the count of the number complete cycles that the pulse has made into the delay-line. There are 3 main reasons to consider a loop technique. These are the area, power reduction, and non-linearity reduction due to PVT variations [3].

It was decided to develop an Asynchronous Counter, Ripple-Counter, mainly due to its simplicity, low area and power consumption. The bottleneck is the maximum speed at which it will operate without eventual code errors.

As it was discussed before the TDC delay line holds a maximum time of 2.918ns, \( \Delta t_{\text{max}} \). Considering that in each delay stage the resolution will be approximately 0.82ps, the maximum number of loops in the chain will be given by,

\[ N_{\text{count}} = \frac{\Delta t_{\text{max}}}{M \times T_{\text{LSB}}} = \frac{3n}{128 \times 0.82} = 27.80 \Rightarrow 28 \]  (17)

where \( \Delta t_{\text{max}} \) is the maximum hold time in the line, \( M \) is the number of elements in the chain and \( T_{\text{LSB}} \) is the TDC resolution.
Therefore, a 5-bit counter will be built for this purpose, based on True Single-Phase Latch (TSPC) flip-flops.

Due to the size of the Delay-line, each clock pulse occurs approximately every 2.918ns, in spite of not having the counter connected directly to the TDC loop, leading to maximum operation frequency of 0.3427 GHz. The time taken to trigger the last flip-flop in the counter is 285ps (leading to a maximum operating frequency of 3.5087 GHz), compared to the delay-line period, it will achieve more than the necessary to fulfill all requirements.

**D. Control Overhead**

The control system is responsible for guaranteeing the proper work flow of every part of the TDC architecture, in such a way that at the end of the measurement, the converter outputs provide a proper and “error-free” result. So, the control circuit will mainly be responsible for 2 tasks; cleaning the delay line and its sampling units, preparing it to receive a new pulse for measurement, and keeping in track the location of the travelling pulse.

The TDC delay-line is built on a looped structure concept, therefore it must be guaranteed that the correct pulse position is not lost. So, at the end of the present measurement the last recorded position could be added to the number of total loops. The control system will reset the sampling elements that the travelling pulse already left behind.

As it is an inverter delay line there are two different conditions to guarantee. Combining the previous propositions and translating both into logical equations, one for each case, the following equations are obtained,

\[ Y = A \cdot B \cdot C + D \]  
\[ \overline{Y} = \overline{A} \cdot \overline{B} \cdot \overline{C} + D \]  

Where, \( A \) and \( B \) refer to the two following stages, \( C \) and \( \overline{C} \) refer to input clock signal acquired from the delay-line and \( D \) is the Master Reset of the circuit. When the travelling pulse is translated by a high state, a falling edge at the output means that it has completely left the element, therefore equation (19) represents all these cases in the element chain. When the travelling pulse is translated into a low state, it is exactly the opposite, a rising edge at the output represents that the pulse has completely left the element, therefore equation (20) will represent all these occurrences in the delay-line. Fig. 6 shows the proposed architecture for both circuits.

**E. Thermometer-to-Binary Decoder**

Thermometer-to-Binary Decoder (TC-to-BC) will be the final stage of the proposed TDC system, responsible for the sampling of the TDC delay-line and delivery of an “error-free”, fine resolution code.

The decoding process will be performed in three steps. The first step will be sampling the outputs of the delay-line. The second step consists of selecting from the previous results the one that has gone far beyond in the chain. The third and final step will be the decoding itself based on the previous results.

1) **Sampling System**

Since it is an inverter-based chain, a negative edge triggered flip-flop is also needed to sample the elements where the pulse position is determined by a low state. The samples will be performed with a circuit based on the TSPC flip-flops. However, due to the topology used in the delay-line and the intended sampling function, the flip-flops were modified into a simpler and more direct circuit. Fig. 7 and Fig. 8 present the proposed positive edge and negative edge sampling circuits respectively.
2) One-of-N-Code

The One-of-N-Code is responsible for obtaining the final position of the pulse in the delay-chain that has been previously sampled. It selects from those the one that achieve a higher position in the sequence thermometer code. Additionally, this circuit prevents the possible occurrence of bubble errors that could cause serious errors in the output binary number.

The circuit, Fig. 9, is implemented by 2-input AND gate where one of the inputs is the inverted.

\[
\text{OUT}_i = \overline{I_n} \cdot \overline{I_{n+1}}, \quad i = 1, 2, 3, \ldots, 2^n - 2
\]

where \( \text{OUT}_i \) is the output at the position \( i \) and \( I_n, I_{n+1} \) are the inputs from the position \( I \), and \( i+1 \) respectively.

3) Fat-Tree Circuit Design

The fat-tree based decoder is one of the simplest structures to decoder the one-of-N code obtained before into a binary final word. It is based on simple CMOS NAND and NOR gates built in a tree structure, that enables it to consume less power, eliminating static power consumption, and area [13]. There are always 3 gates from any leaf node to any root node, making it a very uniform and linear circuit, leading to high speed operations. However, the layout of the fat tree is more difficult when compared with other topologies.

Therefore, and due to the fact that the looped delay-line has 128 delay elements, a 7-bit Far-tree was built to provide the fine measurement binary word.

IV. TDC PERFORMANCE RESULTS

A Full dynamic range measurement will be performed for the different corners. This will enable the calculation of the circuit INL and DNL, and the offset of the proposed circuit.

Additionally, it will be proposed a circuit Layout performed in the 130nm UMC process technology, followed by its extraction and comparison with the test-bench results.

A. Process Corner Test

1) DNL and INL Measurement

Both measures are obtained from a full dynamic range input measurement, thus from its transfer function. Fig. 10 shows the obtained transfer function for each tested corner.

Each of the tested corners presents the intended increasing linear response.

Analysing Fig. 10 each corner transfer function presents a different slope. This, is due to the effect that each corner has on the delay-line time-resolution, as the equation (14) shows.

![Fig. 9 - Partial Proposed One-of-N-Code](image)

![Fig. 10 - TDC Transfer Function](image)

a. DNL and INL Results

The following Fig. 11 represents the DNL (Differential Non-linearity) evolution through all the dynamic range for all the corners, normalized to one \( T_{\text{LSB}} \).

![Fig. 11 - DNL TDC Performance](image)

Fig. 11 may suggest that the proposed TDC presents multiple errors among the dynamic range, and sometimes, as the DNL suggests, those missing codes may rise up to 2.21 LSB.

The following Fig. 12, represents the INL (Integral Non-linearity) through all the dynamic range for all the corners, normalized to one \( T_{\text{LSB}} \).

![Fig. 12 - INL TDC Performance](image)

**Erro! A origem da referência não foi encontrada.** resumes the results of the DNL and INL for all the tested corners.

B. Layout

The circuit full Layout based on the UMC 130nm technology process is proposed. In this design, the main component will be the delay-line and its 128 inverters. The goal of the proposed Layout was to obtain a simple, compact and modular design.
The Layout Assembly is critical in a Time-to-Digital Converter Design, mainly in its delay-line where the actual measurement occurs. Any asymmetry in the layout can cause non-linearity behaviour in the TDC output response. Therefore, it is important to assure that the elements have the same structure and are equally installed to assure that their output nodes have the same parasitic resistances and capacitances associated. So, a multi-level square-based structure was proposed.

A square structure will guarantee that all the elements are placed with the exact same distance from each other, with the exact same connections and metal levels, leading to the exact same parasites in the component nodes, making it a very homogenous circuit.

The circuit is divided in six main blocks: the fine registers and fat-tree (yellow box), the one-of-n code (white box), the sampling and control logic (red box), the pulse-shrinking delay-line (green box), loop-counter and coarse registers (orange box) and decoupling capacitors (blue box).

To power the system and due to the fact that the circuit has multiple levels, a power grid technique was used, alternating VDD and GND power lines.

The global Time-to-Digital Converter Structure occupied an area of 0.148µm².

C. Extracted Results

The present chapter will evaluate the performance of the proposed TDC layout architecture. At the same time these results will be compared with the ones obtained for the TT corner (typical case).

1) DNL and INL Results

The Following Fig. 14 and Fig. 15 present the DNL and INL results, respectively, versus the Typical Corner.

From the DNL analysis, it was concluded that the extracted circuit achieved a variation between -0.91 and 0.87 LSB. The INL analysis presents a variation between -2.4 and 2.11 LSB.

D. Corners and Extracted Circuit DNL and INL analysis

The DNL and INL performance is fully dependent on the transfer function obtained from the full dynamic range test. From the analysis, especially from the DNL, it suggests that the obtained circuit has multiple errors and missing codes through all its dynamic range that could ascend up to 2.21LSB. Erro! A origem da referência não foi encontrada., in the worst case. This data may lead to the wrong conclusion that the circuit is not performing well and that is not reliable.

The main source for this problem resides in the method used to obtain the transfer function of the TDC. An array of Time pulses covering all the TDC dynamic-range was introduced in the TDC input. The array was obtained through the following equation:

$$T_m = T_{LSB} \cdot N, \quad N=1,2,3...$$  \hspace{1cm} (21)$$

However, time-resolutions errors/approximations, PVT variations, parasitic elements and mainly the offset in the circuit, may alter the length and the position of each code step in the transfer function.

The equation (21) does not take that into account, meaning that is not possible to know the position where each sample is going to be performed. Therefore, the results shown may have been a victim of the measurement itself.

Additionally, there are two effects that may contribute to this result. The first one, and common to all the TDC topologies is the cumulative effect of all non-linearities through the delay line. The second one is due to the time transitions differences between the coupling elements and the delay-line.
The following Table I summarizes the obtained results for the Proposed TDC Architecture, comparing them with other state-of-the-art TDCs.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>[14]</td>
<td>90</td>
<td>1.8</td>
<td>9</td>
<td>1.5</td>
<td>1.2</td>
<td>0.014</td>
<td>1</td>
<td>0.098</td>
</tr>
<tr>
<td>[15]</td>
<td>180</td>
<td>6.9</td>
<td>9</td>
<td>8</td>
<td>1.2</td>
<td>3.4</td>
<td>0.07</td>
<td>0.75</td>
</tr>
<tr>
<td>[16]</td>
<td>130</td>
<td>7</td>
<td>11</td>
<td>7</td>
<td>0.8</td>
<td>0.32</td>
<td>0.28</td>
<td>0.40</td>
</tr>
<tr>
<td>[17]</td>
<td>65</td>
<td>7.1</td>
<td>7</td>
<td>3</td>
<td>&lt;1</td>
<td>1.7</td>
<td>0.28</td>
<td>0.28</td>
</tr>
<tr>
<td>[18]</td>
<td>90</td>
<td>1.25</td>
<td>9</td>
<td>2</td>
<td>0.8</td>
<td>3</td>
<td>0.75</td>
<td>0.48</td>
</tr>
</tbody>
</table>

This new proposed TDC is based on a simple, direct and modular design allowing the achievement of high-resolution with a small area (0.14768μm²) and power consumption (7.5mW). The 128 shrinking-elements allow the achievement of a resolution of 0.82 ps and a dynamic range of 2.918ns. The DNL results show a variation between -0.98 and 0.97 LSB and the INL a variation of -1.52 to 1.27 LSB, suggesting that the circuit may have some non-linearity issues. However, this result has been compromised by the measurement process itself that still needs additional research and development in order to avoid possible errors in the results.

V. CONCLUSION

An inverter-based Pulse-shrinking TDC was proposed in this paper. This new proposed TDC, is based on a simple, direct and modular design allowing the achievement of high-resolution with a small area (0.14768μm²) and power consumption (7.5mW). The 128 shrinking-elements allow the achievement of a resolution of 0.82 ps and a dynamic range of 2.918ns. The DNL results show a variation between -0.98 and 0.97 LSB and the INL a variation of -1.52 to 1.27 LSB, suggesting that the circuit may have some non-linearity issues. However, this result has been compromised by the measurement process itself that still needs additional research and development in order to avoid possible errors in the results.

REFERENCES


