Quasi-square wave DC-DC converter in CMOS technology

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***Abstract*—The objective of this work is the design of a QSW-ZVS (Quasi-square Wave Zero Voltage Switching) converter in a 130nm CMOS process, to operate at very-high frequency (in the order of hundreds of MHz). The converter was designed to convert a voltage of 2.4 to 1.2V, with an output load of 50Ω, presents an efficiency of 72.84% in the schematic, with an efficiency improvement of 7% when compared with the equivalent hard switching converter) and 72.32% in the extracted layout circuit, with a Silicon footprint of 0.3401mm^2.**

I. Introduction

Monolithic integration of DC-DC switched converters in CMOS technology implies an increase of frequency, which results in increased switching losses. For the purpose of minimize these losses there are several studies about converters settings that are the result of changes applied to hard switching converters. These modifications consist in the definition of resonant switches, which includes a resonant loop in series or parallel with the switching device, to achieve ZVS or ZCS (Zero Current Switching). The QSW-ZVS converter is based on the hard switching buck PWM (Pulse Width Modulation) converter, and the difference between them is the resonant capacitor in parallel with the switching transistor [2].

The QSW-ZVS converter was intensely studied between the 80s and 90s [4, 5, 11]. In this time frame, only a contribution is focused in monolithic integration [3]. In the subsequent years several works about integrated or partial integrated DC-DC converters, at high frequency switching were reported, either about hard switching converters [6–8, 12–14], or about soft switching converters [1, 2, 10]. For this work, a comparison between [10] and [12] is mandatory, considering that the same process is used, and the power in the load and switching frequencies are similar. Comparing the efficiency of both converters, it is concluded that there is a significant disadvantage of the QSW studied in [10], when compared with the step-down in [12]. A detailed analysis of these contributions shoes that the efficiency increases with the converter power, which is due to the increasing of transferred power by the converter, do not mean a significant increase in losses. It is possible to observe this situation in [1, 7]. Studying two identical cases, [1, 10], in terms of voltage level, process and soft switching, there is a significant difference in efficiency, which happens due to a frequency difference in the load, the losses are less significant and, in the switching frequency, losses increase with increasing frequency. In respect to the objectives of the present work, some conclusions can be pointed out, when analyzing the developed converter in [2], since it is also a QSW-ZVS.

The objective of this work is the study and design of a QSW Buck converter circuit, for a 130nm CMOS process integration. The converter operates at very-high frequency, in the hundreds of MHz range, with a load power in the range of tens of mW. This project will have the support of EDA tools, dedicated to project of integrated circuits, with circuit and mask design and with functionalities validation, including corners.

The paper is divided in five sections. In section II some background knowledge about QSW-ZVS converters is provided. Section III focuses on the implementation of the converter, where each of the circuit blocks and its characterization is described. In relation to section IV, results of the simulations are exposed and the most relevant aspects of QSW converter operation, as well as interpretation of electric parameters of the circuit, are referred. Finally, in section V, conclusions about the extracted layout simulation results are presented.

II. QSW-ZVS converter

The QSW converter is characterized for having soft switching, where power source transmission to load is mainly done by a PWM process, and the resonant process only appears to obtain soft switching. Despite the fact of having resonant switching, this converter does not have oversizing disadvantages of switching devices, as in QR (Quasi Resonant) converters, making it a viable option for its monolithic integration. The QSW-ZVS converter, represented in figure 1, uses the filtering inductor as a resonant inductor, in order to obtain voltage oscillation to the transistor terminals. With this, ZVS is obtained leading to a current with high alternated component, which requires an oversizing of the filter capacitor.

This circuit has four stages of operation, shown in 2, defined by the state of MOSFET, M1 and M2, and by charge and discharge of capacitor C_O. The characteristic impedance of the circuit, Z_0, resonant frequency, ω_0, and quality factor, Q, are respectively given by:

$$Z_0 = \sqrt{\frac{L}{C_O}} \tag{1}$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C_O}} \tag{2}$$

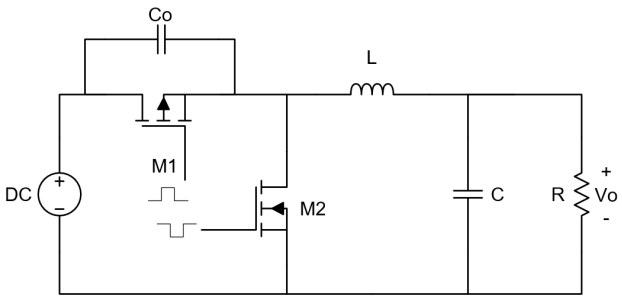
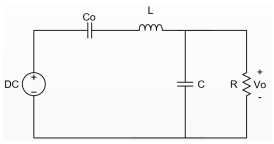


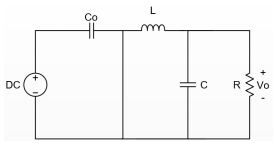
Fig. 1: QSW-ZVS converter.

$$Q = \frac{R}{Z_0} \tag{3}$$

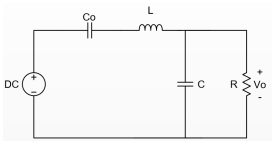
In order to have a detailed analysis of each stage, it is considered that the initial instant, t_0, corresponds to the end of stage 4, figure 2(d), and beginning of stage 1, figure 2(a). This instant is in $t = 0$, in the operation diagram represented in figure 3.



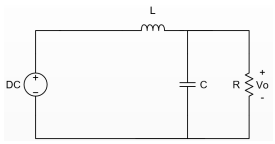
(a) Stage 1, M1 and M2 cut off.



(b) Stage 2, M1 cut off M2 conducting.



(c) Stage 3, M1 and M2 cut off.



(d) Stage 4, M1 conducting M4 cut off.

Fig. 2: Operation stages of QSW-ZVS converter.

Stage 1, $t_0 < t < t_1$: In this stage, with both transistors cut-off, the resonant load of the capacitor, C_O, and of the coil, L, begin. The capacitor voltage, v_{C_O}, and the inductor current, i_L, are given by equations 4 and 5 [2].

$$\begin{aligned} v_{C_O}(t) = &-(V_I - V_O) \cdot \cos(\omega_0 \cdot (t - t_0)) \\ &+ Z_0 \cdot i_L(t_0) \cdot \sin(\omega_0 \cdot (t - t_0)) + (V_I - V_O) \end{aligned} \tag{4}$$

$$\begin{aligned} i_L(t) = &\frac{V_I - V_O}{Z_0} \cdot \sin(\omega_0 \cdot (t - t_0)) \\ &+ i_L(t_0) \cdot \cos(\omega_0 \cdot (t - t_0)) \end{aligned} \tag{5}$$

As $C_O << C$, the duration of this stage is also much lower than in the following stages, which may lead to an approximation of the capacitor load, C_O, to a linear load. This allows an approximation of the current in the inductor to a constant current [2], $i_L(t) \approx i_L(t_0) \approx I_M$, where I_M is the peak current of the inductor (only valid for low

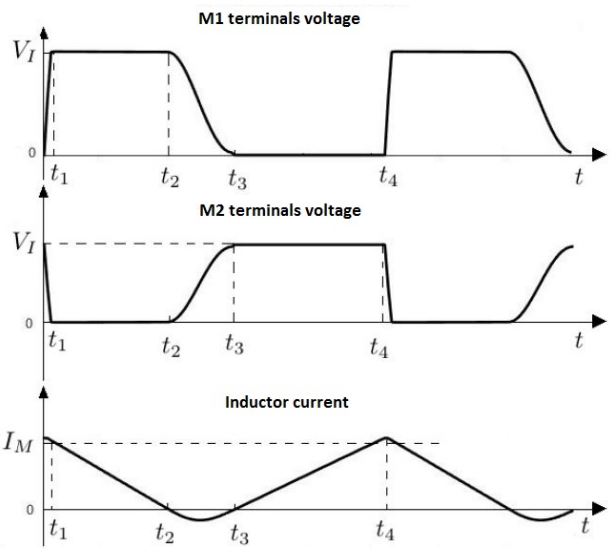


Fig. 3: Operation diagrams of QSW-ZVS buck converter.

frequencies relations, typically $f_s/f_0 < 0.5$). Knowing that $i_{C_O}(t) = i_L(t)$ with $t_0 < t < t_1$, it is obtained that:

$$v_{C_O}(t) = \frac{1}{C_O} \int_{t_0}^{t} i_L(t) \cdot dt = \frac{I_M}{C_O} \cdot (t - t_0) \tag{6}$$

Knowing that the end of this stage is when $v_{C_O}(t) = V_I$, its duration time is:

$$D_1 = \frac{V_I \cdot C_O}{I_M} \tag{7}$$

Stage 2, $t_1 < t < t_2$: The second stage begins when transistor M2 starts the conduction in t_1, starting the linear discharge of the inductor. During this stage, the capacitor voltage, C_O, remains constant, since the capacitor is in parallel with the source, $v_{C_O}(t) = V_I$. The current in the inductor, $i_L(t)$, is given by:

$$i_L(t) = -\frac{V_O}{L} \cdot (t - t_1) + i_L(t_1) \tag{8}$$

This stage ends when the current in the inductor is cancelled and the transistor M2 is cut off, so its duration, D_2, is:

$$D_2 = \frac{L \cdot I_M}{V_O} \tag{9}$$

Stage 3, $t_2 < t < t_3$: The third stage has the same configuration as the first one, where both transistors are cut off. Although, in this stage, the resonant discharge of the capacitor, C_O, with the inductor is done. The voltage in the resonant capacitor and in inductor are:

$$v_{C_O}(t) = V_O \cdot \cos(\omega_0 \cdot (t - t_2)) + (V_I - V_O) \tag{10}$$

$$i_L(t) = -\frac{V_O}{Z_0} \cdot \sin(\omega_0 \cdot (t - t_2)) \tag{11}$$

This stage ends at the full discharge of the capacitor, C_O, in other words, when the capacitor voltage is cancelled, $v_{C_O]}(t) = 0$. Analysing the equation 10, it is verified that, in order to $v_{C_O]}$ getting null , it is necessary that $V_o \geq \frac{V_I}{2}$.

Having this in mind, a limitation of the QSW converter must be considered, $\frac{V_I}{2} \leq V_O \leq V_I$. From the equation 10, it is possible to determine the duration of this stage:

$$D_3 = \frac{1}{\omega_0} \cdot \arccos\left(\frac{V_O - V_I}{V_O}\right) \tag{12}$$

Stage 4, $t_3 < t < t_4$: At t_3, the transistor M1 starts the conduction, M2 is cut off, and the linear load of the inductor begins. During this stage, the capacitor, C_O, has its terminals in short circuit and its voltage remains null, $v_{C_O}(t) = 0$. The current in the inductor, during this stage, is given by:

$$i_L(t) = \frac{V_I - V_O}{L} + i_L(t_3) \tag{13}$$

The duration of the fourth stage is the time that the inductor current takes to reach the maximum current, I_M, getting:

$$D_4 = L \cdot \frac{i_L(t_4) - i_L(t_3)}{V_I - V_O} \tag{14}$$

In [2] a method for the project of QSW-ZVS is presented, which is based on an equation that determines the relation between switching frequency, f_s, and oscillation frequency, f_0, by the gain, M. The equation 15 is obtained considering the ideal situation in which $W_O = W_I$, e $i_L(t_0) \approx I_M$.

$$\frac{f_s}{f_0} = \frac{4 \cdot \pi \cdot M^2 \cdot (1 - M)}{Q \cdot \left(\frac{M^2}{Q^2} \cdot \frac{{I_M}^2}{{I_L}^2} - (2 \cdot M - 1)\right)} \tag{15}$$

The gain of the converter, M, is a known variable, as well as the quality factor, Q, which is obtained in function of the circuit elements so, the only unknown variable is the relation between I_M and I_L. Manipulating equations 7, 9, 12 and 14, with equation 15 it is possible to achieve a third order equation, described in [2], the correspondent diagram of figure 4.

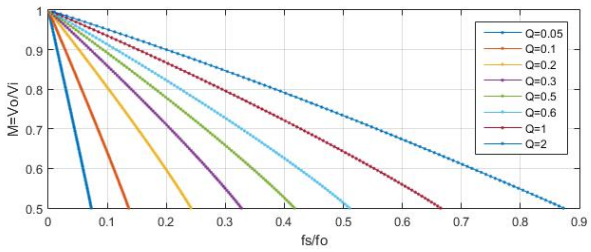


Fig. 4: Normalized switching frequency in order of M for a variety of Q values.

As it is possible to verify in figure 4, the conversion ratio, M, is affected by the variation ratio of frequency and by the load.

III. QSW CONVERTER DESIGN

A. Power circuit

The power circuit is the core of the entire converter, being responsible for switching and transferring power from the source to the load. This circuit is composed by the switching transistors, its drivers, and also by the resonant capacitor. Since the capacitor has small dimensions, of the order of pF, it is also in this block with the purpose of being integrated.

1) Switching transistors and capacitor: The switching transistors of the converter have the same operation mode as a switch, although they have considerable losses during conduction. There is a commitment between conduction losses and parasitic capacitance of each transistor gate, in other words, in order to reduce the conduction resistance of transistors, R_{ON}, its width, W, should be increased and, consequently, the capacity associated with transistor area increases. This capacity is charged or discharged each time the transistor starts conduction or is turned off, which represents losses. So, in order to minimize these losses, it is necessary to balance this parameter. In figure 5 it can be confirmed the relation between R_{ON}, the parasitic capacitance, and the transistor width.

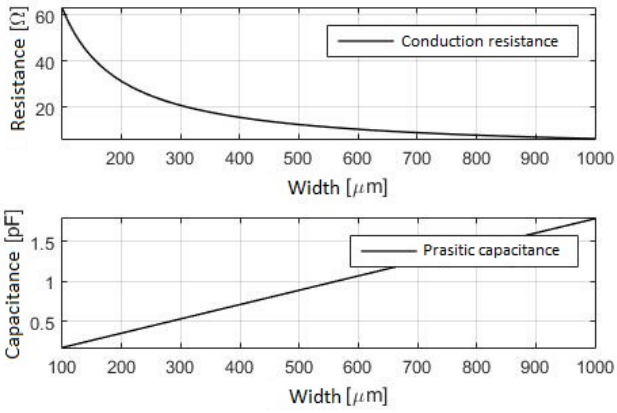


Fig. 5: Conduction resistance and parasitic capacity of transistor NMOS in order of W_N.

Despite this graphic relation between resistance and capacitance of the transistor and its width, the relation to power losses is not trivial. This happens because, associated to the area of each switching transistor, there is a driver. The dimension of each driver transistor depends on the width of the switching transistor, which is translated in more losses. As an alternative to math expressions, EDA tools can be used to compute the losses for a wide range of dimensions of NMOS and PMOS transistors, as shown in figure 6.

In order to get the diagram of figure 6 no changes were made to the drivers, being its dimensions in accordance with table I and II. This means that, for smaller dimensions, the losses could be significantly lower when compared with the diagram, if drivers were adapted. In the case of larger dimensions, if there was a corresponding adjust, the losses would be higher. So, there must be an optimal pair of dimensions W_N/W_P for which the losses are minimum, around 6,9mW. These dimensions should be adjusted in the drivers, in order to confer robustness to converter, which will lead to an higher consumption. Therefore, the transistors of the power circuit will have $W_N = 600\mu m$ and $W_P = 1,7mm$, as can be depicted in figure 7.

The converter design is made through calculations, presented in section II, however, after circuit implementation, emerged the necessity of a redesign, due to the parasitic

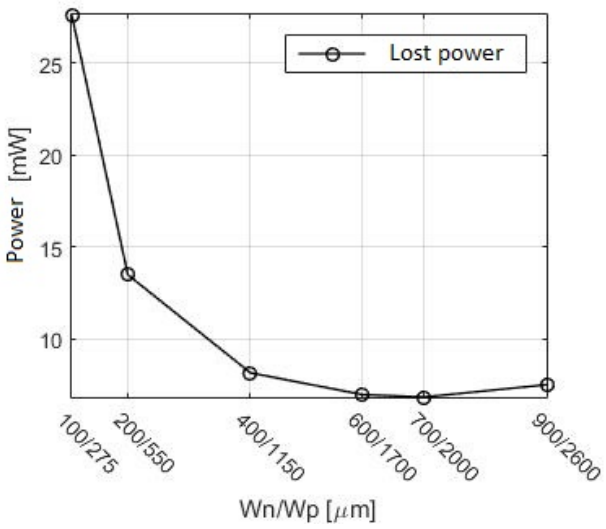


Fig. 6: Losses in the power block for a variety of dimensions of W_P/W_N.

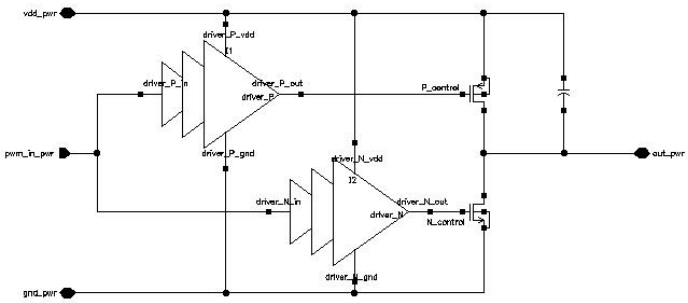


Fig. 7: Electric design of power circuit.

capacitances of the transistors. These parasitic capacities are formed between all the transistors terminals [9] and, as a consequence, they also contribute to the resonant capacitor resultant value.

2) Power Transistors Drivers : The power transistors gates drivers are constituted by four inverters, as demonstrated in figure 8 and 9, and have two fundamental roles in the converter operation. One is the adaptation of the output of fast comparator that uses transistors with dimensions in the order of hundreds of nm, for power transistors which have dimensions in the order of μm. Alongside, drivers have the function of keep fixed the duration of phases 1 and 3 of the QSW-ZVS converter operation, exposed in section II. This interval duration is obtained by the inverter design, in other words, the combination of transistors dimensions of each inverter, presented in tables I and II, and the capacitances associated to its gates, imply delays in transitions from low to high and vice versa, at each node. The dimensions shown in tables I and II only refer to the width of each transistor (W), since their length (L) remains fixed at 340 nm.

The design described in tables I and II afforded the command waves of power transistors, shown in figure 10. Both command waves at the drivers output, presented in the lower graphic of the figure, full for PMOS command and dashed for NMOS command, result from the application of the wave in the upper graphic of the figure.

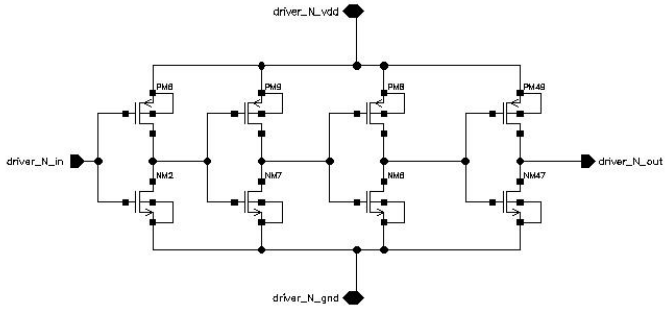


Fig. 8: Command driver of NMOS power transistor.

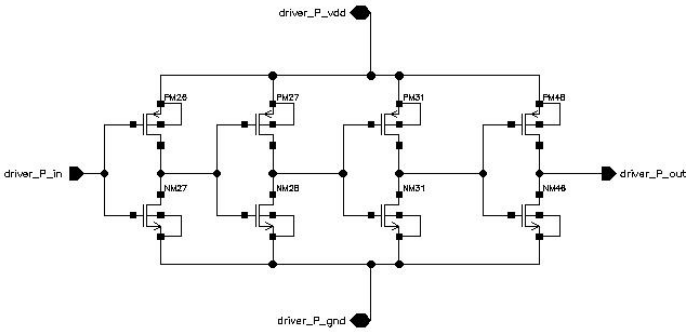


Fig. 9: Command driver of PMOS power transistor.

TABLE I: Command driver design of NMOS power transistor.

$\mathbf{W_{PMOS}}$ $[\mu m]$	0,5	2	33	66
$\mathbf{W_{NMOS}}$ $[\mu m]$	0,17	1	11	22

TABLE II: Command driver design of PMOS power transistor.

$\mathbf{W_{PMOS}}$ $[\mu m]$	0,5	15	60	200
$\mathbf{W_{NMOS}}$ $[\mu m]$	0,5	1	20	66

B. Control circuit blocks

The control of the implemented converter is based in PWM control, as can be seen in figure 11. The output voltage of the converter is also the input for the control circuit. This voltage is applied to the input of an integrator without losses, composed by an OTA amplifier. The integrator has, as a reference voltage, the desired voltage at the converter output, which is supplied by a bandgap voltage reference circuit. The control block has also a fast comparator, where its inputs are the integrator outputs, and a saw-tooth wave with a fixed frequency of 100MHz. The comparator output results in a pulse width modulated wave that will be the control the block output. The amplifier, the fast comparator and the saw-tooth

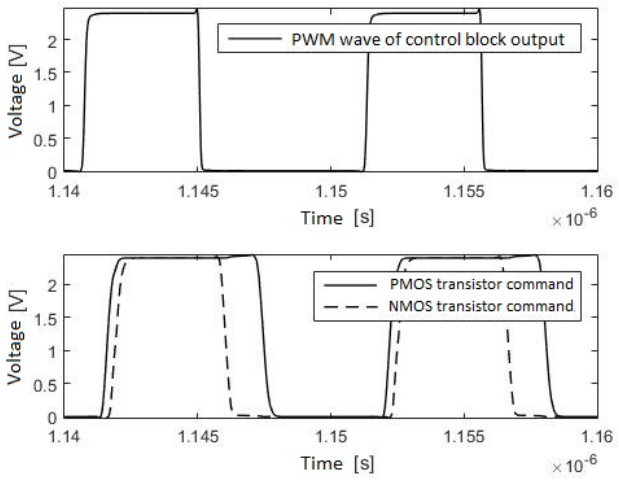


Fig. 10: Diagrams of implemented control block.

generator also need reference currents, which are generated by another block. Some of these functional blocks were used from the available library and developed at the research group were the present work was proposed.

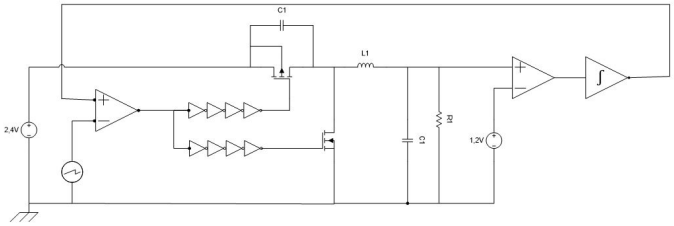


Fig. 11: Electric circuit of control block.

In figure 12 it is possible to see the diagrams associated to the control block operation. In the upper part of the figure lies the converter voltage output, that enters in the block where it is compared with the reference voltage. In the middle graphic, both the output voltage of the integrator and the saw-tooth generator voltage, are shown, which constitute the input of the fast comparator. At the bottom figure of the graphic, the resultant control wave is observed, where it is possible to see a pulse width variation that can cause a decrease in the converter output voltage. This period corresponds to the start-up phase of the circuit, before the nominal output voltage is achieved.

IV. Results

After the separate validation of the constitute blocks, a simulation on the overall system is mandatory. The performed simulations include temperature corners and MOSFET velocity corners associated with the manufacturing process, slow, typical and fast, for all types of transistors. After circuit validation with a single block in schematic, its layout is presented, from which a circuit with all the parasitic capacitance from layout, is extracted. Besides, in this section, results of simulations applied to this extracted circuit will be presented.

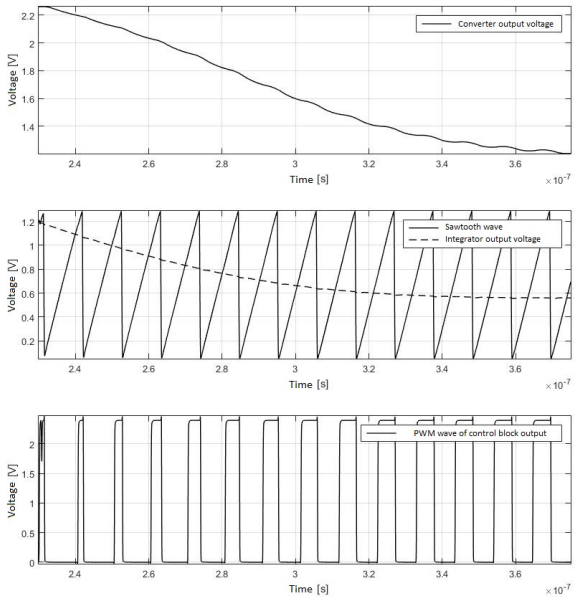


Fig. 12: Electric circuit of the control block.

A. Schematic circuit in CMOS technology

The connection between the integrated circuit with the external elements is made by wire bonding to the system PADs, which have impedance associated. For test purposes it is considered that the associated impedance to each PAD is about 1nH/mm, which may compromise the circuit operation. Accordingly, a connection to the same node in several points becomes necessary, with the purpose of reducing that impedance. In total, the access to the circuit is done by 14 PADs, 5 of which for power VDD, and 5 for power ground, as can be seen in figure 13. In figure 14 the diagrams that

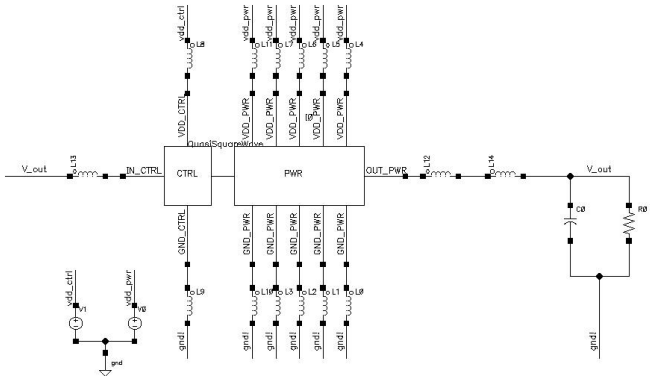


Fig. 13: QSW-ZVS for impedances test.

validate the correct operation of the converter are presented. As shown, the bond wires slightly affect the system behavior. Despite of existing some oscillations, it is not worth adding more PADs, increase significantly the converter area, as will be demonstrated in subsection IV-F. For efficiency calculation,

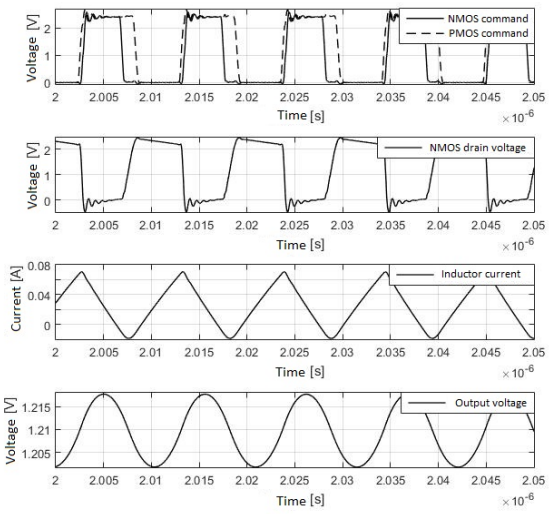


Fig. 14: Results of converter simulation with impedances of outside access.

using equation 16, circuit consumption is PIN = 40.32mW (36.98mW for power circuit and 3.343mW for control circuit).

$$\rho = \frac{P_{OUT}}{P_{IN}} \tag{16}$$

B. Corners

With the system validated for typical conditions and at room temperature, it is necessary to test it at extreme conditions, both temperature and manufacturing variations of the CMOS process. For this purpose, nine simulations that result from the combination of three temperatures (-40, 25, e 125°C) and three transistor velocities (fast, typical and slow), were calculated. In figure 15, the output voltage of the converter in its start-up phase, for each simulated corner, are presented. It is possible to conclude that there are some differences between the nine start up waves, however, all of them converge to desired output voltage. The most diverged curve is the one

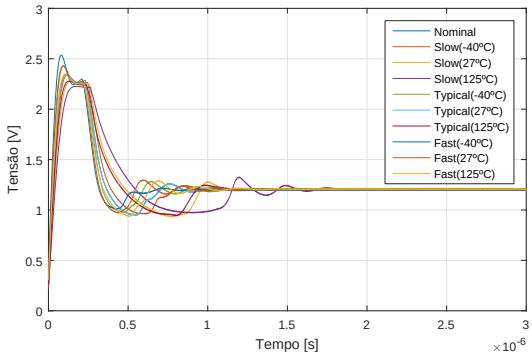


Fig. 15: Converter output voltage for nine corners.

corresponding to the slow mode, with a temperature of 125°C. This case corresponds to the slowest convergence to achieve stability at 1.2V. After stabilization, all nine corners have a maximum divergence bellow to 1%. Taking into consideration the obtained results, the circuit is valid for all corners, since none of the results question the converter operation.

C. Output load variation

As previously said, this converter was designed to operate with a fixed resistance of 50 Ohms. After some tests it was concluded that, for a resistance below 40 Ohms, the converter in no longer operating as a QSW-ZVS topology, due to limitations of the implemented circuit, although efficiency increases to 74,95%. This happens because of an increase of transferred power and, consequently, the power consumption by the converter does not change significantly, resulting in an increase of efficiency. Despite no longer working as soft switching, the converter ensures the desired output voltage to a minimum resistance of 7 Ohms. A superior limit for output load was not established, however, the obtained results for efficiency are below 45% for R values above 200Ω, which becomes not acceptable. Concerning with soft switching, it begins to be lost when 60 Ohms are exceeded.

Figure 16 demonstrates the converter ability to respond to a step change in the output load. The load varies between 25 and 75 Ohms. In simulation, the initial load is 25Ω, suffering a sudden change to 75Ω, with a rise time of 25μs. At 4μs, the load is restored to 25Ω. From graphic analysis, it is verified

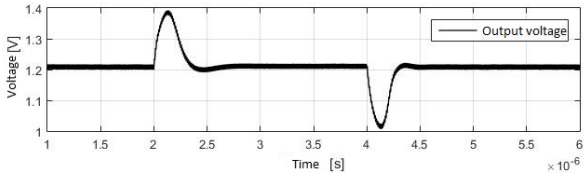


Fig. 16: Converter output voltage variation in response to an abrupt change in load.

that the converter stabilizes the output voltage in about 500ns.

D. Supply voltage variation

In accordance with output load, power supply is also a factor that can suffer some changes, contributing to the converter output voltage. In figure 17 it is possible to analyze the converter output response, when powered by a voltage step. The power supply, at 500ns, rises from 0 to 2.4V in 1ns. From the same instant, the converter output starts rising, reaching values higher than the desired ones, for about 250ns, until it is stabilized in the desired output voltage. Again, the system will need 500ns to stabilize the output voltage to its nominal value. Although the ideal situation is keep the power supply constant at 2.4V in circuit, the diagram of figure 18 shows that the converter has the ability to ensure an output of 1.2V for a range of supply voltages between 1.5 and 7V. This range does not become viable in the extremes, since the circuit operation deviates from the QSW operation, and the efficiency is lower in these situations.

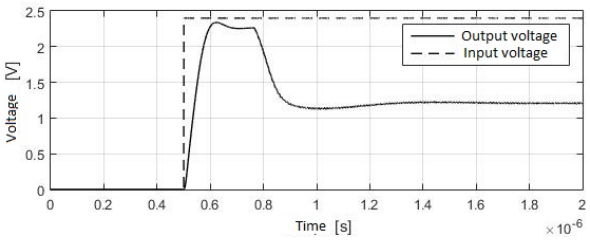


Fig. 17: Converter response to the input step.

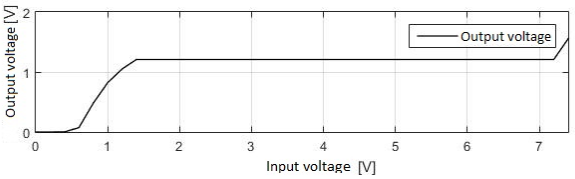


Fig. 18: Output voltage in order of input voltage.

E. Comparison with the hard switching converter

The proposed circuit is characterized by its soft switching at zero voltage operation. This type of switching is responsible for the reduction of losses associated with transistors driving in triode region. For this purpose, a comparison between the two topologies is in scope. The same switching transistors and the same control block were considered. For the hard switching topology, the resonant capacitor was removed, the filtering inductor was adjusted (equivalent of removing the QSW-ZVS resonant inductor) and the switching transistors command drivers were adapted (figure 19). In the first graphic

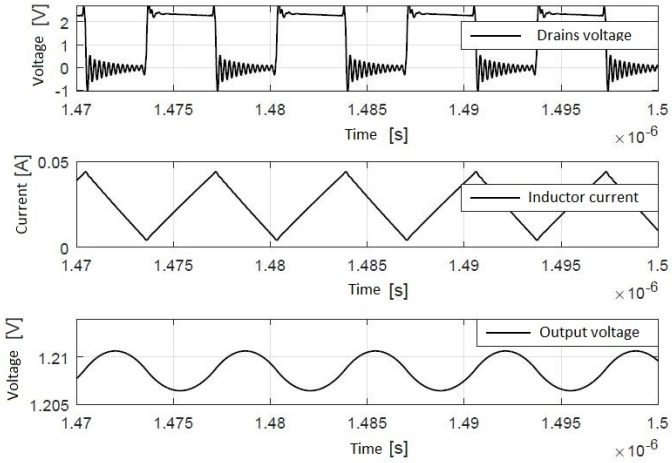


Fig. 19: Results of converter operating in hard switching.

of the figure, it is clear the difference between this diagram and the one in the second graphic of figure 14. This marks the difference between hard and soft switching, in other words, in this case the voltage in the common node of both transistors has higher slope transitions. In the QSW-ZVS converter, the transitions are set by the charge and discharge of the resonant capacitor. Also, in this converter it is notable that, during the transistors conduction, the timing diagram is not constant, due to the conduction resistance of transistors, as in QSW. These shows a voltage drop proportional to the current.

Despite of not being correctly optimized, an increased power loss in transistors is verified. The hard switching converter has a power input of 44,24mW and provides to the load a power of 29,21mW, from which an efficiency of de 66% is obtained, about 7% lower when compared to the developed converter.

F. System Layout

Layout is the final step in integrated circuit design, and it is the step where the circuit is submitted to the nal tests, before its manufacturing. In figure 20 it is represented the converter layout, with all building blocks enumerated: 1-Bandgap; 2-Operational Transconductance Amplier; 3-Fast comparator; 4-Sawtooth generator; 5-Reference current source; 6-Control block. In the periphery of the system layout there are a total

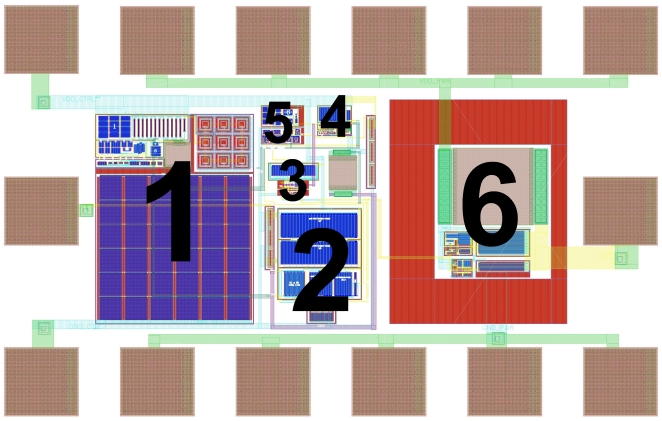


Fig. 20: Converter layout.

of fourteen PADs to external access into the circuit. In its total, the converter, has a length of 736.35μm by a width of 461.93μm, which represents an area of 0.34mm^2 (0.136mm^2 without PADs).

G. Results from the extracted circuit of QSW-ZVS converter

The extracted system has some deviations when compared to the schematic. The most evident one is the oscillating frequency of the saw-tooth generator, that decreased significantly so, it requires an adjustment in order to the system to return to the desired frequency of $100MHz$. After design adjustments, a new simulation of the extracted circuit revealed a frequency of $96.3MHz$. The correct operation is confirmed by the diagrams of figure 21, particularly, by the drain voltage of transistors with respect to the inductor current. The output voltage has an average value of $1.208V$ with $\Delta VO = 15.2mV(1.26\%)$. With $PIN = 39.63mW$ and $POUT = 29.2mW$, the circuit efficiency was higher than in schematic, $\eta = 73.68\%$. This improvement is observed in the power block, where the consumption in schematic was $7.71mW$ and, after the circuit extraction from layout, settled

in $7.08mW$. In accordance with what was done with the

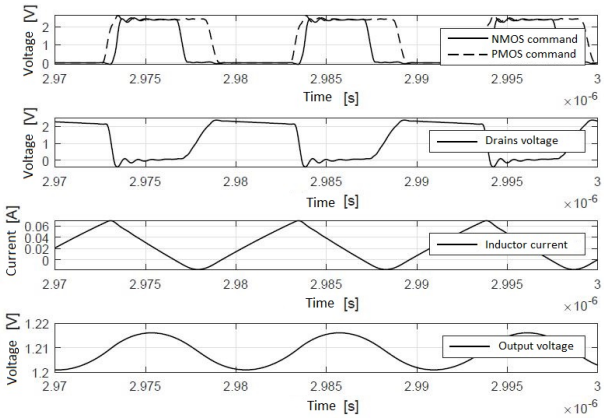


Fig. 21: Results of extracted circuit from layout with adjusted frequency.

schematic circuit, this was also simulated by corners. The results of this simulation are presented in figure 22. Despite of all waves having almost the same behavior and all of them getting in steady state faster than in schematic, it is verified that two of the waves stabilized in a value slightly higher than $1.2V$. As it is possible to see in figure 22, waves with higher

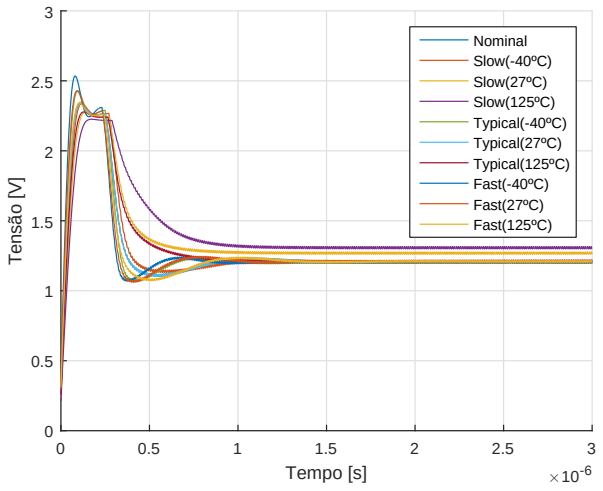


Fig. 22: Results of corners simulation of extracted circuit.

deviation are the ones referring to manufacturing process slow in room temperature, in which the converter output oscillates around $1.27V$, and in $125°C$ oscillates around $1.3V$.

V. Conclusion

One of the advantages of QSW-ZVS is the fact that it only allows transistor conduction in the triode through zero voltage switching, which significantly decrease switching losses, allowing an increase of frequency with higher efficiency. The increase in switching frequency allows the resonant capacitor integration. This converter has some limitations, being the most relevant the fact that conversion ration could not be lower than 0.5. In the designed converter, in particularly, there is another limitation to take into consideration which is the fact that an alteration in output load may compromise soft switching. However, as it is evident by the simulation results, the converter guarantees that the output remains at the desired voltage for a wide range of power supply and output load variations. Another important aspect is the comparison between the designed converter with the hard switching converter, under the same conditions. In this case, an efficiency improvement of about 7% is achieved, when compared with hard switching. The implemented QSW-ZVS, with its layout complete, allowed also that this converter stands out due to its implementation area. This converter has a lower Silicon area than the ones referred in state of art. Extracted layout simulations indicate an efficiency close to 72.32%.

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