A 0.5-2.4 DC-DC Boost Converter in CMOS Technology for Power Harvesting Applications

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***Abstract*—In this work a DC-DC boost converter, dedicated to energy harvesting applications, is developed. This converter is integrated in CMOS 130nm technology to operate at high frequency (MHz), and its goal is to convert voltages from 500mV to 2.4V. The project is assisted in Electronic Design Automation environment (EDA), resorting to the Cadence Design Environment tool (CDE) and the respective CMOS technology kit. This is validated by extreme situation simulations, known as corners' simulation. Ultimately, the projected converter is based on a hybrid architecture, inductive and capacitive, allowing to convert a voltage of 0.5V to 2.4V, with a charge of 10 KΩ and a frequency of X MHz, being the implementation area of the circuit layout 0.303mm2.**

***Index Terms*—boost, CMOS, DC-DC converter, energy harvesting, low voltage.**

I. Introduction

NOWADAYS the search for portable energy sources as been increasing. This way, there has been an increasing search for energy harvesting sources from the environment since this presents a viable alternative to provide energy to applications that are pretended to be energetically self-sufficient and which operate in low voltage. This topic was a study subject for several investigation works [1], [2], [3], [4].

Similarly, it has been sought to increase the portability and autonomy of electronic devices and develop new methods for providing energy to ICs (Integrated Circuits). However, the sources of energy harvesting only supply very low voltages, around tens or hundreds of mV. This implies the need to convert the tensions to one more elevated using, for example, a DC-DC converter, preferably, but not mandatory, with high efficiency [1], [5].

Given that the threshold voltage of the MOS transistors of conventional CMOS technology is, usually, higher than the output voltage of the energy harvesting source, it is necessary, when this occurs, to resort to a startup circuit of the DC-DC converter from the low voltage. Despite the existence of studies and projects about convertors of this kind, it appears that designing a DC-DC converter with a very low supply voltage in CMOS technology is poorly explored and a challenging investigation topic. There is yet few literature about circuits that operate with voltages around the hundreds of mV [1], [3].

This project intends to study and design a voltage lifter DC-DC converter dedicated to energy harvesting applications, to integrate in 130nm CMOS technology. The purpose is to convert the supply voltage of 500mV to 2.4V.

In the second chapter is presented the state of the art and some systems already developed for energy harvesting in CMOS technology, in the third it is shown the converter architecture, in the fourth its implementation and in the fifth the results obtained.

II. State of the art

It is possible to find in the literature several projects of interest, with different circuits and architectures. In the project presented in [6], the DC-DC converter is fed with 0.6V, however it is necessary an external voltage of 2V for the circuit to start. The circuit present in [7], whose voltage is 20mV, there is the need to add an additional external voltage of 0.65V. In [8] it is represented a voltage lifter converter, in which the supply voltage is 35mV, not being necessary an external voltage, as long as it is applied a startup circuit with a mechanical switch, which limits the field of applications. In the project presented in [9] the IC voltage lifter is used as a startup circuit, but its implementation is done in an unconventional process, of silicon-on-insulator (SOI). Yet, in the projects presented in [10]–[12], the startup circuit and the lifter converter are integrated using conventional CMOS technology. However, the startup circuit is not made using a voltage intensifier, being the minimum startup voltage higher than 0.9V, which in its turn is higher than the exit voltage of the energy harvesting sources. Thus it is verified that, to accomplish the energy harvesting applications requirements, it's necessary to integrate a low voltage startup circuit with a lifter converter using conventional CMOS technology [1].

III. Converter architecture

The converter architecture is presented in Fig. 1.

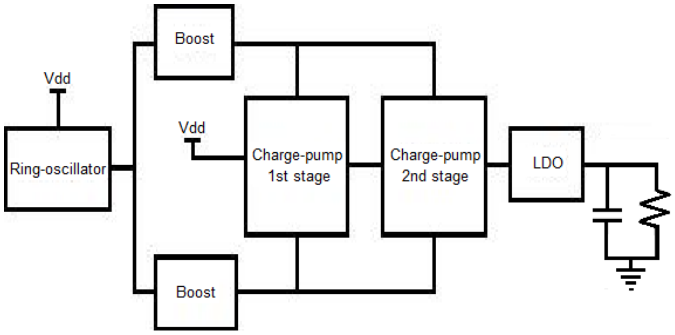

Fig. 1. Converter architecture

As it can be observed, the converter is composed by a ring-oscillator, two boosts, a two stage charge-pump and a LDO (Low Dropout Oscillator). Following is an explanation of the function and purpose of each of these elements.

A. *Boost*

The electric scheme of the boost is presented in Fig. 2 . It is composed by a switch, a inductor (L), a diode and a capacitor (C).

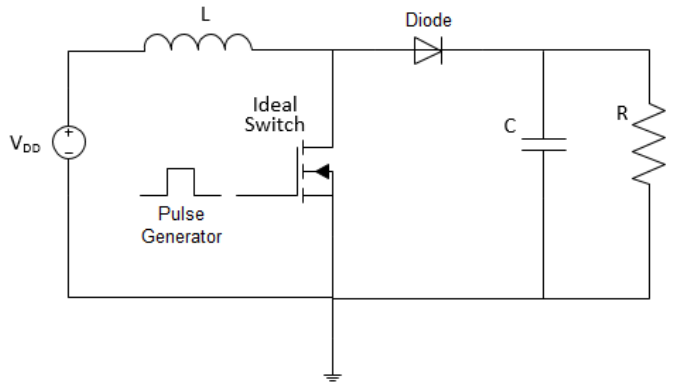

Fig. 2. Electric scheme of the boost

The switch is controlled by the clock signals created by the ring-oscillator. When the switch in conducting (ON), the inductor is connected to the ground, and the current flows from the energy source and goes through L, were the energy is stored. At this stage, the diode does not let the current pass, so the resistor and the capacitor are isolated and the resistor is fed by the charge of the capacitor.

In the moment that the switch is turned off, it is generated a voltage peak in the inductor, forcing the diode to enter in the conduction stage. This implies that the current, previously stored in the inductor, arrives to the capacitor and the resistor. Thus, the inductor is discharged and the diode goes back to not letting the current pass, repeating, cyclically, the described process.

To get the impulses that control the boost transistors, it's used the ring-oscillator. The duty-cycle, D, of the ring-oscillator, that controls the switch is important because the output voltage of the block is strictly dependent on it. This can be seen given the relationship between the output voltage, V_O, and the supply voltage, V_I, to this type of converter, which is highlighted in the next expression:

$$\frac{V_O}{V_I} = \frac{1}{1-D}\ ; \quad 0 \le D \le 1 \qquad (1)$$

Thus, it is possible to verify that the higher the duty-cycle, the higher it will be the output voltage, when the supply voltage is constant.

As it will be shown in this project, the charge-pump uses two non-overlapping clock signals to achieve the voltage increase. To get a good running of the charge-pump, these signals must not overlap, forcing the existence of two different signals. Once it is needed two signals, it can be necessary to use two boosts. In the case that the duty-cycle is 50%, it would only be needed one boost since an inverter after this element would allow to get a second lagged signal from the first. However, to any case in which the duty-cycle is different from 50%, the use of an inverter would not be enough, as the signals would not be lagged from one another, but with an opposite duty-cycle. In these situations, it's necessary two boosts, one for each impulse. This need can be easily perceived on Fig. 3. On it are shown the signals that control the boost transistors, Vx1 and Vx2, (named "control signal") and the impulses that arrive to the charge-pump Vy1 and Vy2 (named "boost signal"), for when the duty-cycle is 75%. In this Fig. 3 it is also possible to see that the duty-cycle from the boost signal is the reverse of the duty-cycle that controls it's transistors. Thus, a 75% duty-cycle at the boost matches to a duty-cycle of 25% at the charge-pump.

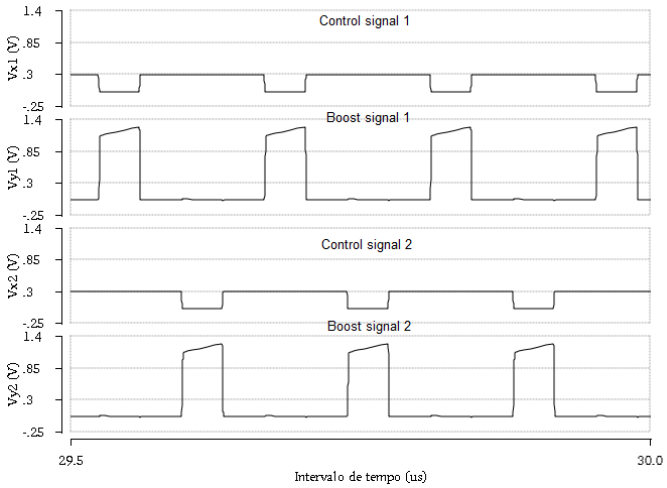

Fig. 3. Command signals and signals obtained in the boost

B. *Charge-pump*

The charge-pump used is presented in Fig. 4. To realize how this block works, in a way that assures the increase of the supply voltage, and having Fig. 4 in account, one must be aware that the M1 and M3 transistors are in conduction mode or blocking mode alternately, being that the same process happens to the M2 and M4 transistors. The M1 and M4 transistors are controlled by CLKB impulses, and the M2 and M3 transistors by CLK impulses. However, these have to be inverted to run the P type transistors.

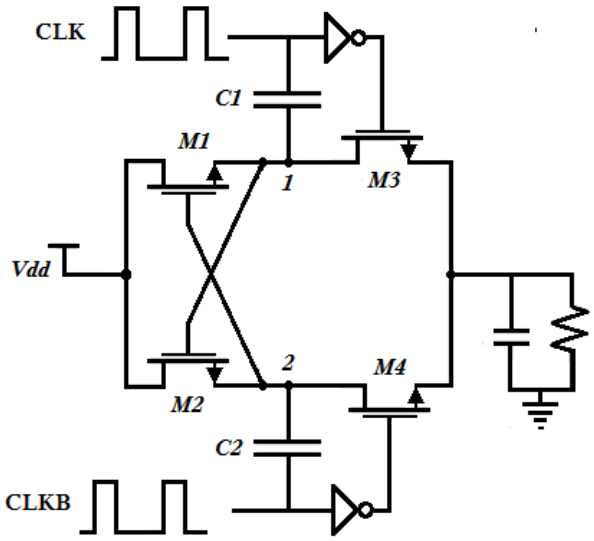

Fig. 4. Charge-pump electric scheme

Since the P type transistors start to conduct when the signal in the gate is low, and it's intended that these are conducting when the voltage in the knot 1 or 2 is high, as it can be seen below, these transistors are controlled by the signals that arrive to the capacitor after being inverted. In other words, for example, when the voltage is high in the knot 1, M3 in conducting, so it's necessary that the voltage is low at the M3 gate. The voltage that arrives to the capacitors are the clock impulses, CLK and CLKB, lagged by 180º, amplified by the boosts. Consider the voltage that arrives to the capacitor V_S and the supply voltage as V_{DD}. It can be said that the CLK impulse is low and the CLKB is high for a time period, T1

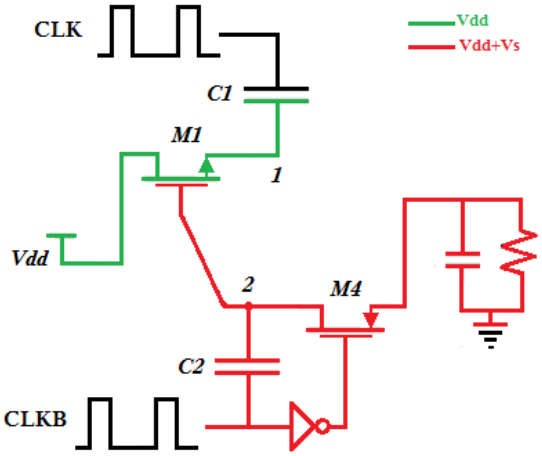

Fig. 5. Charge-pump voltage during T1

. In Fig. 5 is characterized the behavior of the circuit during this period, T1. In this period, M1 is running and the voltage in the knot 1 is $V_{DD,}$ and the voltage in the knot 2 is $V_{DD}+V_S$, M2 is off, preventing the dispersion of energy to the voltage supply, M4 is on and the output voltage is the same as in the knot 2.

In the T2 time period, the circuit is characterized by the behavior shown in Fig. 6. The clock signals get inverted, going CLK up and CLKB down, M1 is off, preventing losses from the knot 1 to the source and the M2 transistor is on, allowing the transfer of energy from the source to the knot 2. In this moment, the voltage at the knot 2 is V_{DD} and in the knot 3 is $V_{DD}+V_S$, M3 is on and the output voltage is the same as in the knot 1.

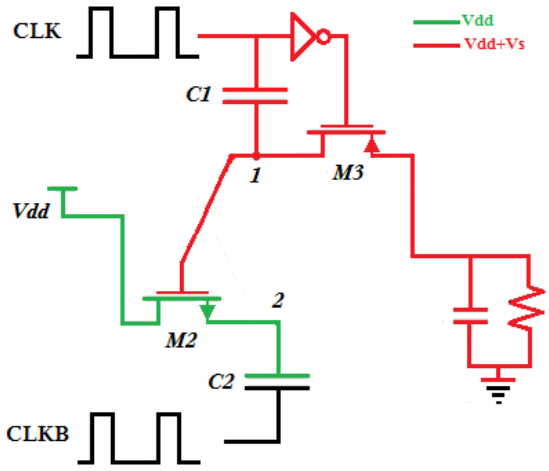

Fig. 6. Charge-pump voltage during T2

This block can increase the voltage supplied by the boost from 1.2V to 1.2+Vdd. Since it is intended that the output voltage is about 2.4V, this circuit is not enough as it would only, ideally, reach 1.5V, if the supply voltage is 0.3V, or 1.8V if the supply voltage is 0.6V. Thus, the need to use more than one stage rises. The operating mode of the second stage is just the same as the first one. This entails that it is possible to draw an output voltage of $2 \times 1.2 + Vdd$. Therefore, ideally, it is possible to get an output voltage of 2.7V when Vdd =0.3V, and a voltage of 3V when Vdd =0.6V. It's also necessary to pay attention to the fact that these figures are only real to ideal circuits, without any losses.

The schematic of the two-stage charge pump circuit is presented in Fig. 7. As it can be observed, the only elements that were not repeated were the inverters, since the impulses that control the first P type transistors are the same that control the second P type transistors.

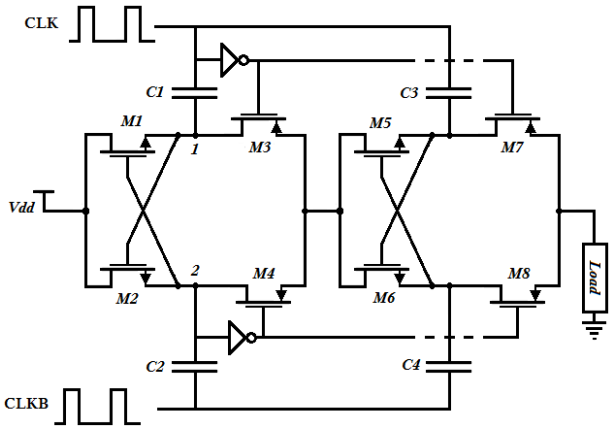

Fig. 7. Two stages charge-pump

C. LDO

The mains parts of the LDO are a P type transistor, an OTA (Operational Transconductance Amplifier), two resistors and a voltage reference. To generate this voltage reference it is used a bandgap which, together with the OTA, implies the necessity to use a current reference source.

The electric scheme is presented in Fig. 8.

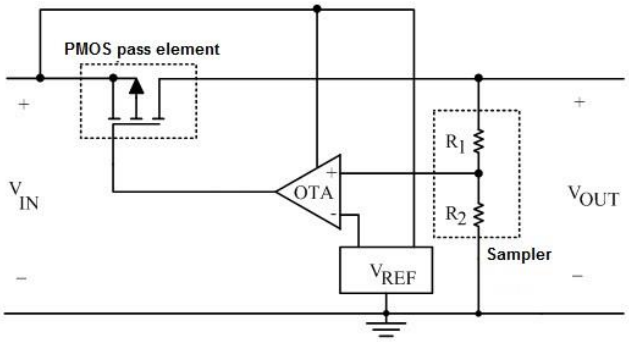

Fig. 8. Electric scheme of a classic LDO

As it was mentioned before, the LDO works as a variable resistence, so, it is needed a feedback so that it is possible to modify the resistence imposed by the LDO in order to regulate the output voltage.

Observing the image it is possible to understand that the transistor is contoled by the OTA, which works as an error amplifier. This compares the reference voltage with the voltage provinient from the node between the resistores, in which it is intended to obtain a voltage equal to the reference voltage. As this voltage varies, the OTA controls the PMOS in a way with allows him to leak more or less current being capable to maintain an output voltage almost constant.

With the use of this block, it is possible to reduce the charge-pump output voltage variations, obtaining a regulated voltage at the output of the converter.

IV. Implementation & Results

A. Power block

The power block is composed by the ring-oscillator and by the step-up, which in turn is composed by the boost and the charge-pump, as can be seen in Fig. 9.

This block as the purpose to increase the supply voltage to a higher voltage of 2.4V, so the LDO can be used and obtain a regulated output voltage of 2.4V. In this section is performed an analysis of the power block behavior.

The ring-oscillator was developed in order to obtain a duty-cycle of 58%, implying that the boost output voltage is 1,2V, when the supply voltage is 0.5V. This duty-cycle is chosen once the transistors used in the boost have a voltage limitation of 1.2V.

Since the ring-oscillator is defined it is possible to analyze the behavior of the power block as a whole. In Fig. 10 is presented the power block output voltage, including the ring-oscillator and the step-up. As can be seen the output voltage is higher than 2.4V, more precisely 2.67V, allowing the use of the LDO after the power block.

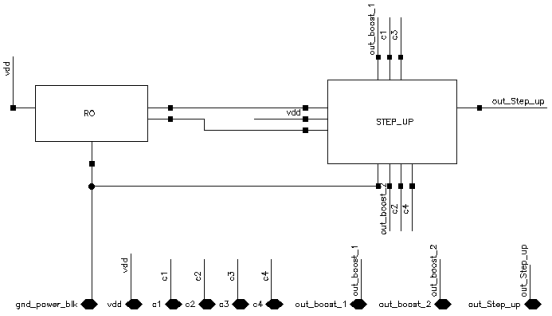

Fig. 9. Electric scheme of the power block

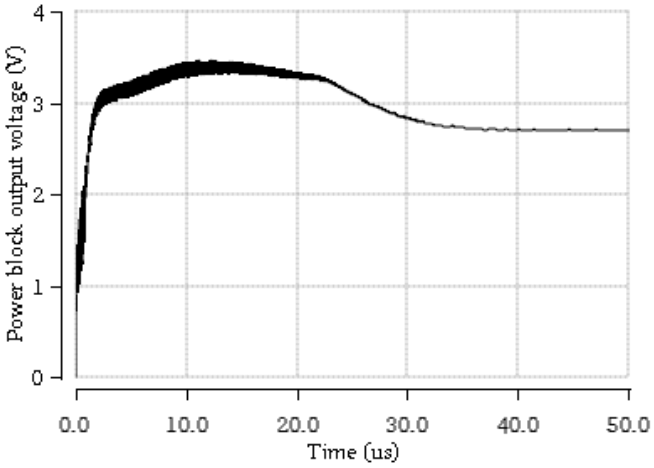

Fig. 10. Power block output voltage

B. Power block and LDO

In order to analyze the total converter, this is, the power block with all its components followed by the LDO, it is used a 0.5V voltage source to supply the system. Testing this converter it is possible to verify that an output voltage of 2.4V can be achieved, as it is intended, showing that the circuit conceived is valid. These results are presented in Fig. 11.

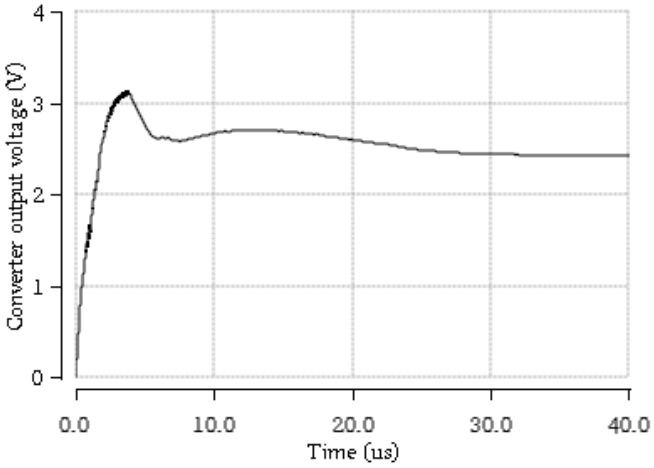

Fig. 11. Converter output voltage

C. Layout

After running the analysis on the functioning of the circuit and adjusting the components, to achieve the required voltage in the electric scheme, comes the next point in designing the circuit: making the layout. In other words, create the plant scheme of the circuit.

In fig. 12 is presented the circuit layout, where it can be seen the assembly of each block, as well as the PAD distribution. This circuit was design in a CMOS UMC 130nm MM/RF technology. Also in fig. 12, there are the main elements of the converter numbered as:

1. Ring-oscillator;
2. Boost;
3. Two stages charge-pump;
4. OTA;
5. Bandgap;
6. PMOS pass element;
7. Current reference.

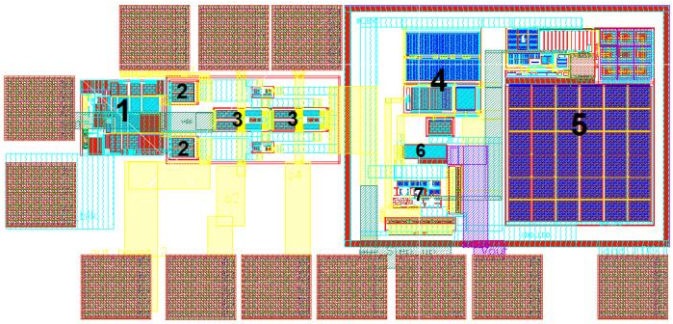

Fig. 12. Converter layout

There is the necessity to have 12 PAD to connect to the outer elements. In total, the circuit presents a length of 799,28µm and a width of 380,31µm, resulting in an area of 0,303mm^2. Without the PADs, the area of the converter is reduced to 0,204mm^2.

Once the layout is implemented, it is possible to proceed to the circuit extraction. Through this process are drawn the non-linearities of the circuit, this is, in the extracted circuit are contemplated all the resistors, capacities and inductances resulting from the connections between the different elements. After extracting the circuit is possible to test its behavior. This test is necessary since it refers to the mentioned non-linearities, while the electric scheme does not, because the connections between the elements are ideal.

D. Results from extracted circuit

In order to verify the functioning of the converter, it's necessary to test it's functioning in extreme conditions, known as corners. The behavior is analyzed for the cases with maximum temperature (125ºC), minimum (-40ºC) and normal (27ºC), by varying to each of the cases the speed of the transistors between slow, fast and typical. Thus nine simulations result, whose goal is to check the running of the circuit to the limit cases mentioned, allowing to find its limitations.

The results of the corner analyses are described in Fig. 13. After analyzing it, it is possible to verify that the intended voltage, of 2.4V, is achieved. However, for the conditions in which the transistors are in slow mode at -40ºC, the output voltage is only 1.8V, approximately. As so, this can be considered the only situation in which the output voltage is not reached. In the situation typical at -40ºC, although the output voltage corresponds to the intended, it is observed considerable fluctuations in it. Every other case assures the objective output voltage, with acceptable oscillation levels.

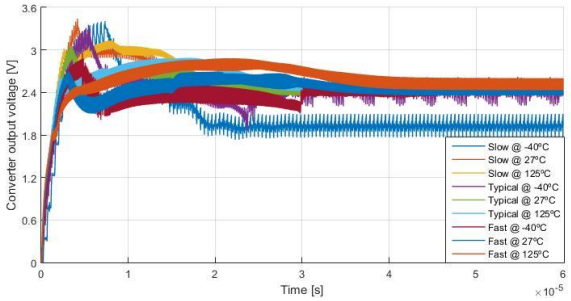

Fig. 13. Converter output voltage for nine corners.

In fig. 14 are presented the results in steady state of the corners tests in detail, were it is possible to observe the referred fluctuations.

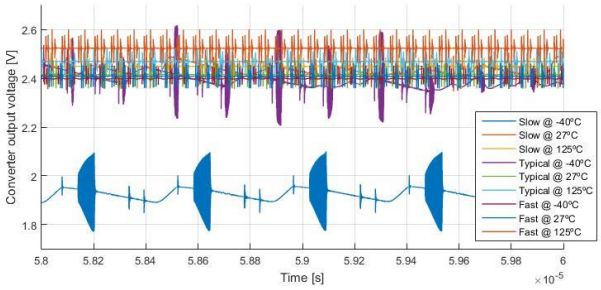

Fig. 14. Converter output voltage for nine corners in steady state.

V. Conclusion

This project studied a system that allows to avail the voltage from energy harvesting sources, increasing that voltage. This system is a voltage lifter DC-DC converter, based on an inductive-capacitive architecture, design in CMOS technology with UMC 130nm technology. The goal of this circuit is to increase the suply voltage from 0.5V to 2.4V to enable its use by other elements of integrated circuits.

Since it was attained a circuit capable of increasing a supply voltage of 0.5V to 2.4V, it can be concluded that the goals were achieved. However, it is emphasized that this circuit presents some defects relatively to the output voltage when doing the corners' testing. These defects happen specifically in cases when the transistors are at the temperature of -40ºC, in typical and slow mode.

Therefore, it can be concluded that it's possible to secure a voltage of 2.4V with a 0.5V supply voltage using a DC-DC converter in CMOS 130 nm technology.

VI. Acknowledgment

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