

Instructions

Before starting the exam, read carefully the following information:

- There are (at least) nine different versions of this exam.
- Although the exam comprises a total of 26 pages, there are two distinct volumes that should be handled as follows:
 - **Volume 1** corresponds to the question list and comprises pages 1 to 19. These pages do not need to be identified because they will be discarded at the end of the exam;
 - **Volume 2** corresponds to the answers sheet and comprises pages 21 to 26. All pages of this volume **MUST** be identified with the **student's name** and **number**.
 - At the end of the exam, all pages of **Volume 2** will be separated. Consequently, all non-identified pages will not be considered.
- The exam is composed of three parts (Part I, II and III) and has a duration of 2 (two) hours.
 - **Part I** comprises N_1 multiple choice questions and awards a total of $P_1 = 15$ points.
 - * Each correct answer awards $C = P_1/N_1$ points;
 - * Each wrong answer awards $W = -C/(A - 1)$ points (negative value), where A denotes the number of possible answers offered to each question;
 - * Each non-answered question awards 0 points.
 - **Part II** comprises an open-answer problem about combinatorial circuits and awards a total of $P_2 = 2.5$ points.
 - **Part III** comprises an open-answer problem about sequential circuits and awards a total of $P_3 = 2.5$ points.
 - All question answers **MUST** be replied in the allotted space of **Volume 2**.
- At the end of **Part I of Volume 1** you will find an empty page - you can use it for auxiliary calculations, but this page will not be delivered at the end. This means that all answers **MUST** be replied (and properly justified) in the allotted space of **Volume 2**.
- Each question includes a Portuguese translation of the corresponding text. In case of a mismatch between the English text and its translation, the English text will be the one to be considered in the evaluation¹.
- You cannot use or consult any material during the exam. On your desk you can only have a pen and your student identity card.

¹Cada pergunta inclui uma tradução para Português do referido texto. Em caso de incoerência entre o texto em Inglês e a sua tradução, será o texto em Inglês que será considerado na avaliação.

Volume 1 - Part I

Question permutation table:

	Version	1	2	3	4	5	6	7	8	9
Question										
A	→	C	N	L	E	C	M	I	R	D
B	→	I	L	D	C	D	J	E	B	C
C	→	H	B	K	N	P	D	H	F	B
D	→	M	O	A	M	Q	E	L	K	P
E	→	K	M	B	G	O	A	F	L	M
F	→	J	E	C	L	M	E	N	E	L
G	→	N	H	N	O	P	O	R	O	H
H	→	R	K	R	Q	N	G	B	P	I
I	→	G	P	J	D	F	R	G	C	K
J	→	P	Q	G	A	L	K	A	M	O
K	→	B	I	Q	P	H	C	C	D	E
L	→	O	D	M	I	B	C	D	H	G
M	→	L	J	H	K	I	L	K	J	Q
N	→	D	A	F	J	G	F	P	G	A
O	→	A	G	E	H	R	I	J	I	J
P	→	E	F	I	R	J	N	M	Q	N
Q	→	F	R	O	B	A	H	O	A	F
R	→	Q	C	P	F	K	B	Q	N	R

*: Question follows previous

A. Represent 237 in binary.

[Represente 237 em binário.]

[1]: 11101101

[2]: 10101101

[3]: 00101101

[4]: 10101100

[5]: 11100000

[6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

	Version	1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[5]	[1]	[4]	[3]	[2]	[3]	[2]	[4]	[2]
[2]	→	[4]	[5]	[3]	[4]	[1]	[4]	[4]	[2]	[3]
[3]	→	[3]	[3]	[2]	[2]	[4]	[2]	[5]	[3]	[4]
[4]	→	[2]	[4]	[5]	[1]	[3]	[5]	[3]	[5]	[1]
[5]	→	[1]	[2]	[1]	[5]	[5]	[1]	[1]	[1]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

B. Represent 321_4 in base 10.

[Represente 321_4 na base 10.]

[1]: 57

[2]: 123

[3]: 42

[4]: 74

[5]: 53

[6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

	Version	1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[5]	[2]	[3]	[2]	[4]	[5]	[2]	[4]	[1]
[2]	→	[4]	[1]	[1]	[3]	[2]	[2]	[4]	[2]	[3]
[3]	→	[2]	[4]	[4]	[1]	[1]	[3]	[5]	[1]	[2]
[4]	→	[1]	[3]	[5]	[4]	[3]	[1]	[1]	[5]	[4]
[5]	→	[3]	[5]	[2]	[5]	[5]	[4]	[3]	[3]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

C. Which of the following expressions corresponds to the minimal function (defined as a sum of products) represented in the Karnaugh-map?
 [Qual das seguintes expressões corresponde à função mínima (definida como uma soma de produtos) representada no mapa de Karnaugh?]

- [1]: $\overline{B}.\overline{D} + \overline{A}.\overline{C} + \overline{A}.\overline{D}$
- [2]: $\overline{B}.\overline{D} + \overline{A}.\overline{C} + \overline{A}.C.\overline{D}$
- [3]: $\overline{A}.C + \overline{A}.B.\overline{C} + \overline{A}.C.\overline{D}$
- [4]: $A.\overline{B} + A.\overline{B}.D + A.B$
- [5]: $\overline{B}.\overline{D} + \overline{A}.\overline{C} + \overline{A}.\overline{D} + A.B.D$
- [6]: None of the other options [Nenhuma das outras opções]

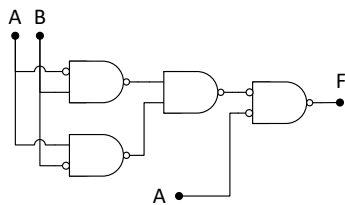
	CD			
	00	01	11	10
00	1	X	0	1
01	X	1	0	1
11	0	X	X	0
10	1	0	0	1

Correct answers: [1]

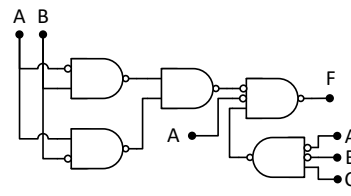
Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer		[4]	[4]	[4]	[5]	[3]	[3]	[1]	[5]	[4]
[1]	→	[4]	[5]	[3]	[1]	[2]	[5]	[2]	[1]	[2]
[2]	→	[5]	[2]	[5]	[3]	[1]	[1]	[4]	[3]	[5]
[3]	→	[2]	[3]	[1]	[2]	[5]	[4]	[5]	[4]	[3]
[4]	→	[1]	[1]	[2]	[4]	[4]	[2]	[3]	[2]	[1]
[5]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

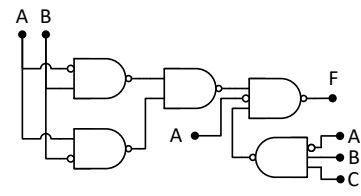
D. Which of the following circuits implements the expression $(A \oplus B) + \overline{A}.B.C + A$?
 [Qual dos seguintes circuitos implementa a expressão $(A \oplus B) + \overline{A}.B.C + A$?]



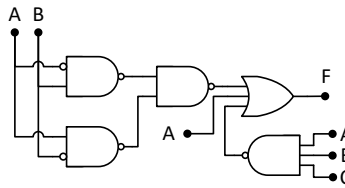
[1]



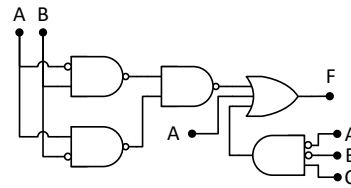
[2]



[3]



[4]



[5]

None of the other options
 [Nenhuma das outras opções]

[6]

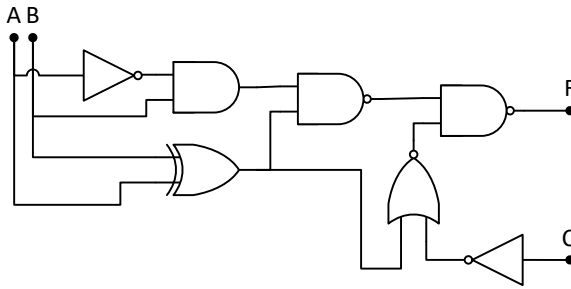
Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer		[1]	[5]	[1]	[1]	[5]	[3]	[1]	[2]	[3]
[1]	→	[4]	[2]	[3]	[2]	[1]	[5]	[3]	[1]	[4]
[2]	→	[5]	[4]	[5]	[5]	[2]	[4]	[2]	[5]	[2]
[3]	→	[2]	[3]	[2]	[3]	[3]	[2]	[5]	[4]	[1]
[4]	→	[3]	[1]	[4]	[4]	[4]	[1]	[4]	[3]	[5]
[5]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

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E. What is the worst case for the propagation time of the following circuit?
 [Qual é o pior caso para o tempo de propagação do seguinte circuito?]



Gate	tp [ns]
INV	4
NAND2	5
NOR2	7
AND2	8
XOR2	12

- [1]: 24
- [2]: 21
- [3]: 22
- [4]: 26
- [5]: 19
- [6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

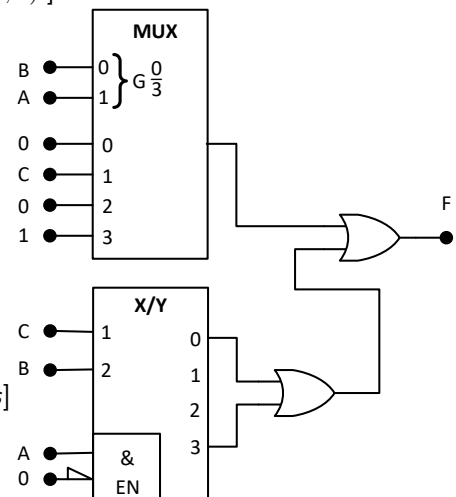
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [3]	→ [3]	→ [5]	→ [4]	→ [3]	→ [1]	→ [2]	→ [4]	→ [2]
[2]	→ [2]	→ [5]	→ [4]	→ [1]	→ [4]	→ [2]	→ [4]	→ [3]	→ [3]
[3]	→ [5]	→ [4]	→ [2]	→ [3]	→ [2]	→ [5]	→ [5]	→ [2]	→ [4]
[4]	→ [4]	→ [2]	→ [3]	→ [2]	→ [1]	→ [4]	→ [3]	→ [1]	→ [5]
[5]	→ [1]	→ [1]	→ [1]	→ [5]	→ [5]	→ [3]	→ [1]	→ [5]	→ [1]
[6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]

F. Select the option corresponding to the output $f(A, B, C)$ of the circuit shown below, when the inputs (A, B, C) have the values $(0, 0, 1), (0, 1, 0)$, and $(1, 1, 1)$.

[Indique qual das opções corresponde à saída $f(A, B, C)$ do circuito apresentado em baixo, quando as entradas (A, B, C) tomam os valores $(0, 0, 1), (0, 1, 0)$, and $(1, 1, 1)$.]

- [1]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{0 ; 0 ; 1\}$
- [2]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{0 ; 1 ; 1\}$
- [3]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{0 ; 1 ; 0\}$
- [4]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{1 ; 0 ; 0\}$
- [5]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{1 ; 1 ; 1\}$
- [6]: None of the other options [Nenhuma das outras opções]



Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

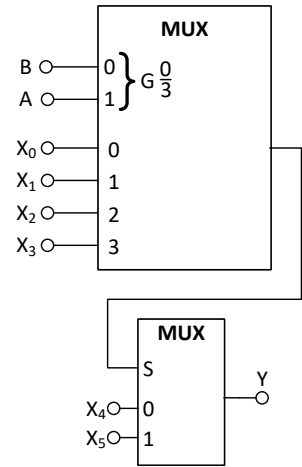
Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [4]	→ [5]	→ [2]	→ [2]	→ [3]	→ [4]	→ [4]	→ [2]	→ [5]
[2]	→ [5]	→ [4]	→ [4]	→ [1]	→ [1]	→ [2]	→ [2]	→ [3]	→ [1]
[3]	→ [3]	→ [3]	→ [1]	→ [3]	→ [5]	→ [3]	→ [1]	→ [5]	→ [3]
[4]	→ [2]	→ [1]	→ [3]	→ [4]	→ [4]	→ [5]	→ [5]	→ [4]	→ [2]
[5]	→ [1]	→ [2]	→ [5]	→ [5]	→ [2]	→ [1]	→ [3]	→ [1]	→ [4]
[6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]

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G. Consider the following circuit and truth table. Select the multiplexers inputs $\{X_5; X_4; X_3; X_2; X_1; X_0\}$ that result in the given truth table.
 [Considere o seguinte circuito e tabela de verdade. Selecione as entradas dos multiplexers $\{X_5; X_4; X_3; X_2; X_1; X_0\}$ que resultam na tabela apresentada.]

- [1]: $\{X_5; X_4; X_3; X_2; X_1; X_0\} = \{1; 0; C; C; 1; \overline{C}\}$
- [2]: $\{X_5; X_4; X_3; X_2; X_1; X_0\} = \{0; 1; C; C; 1; \overline{C}\}$
- [3]: $\{X_5; X_4; X_3; X_2; X_1; X_0\} = \{1; 0; C; 1; C; C\}$
- [4]: $\{X_5; X_4; X_3; X_2; X_1; X_0\} = \{0; 1; \overline{C}; 0; C; \overline{C}\}$
- [5]: $\{X_5; X_4; X_3; X_2; X_1; X_0\} = \{1; 0; \overline{C}; C; 0; C\}$
- [6]: None of the other options
 [Nenhuma das outras opções]

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [4]	[5]	[1]	[3]	[1]	[4]	[2]	[3]	[4]
[2]	→ [1]	[2]	[3]	[1]	[4]	[3]	[5]	[1]	[3]
[3]	→ [2]	[3]	[5]	[5]	[5]	[1]	[1]	[2]	[5]
[4]	→ [3]	[1]	[2]	[2]	[2]	[5]	[3]	[5]	[2]
[5]	→ [5]	[4]	[4]	[4]	[3]	[2]	[4]	[4]	[1]
[6]	→ [6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

H. What is the 8-bit two's complement representation of -45 ?
 [Qual é a representação em complemento para dois com 8-bits de -45 ?]

- [1]: 11010011 [2]: 11011001 [3]: 10011010
- [4]: 11011110 [5]: 00110011 [6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

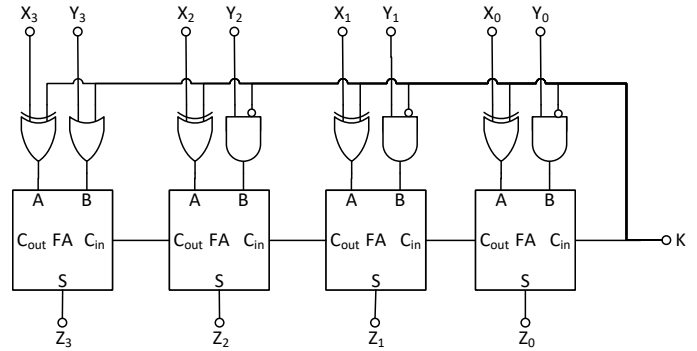
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [5]	[1]	[3]	[5]	[5]	[3]	[3]	[5]	[1]
[2]	→ [1]	[5]	[4]	[2]	[4]	[1]	[2]	[1]	[4]
[3]	→ [2]	[2]	[2]	[1]	[2]	[5]	[5]	[2]	[2]
[4]	→ [3]	[4]	[1]	[3]	[3]	[2]	[4]	[4]	[5]
[5]	→ [4]	[3]	[5]	[4]	[1]	[4]	[1]	[3]	[3]
[6]	→ [6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

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- I. Which function is implemented by the following circuit? Consider that X and Y are 4-bit signed numbers (two's complement).
 [Qual é a função desempenhada pelo seguinte circuito? Assuma que X e Y são números com sinal com 4-bits (em complemento para dois).]

- [1]: K=0: Z= X+Y ; K=1: Z= -8-X
- [2]: K=0: Z= X-Y ; K=1: Z= X+Y
- [3]: K=0: Z= X+1; K=1: Z= Y-1
- [4]: K=0: Z= X+8 ; K=1: Z= X-Y
- [5]: K=0: Z= X+Y ; K=1: Z= 1-Y
- [6]: None of the other options
 [Nenhuma das outras opções]



Correct answers: [1]

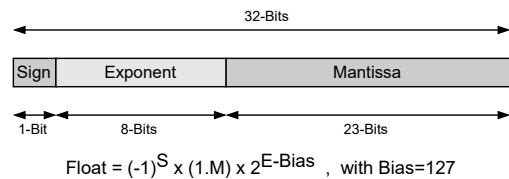
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer	[3]	[5]	[4]	[5]	[1]	[2]	[3]	[5]	[5]
[1]	→ [3]	→ [5]	→ [4]	→ [5]	→ [1]	→ [2]	→ [3]	→ [5]	→ [5]
[2]	→ [4]	→ [2]	→ [1]	→ [2]	→ [2]	→ [4]	→ [1]	→ [1]	→ [3]
[3]	→ [1]	→ [1]	→ [3]	→ [1]	→ [3]	→ [3]	→ [5]	→ [2]	→ [2]
[4]	→ [2]	→ [4]	→ [2]	→ [3]	→ [4]	→ [1]	→ [2]	→ [4]	→ [4]
[5]	→ [5]	→ [3]	→ [5]	→ [4]	→ [5]	→ [5]	→ [4]	→ [3]	→ [1]
[6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]

- J. The following 32-bit words correspond to signed rational numbers represented in fixed-point and floating-point. Which of the options presented below corresponds to an ascending ordering of these words?
 [As seguintes palavras de 32-bits correspondem a números racionais com sinal representados em vírgula fixa e em vírgula flutuante. Qual das opções corresponde à ordenação crescente destas palavras?]

A = 08005603h (Q3.29) B = 70006501h (Q1.31) C = 00870A3Dh (IEEE-754)

- [1]: A,B,C
- [2]: B,A,C
- [3]: C,A,B
- [4]: A,C,B
- [5]: B,C,A
- [6]: C,B,A



Correct answers: [3]

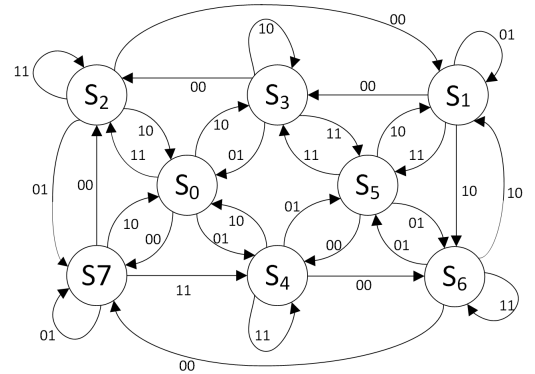
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer	[2]	[4]	[3]	[3]	[2]	[2]	[4]	[2]	[4]
[1]	→ [2]	→ [4]	→ [3]	→ [3]	→ [2]	→ [2]	→ [4]	→ [2]	→ [4]
[2]	→ [3]	→ [2]	→ [2]	→ [5]	→ [1]	→ [4]	→ [5]	→ [1]	→ [1]
[3]	→ [4]	→ [3]	→ [5]	→ [2]	→ [5]	→ [1]	→ [1]	→ [4]	→ [5]
[4]	→ [1]	→ [1]	→ [4]	→ [4]	→ [3]	→ [3]	→ [2]	→ [5]	→ [2]
[5]	→ [5]	→ [5]	→ [1]	→ [1]	→ [4]	→ [5]	→ [3]	→ [3]	→ [3]
[6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]	→ [6]

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K. Consider the following state diagram with two inputs X_1X_0 , one-hot encoding, and where each state $S_i (i = 0, \dots, 7)$ is implemented with D flip-flops, with input D_i (next state) and output Q_i (current state). Select, only for the state S_0 , the correct option for D_0 as a function of X_1 and X_0 and the current states Q_i .

[Considere o seguinte diagrama de estados com duas entradas X_1X_0 , codificação one-hot, em que cada estado $S_i (i = 0, \dots, 7)$ é implementado com flip-flops do tipo D, com entradas D_i (próximo estado) e saída Q_i (estado actual). Indique, para o estado S_0 , a expressão de D_0 como função de X_1 e X_0 e os estados actuais Q_i .]



- [1]: $D_0 = X_1X_0Q_2 + X_1\bar{X}_0Q_3 + \bar{X}_1X_0Q_4 + \bar{X}_1\bar{X}_0Q_4$
- [2]: $D_0 = X_1\bar{X}_0(Q_2 + Q_7) + X_1X_0(Q_3 + Q_4)$
- [3]: $D_0 = X_1\bar{X}_0(Q_2 + Q_7 + Q_4) + \bar{X}_1X_0Q_3$
- [4]: $D_0 = X_1X_0Q_2 + \bar{X}_1\bar{X}_0Q_3 + X_1\bar{X}_0Q_4 + X_1X_0Q_7$
- [5]: $D_0 = X_1\bar{X}_0Q_2 + X_1X_0Q_3 + X_1\bar{X}_0Q_4 + X_1\bar{X}_0Q_7$
- [6]: None of the other options
[Nenhuma das outras opções]

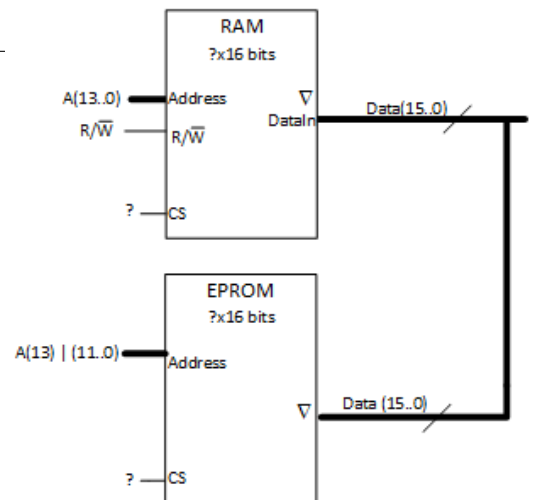
Correct answers: [3]

Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [4]	[5]	[1]	[4]	[2]	[3]	[1]	[1]	[5]
[2]	→ [5]	[4]	[4]	[5]	[1]	[4]	[5]	[5]	[1]
[3]	→ [3]	[3]	[5]	[2]	[5]	[2]	[2]	[3]	[3]
[4]	→ [2]	[2]	[2]	[3]	[4]	[1]	[3]	[2]	[2]
[5]	→ [1]	[1]	[3]	[1]	[3]	[5]	[4]	[4]	[4]
[6]	→ [6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

L. Consider the following incomplete memory system, where the CS logic is missing. The intended address ranges are the following: RAM:4000h..7FFFh, EPROM:D000h..EFFFh. Indicate the correct CS logic expressions that implement these address ranges.

[Considere o seguinte sistema de memória incompleto, onde a lógica dos sinais CS está em falta. Os intervalos de endereços que se pretendem são RAM:4000h..7FFFh, EPROM:D000h..EFFFh. Indique as expressões corretas para os sinais CS que implementam estes intervalos de endereçamento.]



- [1]: RAM: $\bar{A}(15) \cdot A(14)$; EPROM: $A(15) \cdot A(14) \cdot (\bar{A}(13) \oplus A(12))$
- [2]: RAM: $A(15) \cdot \bar{A}(14)$; EPROM: $A(15) \cdot A(14) \cdot \bar{A}(13)$
- [3]: RAM: $\bar{A}(15) \cdot \bar{A}(14)$; EPROM: $A(15) \cdot A(14) \cdot (A(13) \odot A(12))$
- [4]: RAM: $\bar{A}(15) \cdot A(14)$; EPROM: $A(15) \cdot (\bar{A}(14) \oplus A(13))$
- [5]: RAM: $\bar{A}(15) \cdot A(14)$; EPROM: $A(15) \cdot A(14) \cdot (A(13) \oplus A(12))$
- [6]: None of the other options
[Nenhuma das outras opções]

Correct answers: [5]

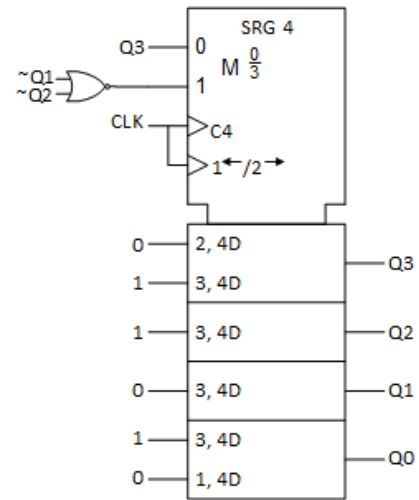
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Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [4]	[5]	[3]	[2]	[4]	[3]	[4]	[3]	[3]
[2]	→ [2]	[2]	[2]	[3]	[1]	[5]	[1]	[2]	[2]
[3]	→ [3]	[3]	[1]	[1]	[2]	[1]	[2]	[5]	[1]
[4]	→ [1]	[4]	[5]	[4]	[5]	[4]	[3]	[4]	[5]
[5]	→ [5]	[1]	[4]	[5]	[3]	[2]	[5]	[1]	[4]
[6]	→ [6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

M. Consider the following circuit with a 4-bit shift register, as depicted in the figure. The current state is $Q_3 Q_2 Q_1 Q_0 = 1011$. What are the next two states of the circuit?

[Considere o seguinte circuito com um registo de deslocamento de 4-bits representado na figura. O estado actual é $Q_3 Q_2 Q_1 Q_0 = 1011$. Quais serão os próximos dois estados?]



- [1]: 0110, 0011
- [2]: 0111, 1110
- [3]: 1101, 0110
- [4]: 1010, 0110
- [5]: 1001, 1001
- [6]: None of the other options
[Nenhuma das outras opções]

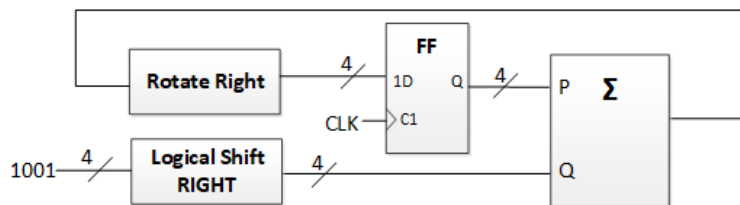
Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [4]	[1]	[1]	[1]	[5]	[3]	[4]	[1]	[1]
[2]	→ [5]	[2]	[3]	[3]	[4]	[4]	[3]	[5]	[3]
[3]	→ [2]	[3]	[2]	[5]	[3]	[2]	[1]	[2]	[2]
[4]	→ [1]	[4]	[4]	[2]	[1]	[1]	[2]	[3]	[4]
[5]	→ [3]	[5]	[5]	[4]	[2]	[5]	[5]	[4]	[5]
[6]	→ [6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

N. Consider the following circuit with an adder, a register (4 FF's) and a combinational logic circuit. Assuming that the current state is $Q(3:0) = 0011$, what are the next two states of the circuit?

[Considere o seguinte circuito com um somador, um registo (4 FF's) e lógica combinatória. Assumindo que o estado actual é $Q(3:0) = 0011$, quais serão os próximos dois estados do circuito?]



- [1]: 0101, 1101
- [2]: 1001, 1101
- [3]: 0011, 1010
- [4]: 0100, 1111
- [5]: 1011, 1111
- [6]: None of the other options
[Nenhuma das outras opções]

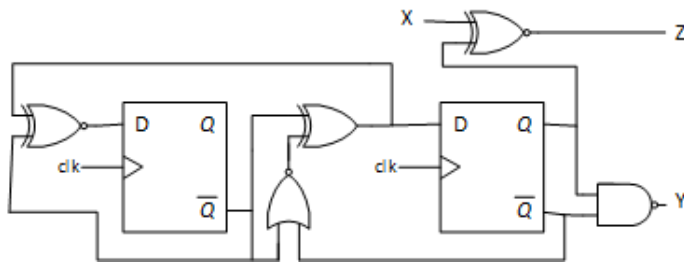
Correct answers: [5]

Answer permutations: (All answers permuted, except last answer)

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Version	1	2	3	4	5	6	7	8	9	
Answer										
[1]	→	[5]	[4]	[3]	[2]	[2]	[5]	[3]	[2]	[3]
[2]	→	[2]	[3]	[5]	[4]	[4]	[3]	[2]	[4]	[4]
[3]	→	[1]	[5]	[2]	[1]	[5]	[4]	[5]	[1]	[2]
[4]	→	[4]	[2]	[4]	[3]	[1]	[1]	[4]	[5]	[1]
[5]	→	[3]	[1]	[1]	[5]	[3]	[2]	[1]	[3]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

O. What is the minimum clock period of the following circuit, given the table values (in ns)?
 [Qual é o período de relógio mínimo do seguinte circuito, assumindo os valores da tabela (em ns)?]



	tp [ns]	tsu [ns]	th [ns]
FF D	12	5	7
NOR	4		
XNOR	11		
XOR	8		
NAND	5		

- [1]: 36
- [2]: 35
- [3]: 40
- [4]: 28
- [5]: 34
- [6]: None of the other options [Nenhuma das outras opções]

Correct answers: [3]

Answer permutations: (All answers permuted, except last answer)

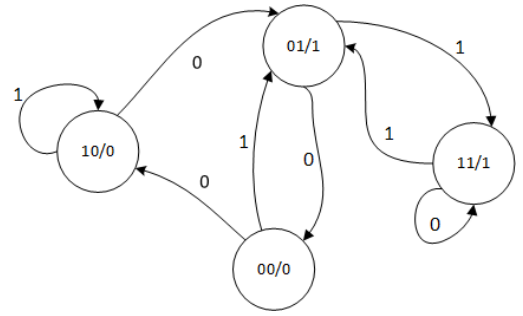
Version	1	2	3	4	5	6	7	8	9	
Answer										
[1]	→	[4]	[4]	[3]	[4]	[3]	[3]	[5]	[3]	[4]
[2]	→	[5]	[1]	[2]	[3]	[1]	[5]	[2]	[1]	[2]
[3]	→	[1]	[2]	[5]	[5]	[5]	[1]	[1]	[2]	[5]
[4]	→	[3]	[3]	[4]	[2]	[2]	[4]	[3]	[4]	[1]
[5]	→	[2]	[5]	[1]	[1]	[4]	[2]	[4]	[5]	[3]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

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P.

Consider the following state diagram. Select the output value for each state and the value of the next state for each state and input.

[Considere o seguinte diagrama de estados. Indique o valor da saída do circuito para cada estado e o valor do próximo estado para cada valor do estado e entrada.]



Q(n)	Y(n)	Q(n+1) x=0	Q(n+1) x=1
00	0	10	01
01	1	00	11
10	0	01	10
11	1	11	01

[1]

Q(n)	Y(n)	Q(n+1) x=0	Q(n+1) x=1
00	0	10	11
01	1	00	10
10	1	10	10
11	0	11	01

[2]

Q(n)	Y(n)	Q(n+1) x=0	Q(n+1) x=1
00	0	11	00
01	1	10	11
10	1	10	01
11	0	11	01

[3]

Q(n)	Y(n)	Q(n+1) x=0	Q(n+1) x=1
00	0	11	00
01	1	01	00
10	0	01	10
11	1	01	01

[4]

Q(n)	Y(n)	Q(n+1) x=0	Q(n+1) x=1
00	1	10	01
01	0	11	10
10	1	00	00
11	0	01	01

[5]

None of the other options
[Nenhuma das outras opções]

[6]

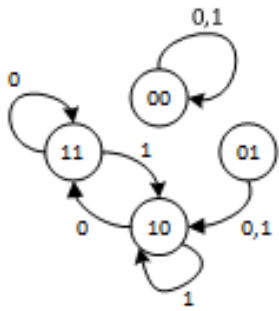
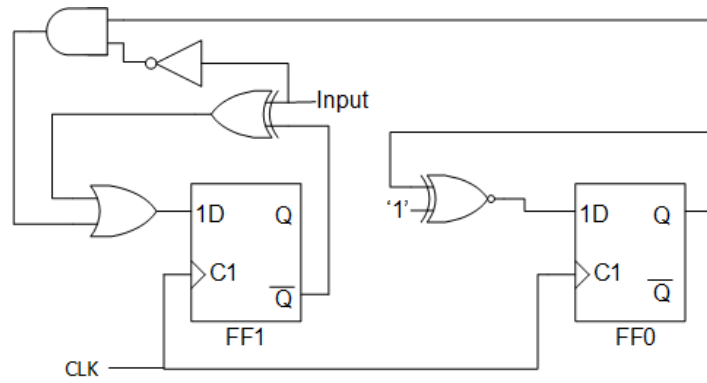
Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

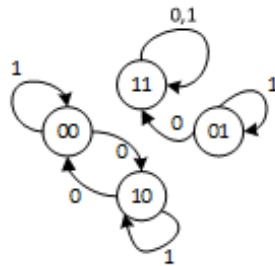
Version	1	2	3	4	5	6	7	8	9	
Answer	[1]	[2]	[1]	[5]	[2]	[5]	[2]	[3]	[2]	[4]
	[2]	[1]	[3]	[3]	[3]	[2]	[1]	[2]	[4]	[1]
	[3]	[4]	[5]	[1]	[1]	[1]	[4]	[1]	[1]	[5]
	[4]	[5]	[4]	[2]	[4]	[4]	[5]	[4]	[5]	[2]
	[5]	[3]	[2]	[4]	[5]	[3]	[3]	[5]	[3]	[3]
	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

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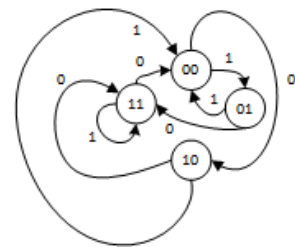
Q. Consider the following circuit.
 Which state diagram corresponds to the circuit?
 [Considere o seguinte circuito.
 Qual dos diagramas de estado
 corresponde ao funcionamento
 do circuito?]



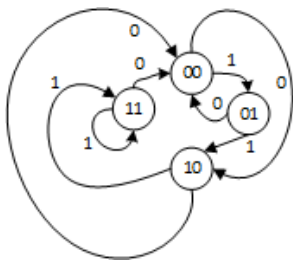
[1]



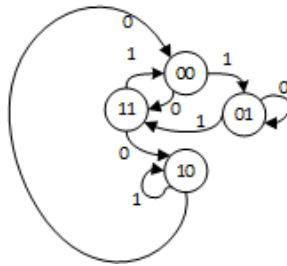
[2]



[3]



[4]



[5]

None of the other options
 [Nenhuma das outras opções]

[6]

Correct answers: [2]

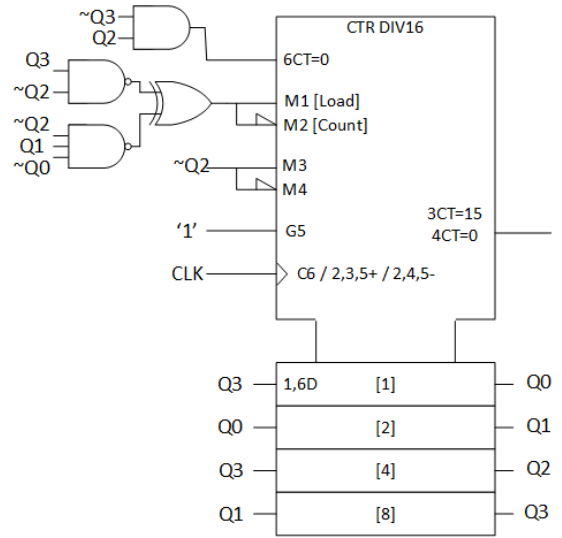
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]
[1]	→	[3]	[2]	[1]	[3]	[1]	[3]	[1]	[4]
[2]	→	[5]	[5]	[3]	[2]	[2]	[5]	[5]	[2]
[3]	→	[1]	[1]	[2]	[5]	[3]	[4]	[3]	[1]
[4]	→	[4]	[4]	[5]	[4]	[4]	[1]	[4]	[5]
[5]	→	[2]	[3]	[4]	[1]	[5]	[2]	[2]	[3]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

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R. Which of the following options corresponds to the sequence, in stationary mode, in decimal format at the output of the circuit in the figure below? (suggestion: start by analyzing a "load" situation.)

[Qual das seguintes opções corresponde à sequência de saída do seguinte circuito, em regime estacionário e em formato decimal? (sugestão: comece por analisar a situação de carregamento ("load") de dados.)]



- [1]: 5 - 0 - 1 - 2 - 8 - 5 ...
- [2]: 9 - 8 - 7 - 4 - 3 - 9 ...
- [3]: 4 - 12 - 0 - 1 - 2 - 3 - 4 ...
- [4]: 4 - 12 - 11 - 10 - 8 - 3 - 4 ...
- [5]: 12 - 0 - 1 - 2 - 3 - 4 - 11...
- [6]: None of the other options
[Nenhuma das outras opções]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1]	→ [1]	[3]	[5]	[1]	[5]	[2]	[5]	[3]	[5]
[2]	→ [4]	[5]	[2]	[2]	[1]	[3]	[2]	[4]	[4]
[3]	→ [5]	[4]	[1]	[5]	[4]	[1]	[4]	[5]	[2]
[4]	→ [3]	[1]	[4]	[3]	[2]	[4]	[1]	[1]	[1]
[5]	→ [2]	[2]	[3]	[4]	[3]	[5]	[3]	[2]	[3]
[6]	→ [6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

(This space was intentionally left blank for you auxiliary calculations.)

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Volume 1 - Part II

NOTE: Portuguese version bellow

[Question score partitioning: 35% + 35% + 30%]

Assume a drone can lift a cargo of 9 Kg and that, when in suspension, it selects the blade speed based V on the cargo P using the formula:

Blade speed $V = 9/2 \times P$ (thousands of rpms).

1. Assume that the cargo P is given by a sensor that outputs an unsigned 4-bit signal (in Kg). Draw the logic diagram of the circuit that calculates V given P . Use 8 bits to represent signal V . Use only 4-bit adders and discrete logic.
2. The actual blade speed (divided by 3) U is measured using another unsigned 6-bit sensor. Draw the logic diagram of the circuit that determines the error signal E equal to $3U - V$. Use only 8-bit adders and discrete logic. Ignore overflows.
3. Design a circuit that activates an output alarm signal when the cargo is greater than or equal to 10 Kg. Use only discrete logic.



Suponha que um drone pode levantar uma carga de 9 Kg e que, quando em suspensão, seleciona a velocidade das hélices com base na carga P usando a fórmula:

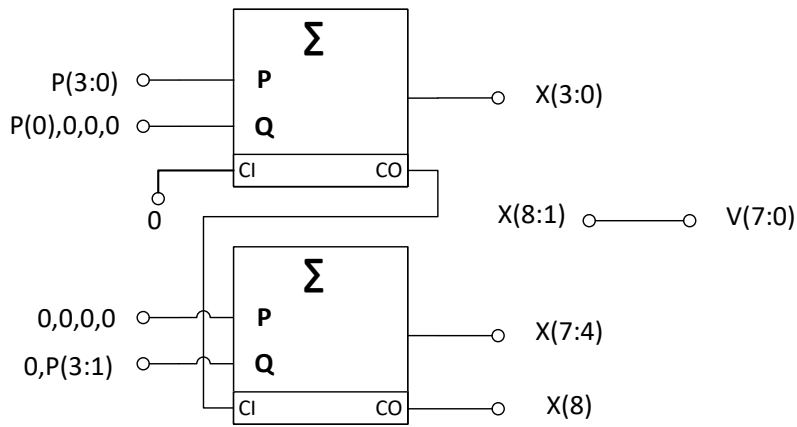
Velocidade das hélices $V = 9/2 \times P$ (milhares de rpms).

1. Suponha que a carga P é medida por um sensor resultando num sinal de 4 bits sem sinal (em Kg). Desenhe o diagrama lógico do circuito que calcula V dado P . Use 8 bits para representar o sinal V . Use apenas somadores de 4 bits e lógica discreta.
2. A velocidade real das hélices (dividida por 3) U é medida usando outro sensor de 6 bits sem sinal. Projete o circuito que determina o sinal de erro E igual a $3U - V$. Use apenas somadores de 8 bits e lógica discreta. Ignore *overflows*.
3. Projete um circuito que ative um sinal de alarme quando a carga for maior ou igual a 10 Kg. Use apenas lógica discreta.

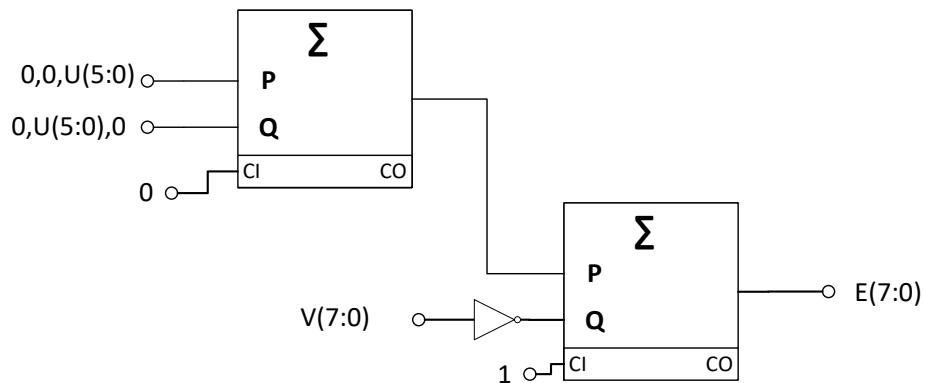


Solução Proposta:

1



2



3

$$A = P(3) P(1) + P(3) P(2)$$

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Volume 1 - Part III

NOTE: Portuguese version in the following page

[Question score partitioning: 50% + 50%]

Question A:

Design a circuit that controls a self-service checkout (SCO) of the type used in super-markets. The controller to be developed works as follows:



- Unless otherwise indicated, all the signals are Active High.
- There is one external timer, whose outputs are inputs of the control state machine. The timer starts when signal AT makes a transition from '0' to '1'. The timer is deactivated when AT returns to '0', after which it becomes ready for a new activation. Input TO is activated when the timer expires after an interval of duration TI, and remains activated until AT returns to '0'.
- The initial state corresponds to the idle state. In this state, the controller waits for input signal ID to be active, which indicates that the user has successfully identified itself to the SCO interface. This triggers the beginning of the session.
- The first phase of the session consists of registering products. Throughout this phase, a green LED (output signal GL) remains lit.
- During the product registration phase, the controller waits for the activation of input signal BC, which indicates that a product bar code was read. Then, the controller waits for a product with the correct weight to be placed on the weight scale, which is signaled by input signal SC.
- During the product registration phase, waiting for BC is limited to an interval TI, and the same applies when waiting for SC. If the timer expires while waiting, the controller returns to the initial state.
- When the controller is waiting for a bar code to be read, activation of input FI means that the user has pressed the button to finish. In this case, the controller moves to the payment phase, throughout which a yellow LED (output signal YL), and only this one, remains lit. The controller then waits for payment to finish, which is indicated by the activation of input signal PM. After payment is concluded, the controller returns to the initial state. During the payment phase, if an interval of length TI passes without concluding payment, the controller returns to the initial state.

Consider the incomplete state diagram of the Moore machine of the circuit (see Volume 2, Part III).

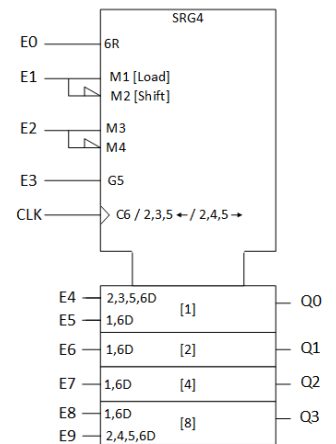
Complete the diagram, defining the values of the input signals associated with all state transitions, as well as the values of the output signals associated with each state. "Don't cares" must be used for the inputs whose value does not matter for given a state transition. In the diagram, indicate the inputs/outputs according to the following order:

- Order of the inputs: ID, BC, SC, FI, PM, TO.
- Order of the outputs: GL, YL, AT.

Question B:

IMPORTANT: This page will **NOT** be considered for your evaluation

Consider a state machine with input A and state bits Q3, Q2, Q1 and Q0, implemented with the circuit depicted in the figure. Complete the state transition table (see Volume 2, Part IIIB), considering the provided state transitions. Justify, identifying the operation performed by the circuit in each transition. **Note: The parallel LOAD operation will only be accepted in case there is no other alternative leading to the same result. The signals that don't care to a given operation must mandatorily be marked as don't cares.**



Pergunta A:

Projete um circuito para controlar uma caixa de pagamento automático (CPA) do tipo utilizado em supermercados. O controlador a desenvolver funciona da seguinte forma:



- A não ser que se especifique o contrário, todos os sinais são Ativos a High.
- A menos que indicado de outra forma, todos os sinais são Ativos a High.
- Existe um temporizador externo, cujas saídas são entradas da máquina de estados de controlo. O temporizador inicia a contagem quando o sinal AT faz uma transição de '0' para '1'. O temporizador é desativado quando AT retorna a '0', após o que fica pronto para uma nova ativação. A entrada TO é ativada quando o temporizador expira após um intervalo de duração TI, e permanece ativada até que AT retorne a '0'.
- O estado inicial corresponde ao estado sem atividade. Neste estado, o controlador espera pela ativação do sinal de entrada ID, o que indica que o utilizador se identificou com sucesso no interface da CPA. Este evento dá início à sessão.
- A primeira parte da sessão consiste no registo de produtos. Durante este fase, um LED verde (sinal de saída GL) permanece aceso.
- Durante a fase de registo de produtos, o controlador aguarda a ativação do sinal de entrada BC, que indica que o código de barras de um produto foi lido. Então, o controlador passa a aguardar que um produto com o peso correto seja colocado na balança, o que é sinalizado pelo sinal de entrada SC.
- Durante a fase de registo de produtos, a espera por BC está limitada a um intervalo de duração TI, e o mesmo acontece à espera por SC. Se o temporizador expirar durante a espera, o controlador regressa ao estado inicial.
- Enquanto o controlador aguarda a leitura do código de barras, a ativação do sinal FI significa que o utilizador pressionou o botão para terminar a sessão. Neste caso, o controlador passa à fase de pagamento, durante a qual um LED amarelo (sinal de saída YL), e apenas este, permanece aceso. O controlador aguarda então que o pagamento termine, o que é indicado através da ativação do sinal de entrada PM. Após conclusão do pagamento, o controlador regressa ao estado inicial. Durante a fase de pagamento, caso passe mais de um intervalo de tempo TI sem o pagamento se concluir, o controlador regressa ao estado inicial.

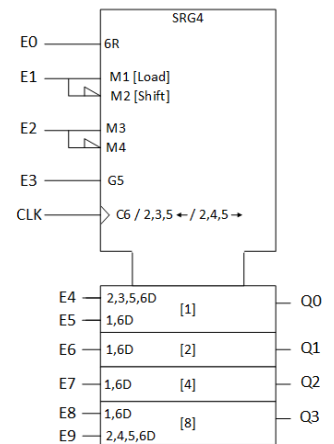
Considere o diagrama de estados incompleto da máquina de Moore do circuito (ver Volume 2, Parte III).

Complete o diagrama, definindo os valores dos sinais de entrada que desencadeiam todas as transições de estado, assim como os valores de saída de cada estado. As "indiferenças" têm de ser obrigatoriamente usadas para entradas que não tenham influência numa determinada transição de estado. As entradas/saídas têm de ser indicadas de acordo com a ordem seguinte:

- Ordem das entradas: ID, BC, SC, FI, PM, TO.
- Ordem das saídas: GL, YL, AT.

Pergunta B:

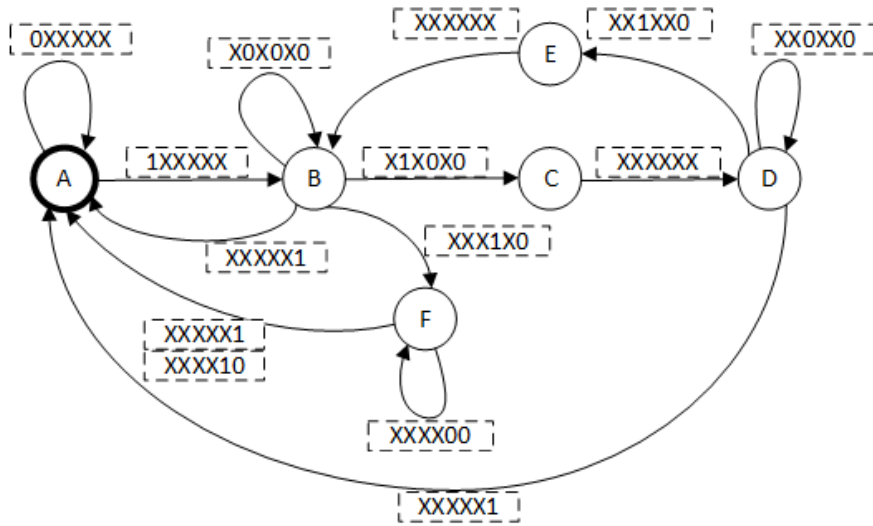
Considere uma máquina de estados com entrada A e bits de estado Q3, Q2, Q1 e Q0, realizada com base no circuito da figura. Complete a tabela de transição de estados (ver Volume 2, Parte IIIB), considerando as transições nela representadas. Justifique, identificando na tabela as operações realizadas em cada transição. **Nota: A operação de carregamento em paralelo (LOAD) só será aceite se não houver uma operação alternativa que conduza ao mesmo resultado. Os sinais indiferentes para determinada operação têm obrigatoriamente de ser marcados como indiferenças.**



Solução Proposta:

Pergunta A:

- A: Initial state [Estado inicial]
- B: Wait for bar code reading [Esperar pela leitura do código de barras]
- C: Reset timer before D [Desativar o temporizador antes de D]
- D: Wait for product in the scale [Esperar por produto na balança]
- E: Reset timer before B [Desativar o temporizador antes de B]
- F: Wait for payment [Esperar pagamento]



- A: 000
- B: 101
- C: 100
- D: 101
- E: 100
- F: 011

Pergunta B:

$Q_3^n Q_2^n Q_1^n Q_0^n$	A	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	$Q_3^{n+1} Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}$	Operation
0000	0	0	0	X	0	X	X	X	X	X	X	0000	HOLD
0000	1	0	0	1	1	1	X	X	X	X	X	0001	SHL
0001	0	0	0	0	1	X	X	X	X	X	0	0000	SHR
0001	1	0	0	1	1	1	X	X	X	X	X	0011	SHL
0011	0	0	0	0	1	X	X	X	X	X	1	1001	SHR
0011	1	1	X	X	X	X	X	X	X	X	X	0000	RESET
1001	0	0	1	X	X	X	1	0	0	0	X	0001	LOAD
1001	1	0	0	1	1	1	X	X	X	X	X	0011	SHL

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**Don't forget to identify this and the following pages!
Only these pages will be considered for your evaluation.**

Volume 2 - Part I

For each question of Part I (question A, B, C, ...), fill in the number of the **correct answer** from the supplied multiple-choice list (answer 1, 2, 3, ...):

*	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
9																			X	X	X	X	X	X	X	X

NOTE: Leave blank (or fill in with 0) all questions that you do not wish to answer.

Volume 2 - Part I (Cont.)

Volume 2 - Part II

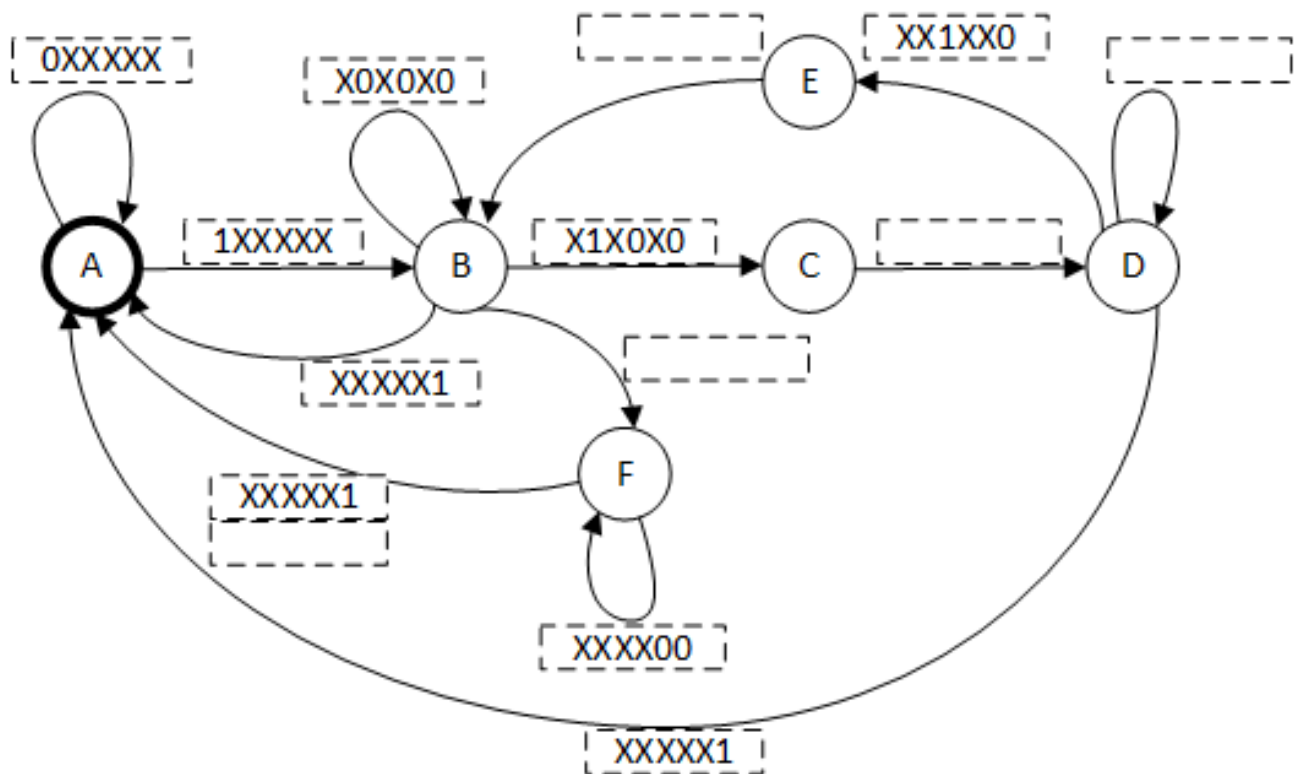
Volume 2 - Part II (Cont.)

Volume 2 - Part III

Pergunta A:

Meaning of the states [*Significado dos estados*]:

- A: Initial state [Estado inicial];
- B: Wait for bar code reading [*Esperar pela leitura do código de barras*];
- C: Reset timer before D [*Desativar o temporizador antes de D*];
- D: Wait for product in the scale [*Esperar por produto na balança*];
- E: Reset timer before B [*Desativar o temporizador antes de B*];
- F: Wait for payment [*Esperar pagamento*];



For each state, define the values of the inputs (in the diagram) and of the outputs (below) according to the following order:
 [Para cada estado, indique os valores das entradas (no diagrama) e das saídas (em baixo) de acordo com a seguinte ordem]:

- Order of the inputs [*Ordem das entradas*]: ID, BC, SC, FI, PM, TO.
- Order of the outputs [*Ordem das saídas*]: GL, YL, AT.

- A: _____
- B: _____
- C: _____
- D: _____
- E: _____
- F: _____

Pergunta B:

Number: _____ Name: _____

Degree: LEEC LEAer LEFT

$Q_3^n Q_2^n Q_1^n Q_0^n$	A	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	$Q_3^{n+1} Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}$	Operation
0000	0	0										0000	
0000	1	0										0001	
0001	0	0										0000	
0001	1	0										0011	
0011	0	0										1001	
0011	1	1										0000	
1001	0	0										0001	
1001	1	0										0011	

