

Instructions

Before starting the exam, read carefully the following information:

- There are (at least) nine different versions of this exam.
- Although the exam comprises a total of 21 pages, there are two distinct volumes that should be handled as follows:
 - **Volume 1** corresponds to the question list and comprises pages 1 to 16. These pages do not need to be identified because they will be discarded at the end of the exam;
 - **Volume 2** corresponds to the answers sheet and comprises pages 17 to 21. All pages of this volume **MUST** be identified with the **student's name** and **number**.
 - At the end of the exam, all pages of **Volume 2** will be separated. Consequently, all non-identified pages will not be considered.
- The exam is composed of three parts (Part I, II and III) and has a duration of 2 (two) hours.
 - **Part I** comprises N_1 multiple choice questions and awards a total of $P_1 = 15$ points.
 - * Each correct answer awards $C = P_1/N_1$ points;
 - * Each wrong answer awards $W = -C/(A - 1)$ points (negative value), where A denotes the number of possible answers offered to each question;
 - * Each non-answered question awards 0 points.
 - **Part II** comprises an open-answer problem about combinatorial circuits and awards a total of $P_2 = 2.5$ points.
 - **Part III** comprises an open-answer problem about sequential circuits and awards a total of $P_3 = 2.5$ points.
 - All question answers **MUST** be replied in the allotted space of **Volume 2**.
- At the end of **Part I of Volume 1** you will find an empty page - you can use it for auxiliary calculations, but this page will not be delivered at the end. This means that all answers **MUST** be replied (and properly justified) in the allotted space of **Volume 2**.
- Each question includes a Portuguese translation of the corresponding text. In case of a mismatch between the English text and its translation, the English text will be the one to be considered in the evaluation¹.
- You cannot use or consult any material during the exam. On your desk you can only have a pen and your student identity card.

¹Cada pergunta inclui uma tradução para Português do referido texto. Em caso de incoerência entre o texto em Inglês e a sua tradução, será o texto em Inglês que será considerado na avaliação.

Volume 1 - Part I

A. Represent 11010010_2 in octal.

[Represente 10010111_2 em octal.]

[1]: 322

[2]: D2

[3]: 427

[4]: 210

[5]: A2

[6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

B. Represent B_{416} in base 10.

[Represente B_{416} na base 10.]

[1]: 180

[2]: 264

[3]: 138

[4]: 087

[5]: 501

[6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

C. Which of the following expressions corresponds to the minimal function (defined as a product-of-sums) represented in the Karnaugh-map?

[Qual das seguintes expressões corresponde à função mínima (definida como um produto de somas) representada no mapa de Karnaugh?]

[1]: $(\bar{A} + B)(\bar{A} + \bar{B})(\bar{B} + D)$

[2]: $(\bar{A} + C)(A + \bar{C})(B + \bar{D})$

[3]: $(B + \bar{C})(\bar{B} + D)(C + \bar{D})$

[4]: $(A + \bar{C})(\bar{B} + D)(\bar{B} + D)$

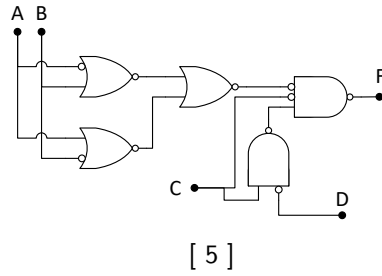
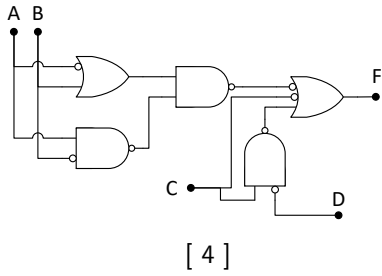
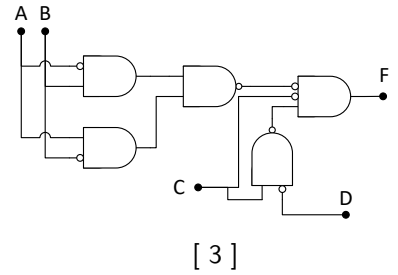
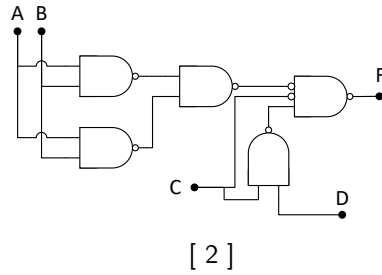
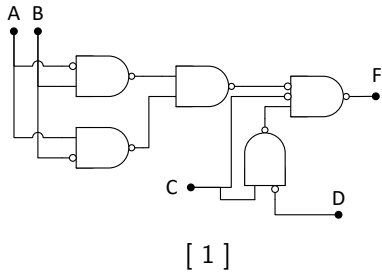
[5]: $(\bar{A} + \bar{C})(A + D)(B + \bar{C})$

[6]: None of the other options [Nenhuma das outras opções]

		CD			
		00	01	11	10
AB	00	1	0	0	0
	01	1	1	X	0
	11	X	0	1	1
	10	0	0	0	1

Correct answers: [2]

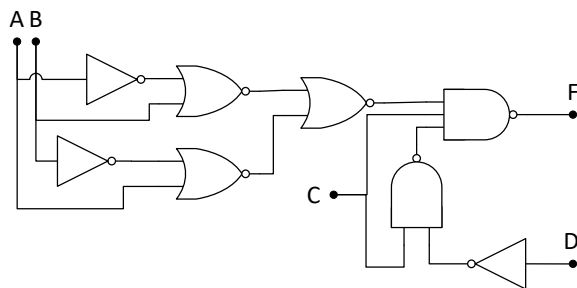
D. Which of the following circuits implements the expression $(A \oplus B) + C + \overline{D}C$?
 [Qual dos seguintes circuitos implementa a expressão $(A \oplus B) + C + \overline{D}C$?



None of the other options
 [Nenhuma das outras opções]
 [6]

Correct answers: [1]

E. What is the worst case for the propagation time of the following circuit?
 [Qual é o pior caso para o tempo de propagação do seguinte circuito?]



Gate	tp [ns]
NOT	5
NAND	9
NOR	10

[1]: 34
 [4]: 30

[2]: 26
 [5]: 50

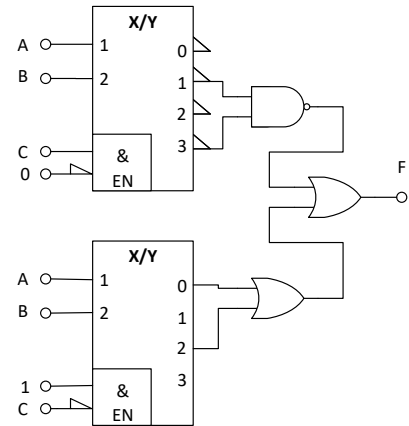
[3]: 38
 [6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

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F. Select the option corresponding to the output $f(A, B, C)$ of the circuit shown below, when the inputs (A, B, C) have the values $(0, 0, 1), (0, 1, 0)$, and $(1, 1, 1)$.
 [Indique qual das opções corresponde à saída $f(A, B, C)$ do circuito apresentado em baixo, quando as entradas (A, B, C) tomam os valores $(0, 0, 1), (0, 1, 0)$, e $(1, 1, 1)$.]

- [1]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{0 ; 0 ; 1\}$
- [2]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{1 ; 0 ; 1\}$
- [3]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{1 ; 0 ; 0\}$
- [4]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{1 ; 0 ; 0\}$
- [5]: $\{f(0, 0, 1) ; f(0, 1, 0) ; f(1, 1, 1)\} = \{0 ; 1 ; 0\}$
- [6]: None of the other options [Nenhuma das outras opções]



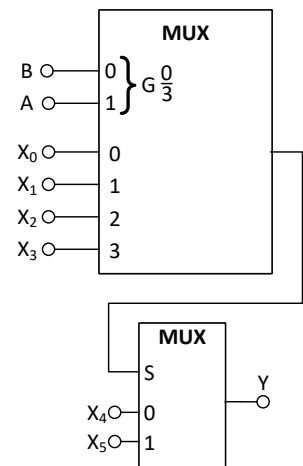
Correct answers: [6]

G. Consider the following circuit and truth table. Select the multiplexer inputs $\{X_5, X_4, X_3; X_2; X_1; X_0\}$ that result in the given truth table.

[Considere o seguinte circuito e tabela de verdade. Selecione as entradas do multiplexer $\{X_5, X_4, X_3; X_2; X_1; X_0\}$ que resultam na tabela apresentada.]

- [1]: $\{X_5, X_4, X_3; X_2; X_1; X_0\} = \{0, 1, C; C; C; 1\}$
- [2]: $\{X_5, X_4, X_3; X_2; X_1; X_0\} = \{1, 0, \bar{C}; C; 0; C\}$
- [3]: $\{X_5, X_4, X_3; X_2; X_1; X_0\} = \{0, 1, C; \bar{C}; C; 1\}$
- [4]: $\{X_5, X_4, X_3; X_2; X_1; X_0\} = \{1, 0, \bar{C}; 1; 0; C\}$
- [5]: $\{X_5, X_4, X_3; X_2; X_1; X_0\} = \{1, 1, C; \bar{C}; \bar{C}; 1\}$
- [6]: None of the other options
[Nenhuma das outras opções]

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



Correct answers: [1]

H. What is the 8-bit two's complement representation of -77 ?

[Qual é a representação em complemento para dois com 8-bits de -77 ?]

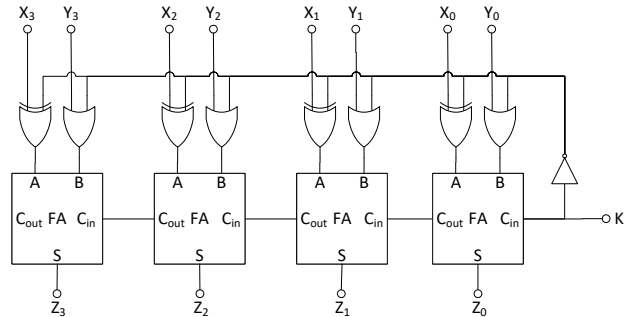
- [1]: 10110011
- [2]: 10101101
- [3]: 01001110
- [4]: 10110001
- [5]: 10011011
- [6]: None of the other options [Nenhuma das outras opções]

Correct answers: [1]

This page will be discarded

- I. Which function is implemented by the following circuit? Consider that X and Y are 4-bit signed numbers (two's complement).
 [Qual é a função desempenhada pelo seguinte circuito? Assuma que X e Y são números com sinal com 4-bits (em complemento para dois).]

- [1]: $K=0: Z=-X-2$; $K=1: Z=X+Y+1$
- [2]: $K=0: Z=X-Y$; $K=1: Z=Y+1$
- [3]: $K=0: Z=X-2$; $K=1: Z=X+Y+1$
- [4]: $K=0: Z=X+2$; $K=1: Z=X-Y$
- [5]: $K=0: Z=X+1$; $K=1: Z=X-Y$
- [6]: None of the other options
 [Nenhuma das outras opções]

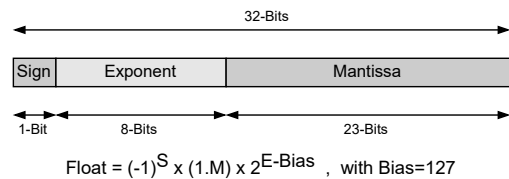


Correct answers: [1]

- J. The following 32-bit words correspond to signed rational numbers represented in fixed-point and floating-point. Which of the options presented below corresponds to an ascending ordering of these words?
 [As seguintes palavras de 32-bits correspondem a números racionais com sinal representados em vírgula fixa e em vírgula flutuante. Qual das opções corresponde à ordenação crescente destas palavras?]

A = 4FB70A3Dh (IEEE-754) B = 48005603h (Q2.30) C = B0006501h (Q1.31)

- [1]: A,B,C [2]: B,A,C [3]: C,A,B
- [4]: A,C,B [5]: B,C,A [6]: C,B,A



Correct answers: [6]

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K. Consider the following state transition table (one-hot encoding) with two inputs $Init$ and X , two outputs $Y1$ and $Y0$, where each state $S_i (i = 0, \dots, 3)$ is implemented with D flip-flops, with input D_i (next state) and output Q_i (current state). Select, only for the state S_2 , the correct option for D_2 as a function of $Init$ and X and the current states Q_i .

[Considere a seguinte tabela de transição de estados (codificação one-hot) com duas entradas $Init$ e X , duas saídas $Y1$ e $Y0$, em que cada estado $S_i (i = 0, \dots, 3)$ é implementado com flip-flops do tipo D, com entradas D_i (próximo estado) e saídas Q_i (estado actual). Indique, para o estado S_2 , a expressão de D_2 como função de $Init$ e X e os estados actuais Q_i .]

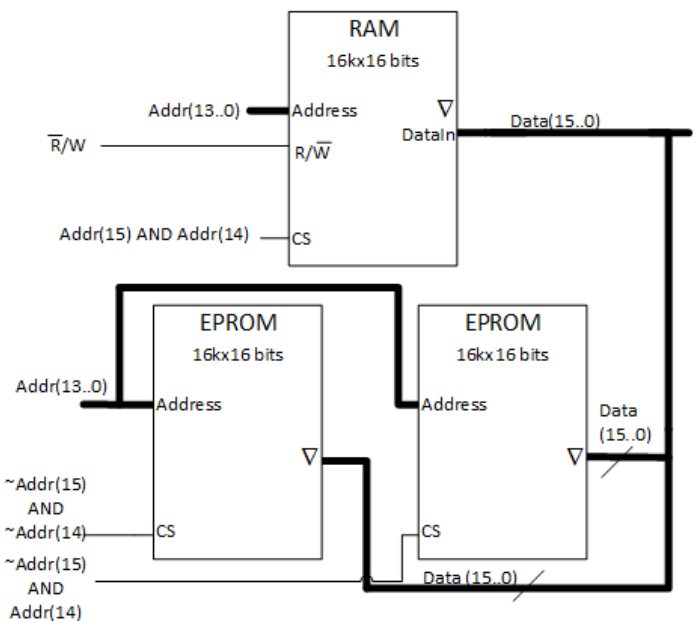
Q3(n)	Q2(n)	Q1(n)	Q0(n)	Init	X	Q3(n+1)	Q2(n+1)	Q1(n+1)	Q0(n+1)	Y1	Y0
0	0	0	1	0	0	0	1	0	0	1	1
0	0	0	1	0	1	0	1	0	0	1	1
0	0	1	0	0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	0	1	0
0	1	0	0	0	0	0	1	0	0	0	0
0	1	0	0	0	1	0	0	0	1	1	1
1	0	0	0	0	0	0	0	1	0	1	1
1	0	0	0	0	1	0	1	0	0	1	0
-	-	-	-	1	-	0	1	0	0	1	0

- [1]: $D_2 = Init + Q_0 + \bar{X} \cdot Q_1 + \bar{X} \cdot Q_2 + X \cdot Q_3$
- [2]: $D_2 = Init + Q_0 + \bar{X} \cdot Q_1 + \bar{X} \cdot Q_2 + X \cdot Q_3$
- [3]: $D_2 = Init + Q_0 + X \cdot Q_1 + \bar{X} \cdot Q_2 + X \cdot Q_3$
- [4]: $D_2 = Init + X \cdot Q_0 + \bar{X} \cdot Q_1 + X \cdot Q_2 + X \cdot Q_3$
- [5]: $D_2 = Init + \bar{X} \cdot Q_0 + X \cdot Q_1 + X \cdot Q_2 + \bar{X} \cdot Q_3$
- [6]: None of the other options
[Nenhuma das outras opções]

Correct answers: [1]

L. Consider the following memory system. Indicate the range of addresses that correspond to RAM and EPROM.

[Considere o seguinte sistema de memória. Indique os intervalos de endereços que correspondem a RAM e EPROM.]

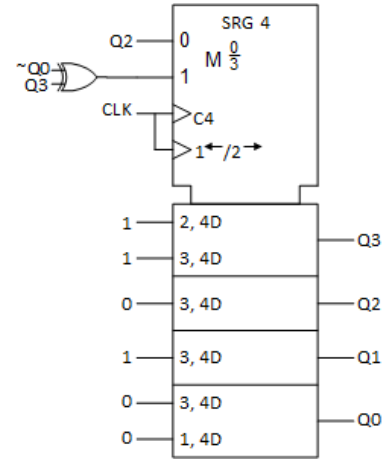


- [1]: RAM:C000h..FFFFh;
EPROM:0000h..7FFFh
- [2]: RAM:A000h..CFFFh;
EPROM:0000h..7FFFh
- [3]: RAM:B000h..BFFFh;
EPROM:0000h..EFFFh
- [4]: RAM:C000h..CFFFh;
EPROM:7000h..EFFFh
- [5]: RAM:D000h..DFFFh;
EPROM:8000h..8FFFh
- [6]: None of the other options
[Nenhuma das outras opções]

Correct answers: [1]

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M. Consider the following circuit with a 4-bit shift register, as depicted in the figure. The current state is $Q_3 Q_2 Q_1 Q_0 = 1011$. What are the next two states of the circuit?
 [Considere o seguinte circuito com um registo de deslocamento de 4-bits representado na figura. O estado actual é $Q_3 Q_2 Q_1 Q_0 = 1011$. Quais serão os próximos dois estados?]

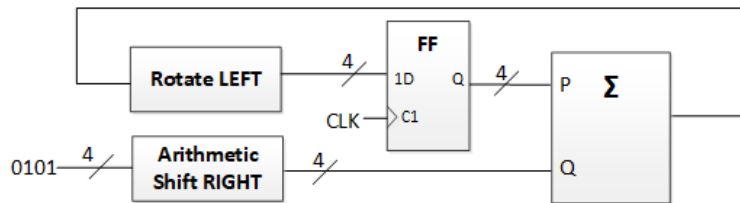


- [1]: 1101, 1010
- [2]: 0011, 1011
- [3]: 1110, 0110
- [4]: 1010, 0110
- [5]: 1001, 1101
- [6]: None of the other options
[Nenhuma das outras opções]

Correct answers: [1]

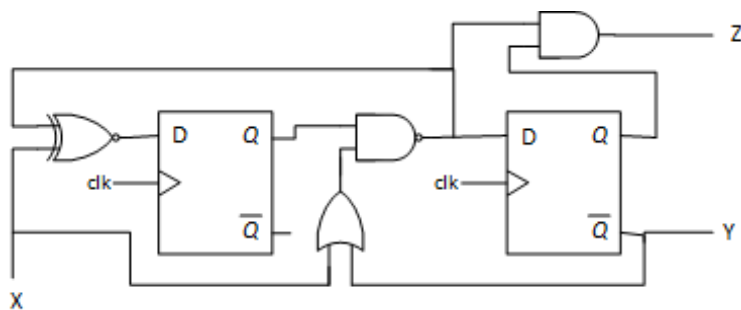
N. Consider the following circuit with an adder, a register (4 FF's) and a combinational logic circuit. Assuming that the current state is $Q(3:0) = 1100$, what are the next two states of the circuit?
 [Considere o seguinte circuito com um somador, um registo (4 FF's) e lógica combinatória. Assumindo que o estado actual é $Q(3:0) = 1100$, quais serão os próximos dois estados do circuito?]

- [1]: 1101, 1111
- [2]: 1100, 1000
- [3]: 0011, 1110
- [4]: 1010, 1011
- [5]: 0101, 0101
- [6]: None of the other options
[Nenhuma das outras opções]



Correct answers: [1]

O. What is the minimum clock period of the following circuit, given the table values (in ns)?
 [Qual é o período de relógio mínimo do seguinte circuito, assumindo os valores da tabela (em ns)?]



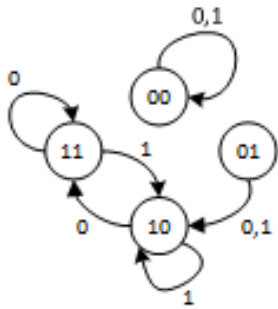
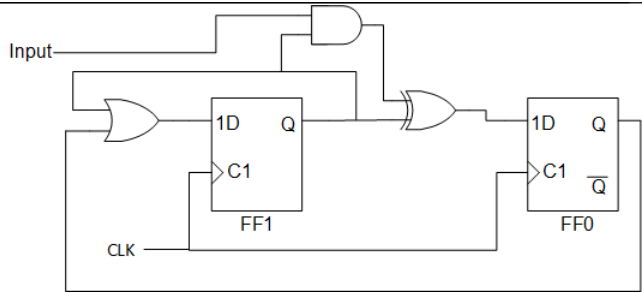
	tp [ns]	tsu [ns]	th [ns]
FF D	13	6	8
NAND	4		
AND	6		
XNOR	12		
OR	5		

- [1]: 40
- [2]: 45
- [3]: 41
- [4]: 50
- [5]: 51
- [6]: None of the other options [Nenhuma das outras opções]

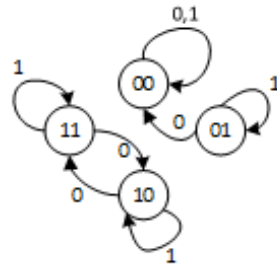
Correct answers: [1]

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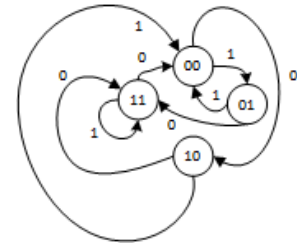
Q. Consider the following circuit. Which state diagram corresponds to the circuit?
 [Considere o seguinte circuito. Qual dos diagramas de estado corresponde ao funcionamento do circuito?]



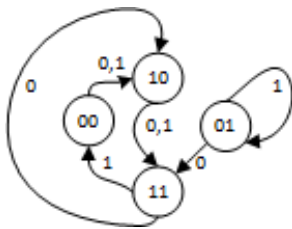
[1]



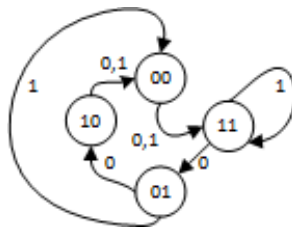
[2]



[3]



[4]



[5]

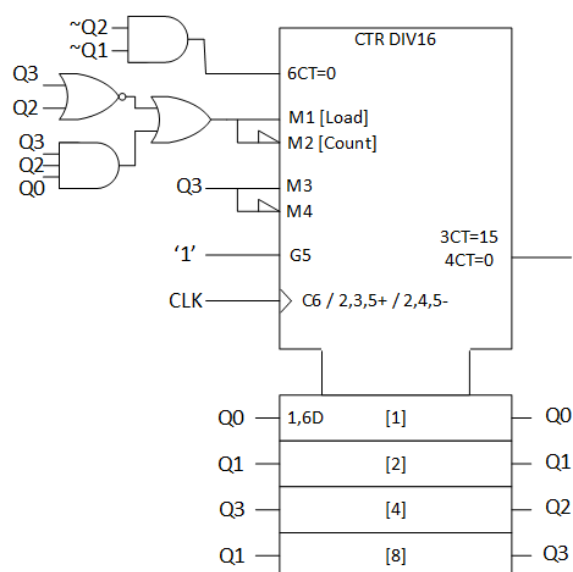
None of the other options
 [Nenhuma das outras opções]

[6]

Correct answers: [1]

R. Which of the following options corresponds to the sequence, in stationary mode, in decimal format at the output of the circuit in the figure below? (suggestion: start by analyzing a "load" situation.)

[Qual das seguintes opções corresponde à sequência de saída do seguinte circuito, em regime estacionário e em formato decimal? (sugestão: comece por analisar a situação de carregamento ("load") de dados.)]



[1]: ... 3 - 11 - 12 - 13 - 5 - 4 - 3 ...

[2]: ... 5 - 12 - 13 - 14 - 7 - 6 - 5 ...

[3]: ... 14 - 3 - 2 - 1 - 12 - 13 - 14 ...

[4]: ... 11 - 3 - 4 - 5 - 13 - 12 - 11 ...

[5]: ... 11 - 5 - 4 - 3 - 9 - 10 - 11 ...

[6]: None of the other options
 [Nenhuma das outras opções]

Correct answers: [1]

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Volume 1 - Part II

NOTE: Portuguese version in the following

[Question score partitioning: 33% + 34% + 33%]

In the following questions, design circuits that calculate the desired signals using 8-bit adders and discrete logic. Always assume 8-bit unsigned inputs and outputs, ignore output saturation, and prevent it in internal calculations. Assume a river that has an average discharge of $D = 100 \text{ m}^3/\text{s}$ and an area of $A = 12 \text{ Mm}^2$.

1. Given the precipitation p in $L/\text{m}^2/\text{h}$ first convert it to p_1 in $\text{m}^3/\text{Mm}^2/\text{s}$ by multiplying by $9/32$.
2. Calculate the total water volume v in m^3 that falls in the river per second using $v = p_1 A$ ($A = 12 = 1100_2$).
3. Consider an irrigation system that takes $r/2 \text{ m}^3/\text{s}$ from the river. Determine the resulting water flow $v_1 = v - r/2$ given the v and r inputs.
4. Draw the circuit that allows you to determine if the rain fall on the river is bigger than the discharge predicting a flood, $v > D$, where D takes the value given above.

Versão Portuguesa:

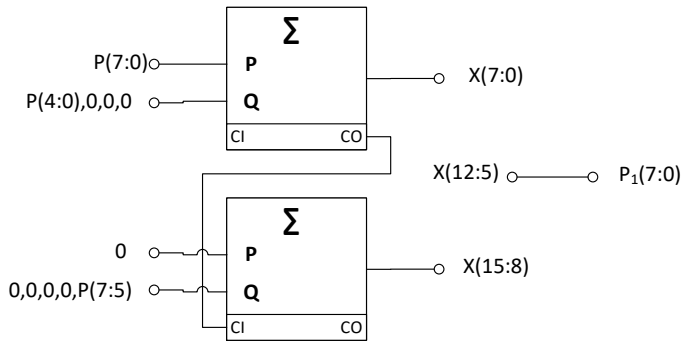
Nas questões que se seguem, projete circuitos que calculem os sinais desejados usando somadores de 8 bits e lógica discreta. Assuma entrada e saída de 8 bits sem sinal, ignore a saturação de saída e evite-a em cálculos internos. Suponha um rio que tenha uma vazão média de $D = 100 \text{ m}^3/\text{s}$ e uma área de $A = 12 \text{ Mm}^2$.

1. Dada a precipitação p em $L/\text{m}^2/\text{h}$ primeiro converta-a para p_1 em $\text{m}^3/\text{Mm}^2/\text{s}$ multiplicando por $9/32$.
2. Calcule o volume total de água v em m^3 que cai no rio por segundo usando $v = p_1 A$ ($A = 12 = 1100_2$).
3. Considere um sistema de irrigação que retira $r/2 \text{ m}^3/\text{s}$ do rio. Determine o fluxo de água resultante $v_1 = v - r/2$ dadas as entradas v e r .
4. Desenhe o circuito que permite determinar se a queda de chuva no rio é maior que a vazão prevendo uma enchente, $v > D$, onde D assume o valor dado em cima.

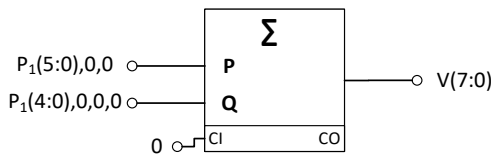


Solução Proposta:

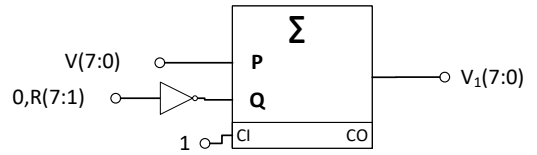
1



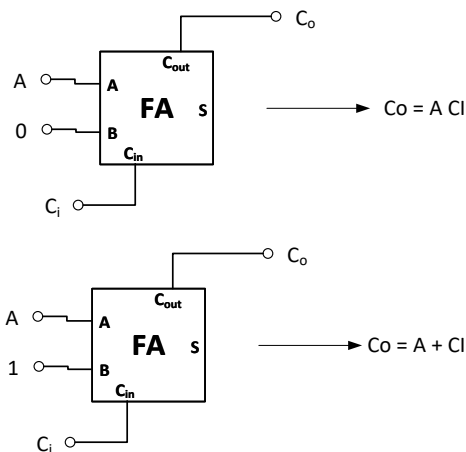
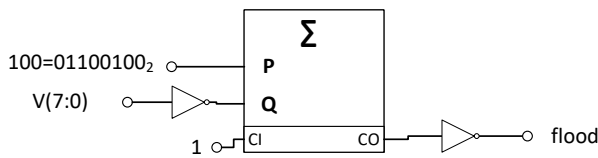
2



3



4



The circuit simplifies to:

$$\text{flood} = V7 + V6 V5 (V4 + V3 + V2 (V1 + V0))$$

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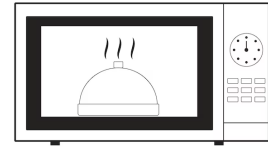
Volume 1 - Part III

NOTE: Portuguese version in the following page

[Question score partitioning: 50% + 50%]

Question A:

Design a circuit that controls a microwave oven. The microwave oven works as follows:



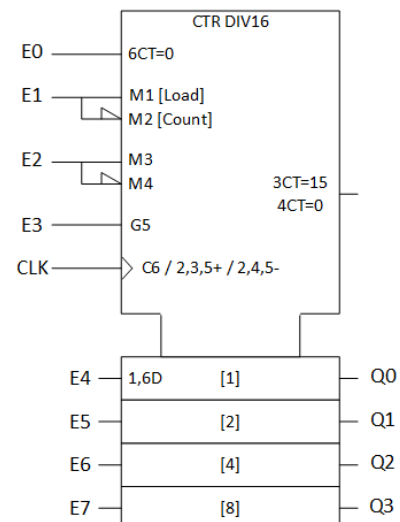
- Unless otherwise indicated, all the signals are Active High.
- There is one external timer, whose outputs are inputs of the control state machine. The timer starts when signal **TIMER_ACT** makes a transition from '0' to '1'. The timer is deactivated when **TIMER_ACT** returns to '0', after which it becomes ready for a new activation. Input **TIMEOUT** is activated when the timer expires after an interval of duration **TI**, and remains activated until **TIMER_ACT** returns to '0'.
- A switch called **HTIME** allows the user to select between two heating durations, measured in intervals of duration **TI**. Each position of the switch corresponds to a different heating duration: '0' means $1 \times TI$, while '1' means $2 \times TI$.
- The **START** input signal is obtained from a button, and it initiates the heating process. The heating process has the duration selected by **HTIME**, after which it finishes. Once started, the heating process cannot be restarted unless signal **START** remains deactivated for at least one clock cycle.
- Output signal **HEAT** activates the heating mechanism of the microwave oven.
- The heating process can be aborted by opening the door, which is indicated by input signal **DOOR**. Input signal **DOOR** equal to '1' indicates that the door is open, while a value of '0' indicates that the door is closed. Attention: heating cannot start while the door is open.

Consider the incomplete state diagram of the Moore machine of the circuit (see Volume 2, Part III). Complete the diagram, defining the values of the input signals associated with all state transitions, as well as the values of the output signals associated with each state. "Don't cares" must be used for the inputs whose value does not matter for given a state transition. In the diagram, indicate the inputs/outputs according to the following order:

- Order of the inputs: **START**, **DOOR**, **HTIME**, **TIMEOUT**.
- Order of the outputs: **HEAT**, **TIMER_ACT**.

Question B:

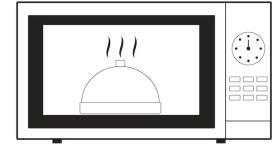
Consider a state machine with input **A** and state bits **Q3**, **Q2**, **Q1** and **Q0**, implemented with the circuit depicted in the figure. Complete the state transition table (see Volume 2, Part IIIB), considering the provided state transitions. Justify, identifying the operation performed by the circuit in each transition. **Note: The parallel LOAD operation will only be accepted in case there is no other alternative leading to the same result. The signals that don't care to a given operation must mandatorily be marked as don't cares.**



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Pergunta A:

Projete o circuito de controlo de um forno de micro-ondas. O forno de micro-ondas funciona da forma seguinte:



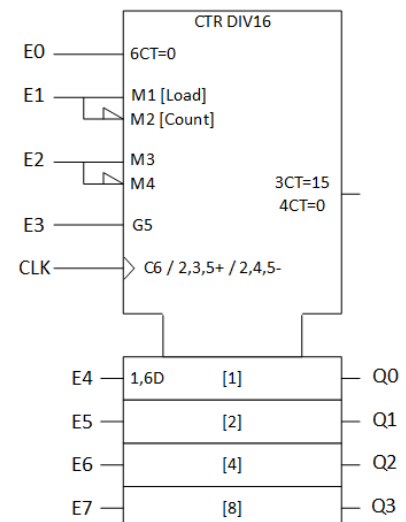
- A menos que indicado de outra forma, todos os sinais são Ativos a High.
- Existe um temporizador externo, cujas saídas são entradas da máquina de estados de controlo. O temporizador inicia a contagem quando o sinal `TIMER_ACT` faz uma transição de '0' para '1'. O temporizador é desativado quando `TIMER_ACT` retorna a '0', após o que fica pronto para uma nova ativação. A entrada `TIMEOUT` é ativada quando o temporizador expira após um intervalo de duração `TI`, e permanece ativada até que `TIMER_ACT` retorne a '0'.
- Um interruptor chamado `HTIME` permite ao utilizador seleccionar entre duas durações de aquecimento, medidas em intervalos de duração `TI`. Cada posição do interruptor corresponde a uma duração de aquecimento diferente: '0' significa $1 \times TI$, enquanto '1' significa $2 \times TI$.
- O sinal de entrada `START`, ativado através de um botão, inicia o processo de aquecimento. O processo de aquecimento tem a duração seleccionada por `HTIME`, após o qual termina. Uma vez iniciado, o processo de aquecimento não pode ser reiniciado a menos que o sinal `START` seja desativado durante pelo menos um ciclo de relógio.
- O sinal de saída `HEAT` ativa o mecanismo de aquecimento do micro-ondas.
- O processo de aquecimento pode ser abortado ao abrir a porta, o que é indicado pelo sinal de entrada `DOOR`. O sinal de entrada `DOOR` igual a '1' indica que a porta está aberta, enquanto um valor de '0' indica que a porta está fechada. O aquecimento não pode começar quando a porta está aberta. Atenção: o aquecimento não pode começar quando a porta está aberta.

Considere o diagrama de estados incompleto da máquina de Moore do circuito (ver Volume 2, Parte III). Complete o diagrama, definindo os valores dos sinais de entrada que desencadeiam todas as transições de estado, assim como os valores de saída de cada estado. As "indiferenças" têm de ser obrigatoriamente usadas para entradas que não tenham influência numa determinada transição de estado. As entradas/saídas têm de ser indicadas de acordo com a ordem seguinte:

- Ordem das entradas: `START`, `DOOR`, `HTIME`, `TIMEOUT`.
- Ordem das saídas: `HEAT`, `TIMER_ACT`.

Pergunta B:

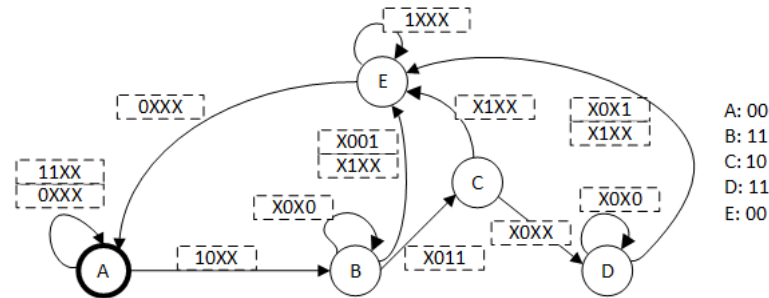
Considere uma máquina de estados com entrada `A` e bits de estado `Q3`, `Q2`, `Q1` e `Q0`, realizada com base no circuito da figura. Complete a tabela de transição de estados (ver Volume 2, Parte IIIB), considerando as transições nela representadas. Justifique, identificando na tabela as operações realizadas em cada transição. **Nota: A operação de carregamento em paralelo (LOAD) só será aceite se não houver uma operação alternativa que conduza ao mesmo resultado. Os sinais indiferentes para determinada operação têm obrigatoriamente de ser marcados como indiferenças.**



Solução Proposta:

Pergunta A:

- A: Initial state [Estado inicial]
- B: Heating during first TI [Aquecimento durante o primeiro TI]
- C: Deactivate timer preparing new activation [Desativar temporizador para preparar nova ativação]
- D: Heating during second TI [Aquecimento durante o segundo TI]
- E: Checking that START is deactivated [Verifica que START está desativado]



Pergunta B:

$Q_3^n Q_2^n Q_1^n Q_0^n$	A	E0	E1	E2	E3	E4	E5	E6	E7	$Q_3^{n+1} Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}$	Operation
0000	0	0	0	0	1	X	X	X	X	1111	DEC
0000	1	0	1	X	X	0	0	1	0	0100	LOAD
0001	0	0	0	1	1	X	X	X	X	0010	INC
0001	1	0	1	X	X	1	1	0	0	0011	LOAD
0100	0	1	X	X	X	X	X	X	X	0000	RESET
0100	1	0	0	1	1	X	X	X	X	0101	INC
1001	0	0	0	1	1	X	X	X	X	1010	INC
1001	1	0	1	X	X	1	1	1	0	0111	LOAD

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**Don't forget to identify this and the following pages!
Only these pages will be considered for your evaluation.**

Volume 2 - Part I

For each question of Part I (question A, B, C, ...), fill in the number of the **correct answer** from the supplied multiple-choice list (answer 1, 2, 3, ...):

★	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																			X	X	X	X	X	X	X	X

NOTE: Leave blank (or fill in with 0) all questions that you do not wish to answer.

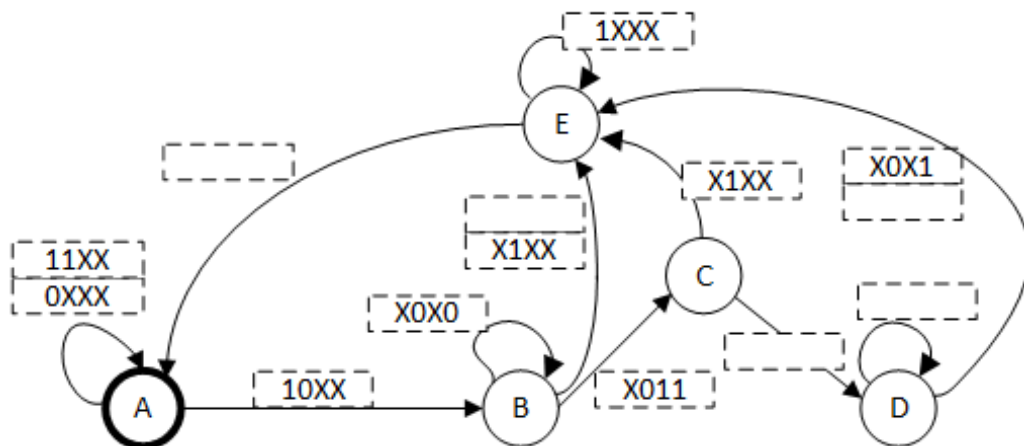
Volume 2 - Part II

Volume 2 - Part II (Cont.)

Volume 2 - Part III

Meaning of the states [*Significado dos estados*]:

- A: Initial state [Estado inicial]
- B: Heating during first TI [Aquecimento durante o primeiro TI]
- C: Deactivate timer preparing new activation [Desativar temporizador para preparar nova ativação]
- D: Heating during second TI [Aquecimento durante o segundo TI]
- E: Checking that START is deactivated [Verifica que START está desativado]



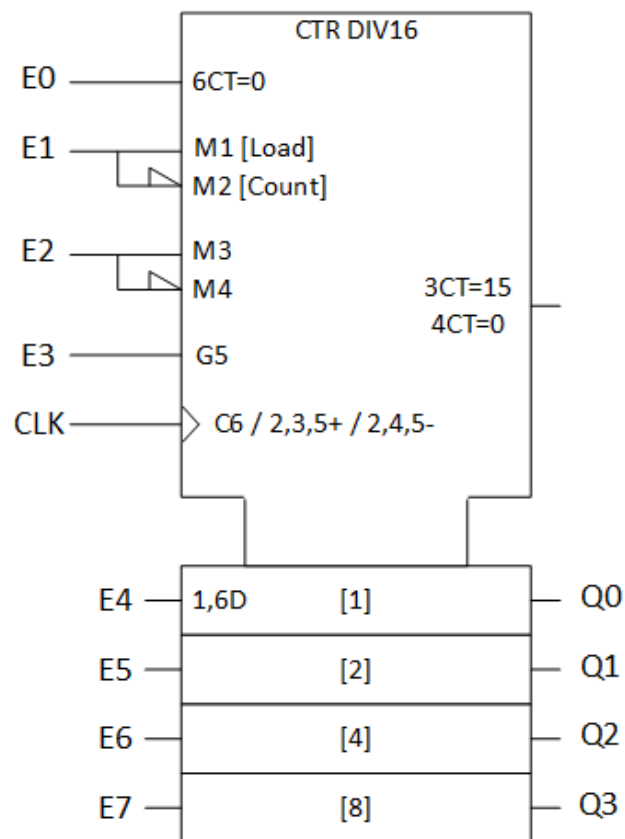
For each state, define the values of the inputs (in the diagram) and of the outputs (below) according to the following order:
 [Para cada estado, indique os valores das entradas (no diagrama) e das saídas (em baixo) de acordo com a seguinte ordem]:

- Order of the inputs [*Ordem das entradas*]: START, DOOR, HTIME, TIMEOUT.
- Order of the outputs [*Ordem das saídas*]: HEAT, TIMER_ACT.

- A: _____
- B: _____
- C: _____
- D: _____
- E: _____

Pergunta B:

$Q_3^n Q_2^n Q_1^n Q_0^n$	A	E0	E1	E2	E3	E4	E5	E6	E7	$Q_3^{n+1} Q_2^{n+1} Q_1^{n+1} Q_0^{n+1}$	Operation
0000	0	0								1111	
0000	1	0								0100	
0001	0	0								0010	
0001	1	0								0011	
0100	0	1								0000	
0100	1	0								0101	
1001	0	0								1010	
1001	1	0								0111	



Volume 2 - Part III (Cont.)