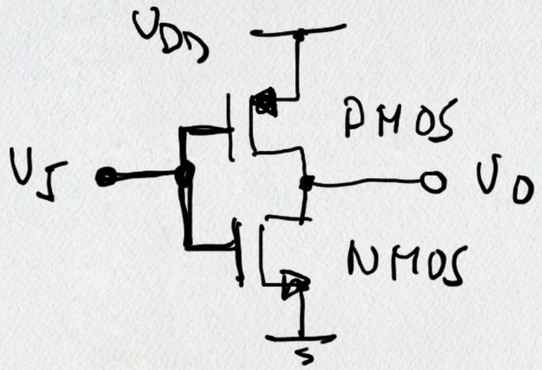
Problema 4

Considerando a mesma ~~família~~ lógica do inversor da Figura 3 ...

a) $Y = \overline{(X_1 + X_2) \cdot X_3}$

b) $Y = \overline{(X_1 \cdot X_2) + X_3}$

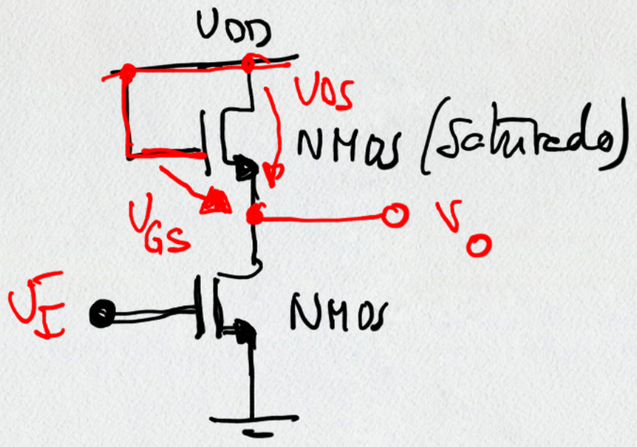


Inversor CMOS

Complementary MOS

NMOS+PMOS

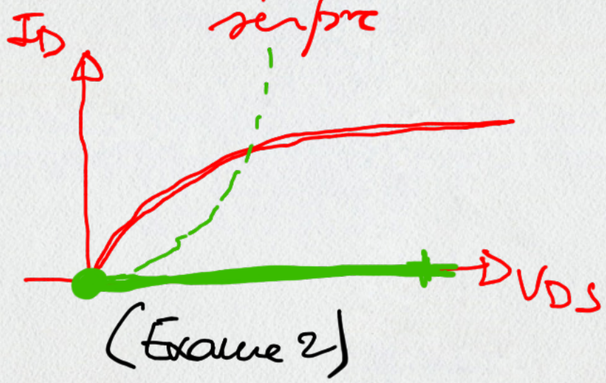
(Exame 1)



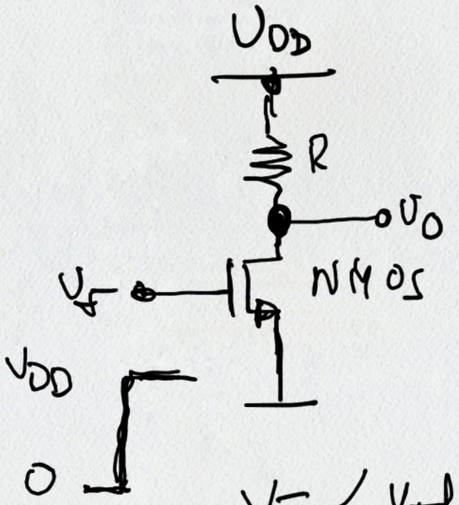
$V_{DS} = V_{GS}$

$V_{DS} \geq (V_{GS} - V_{th})$

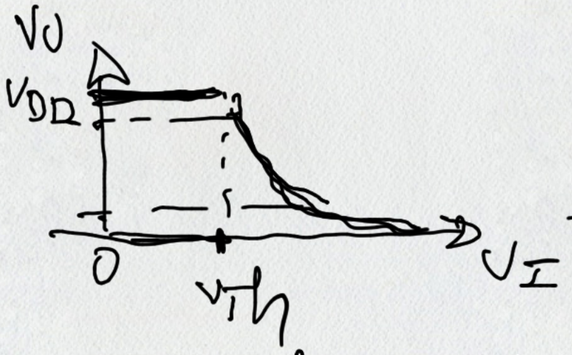
verifica-se sempre



(Exame 2)



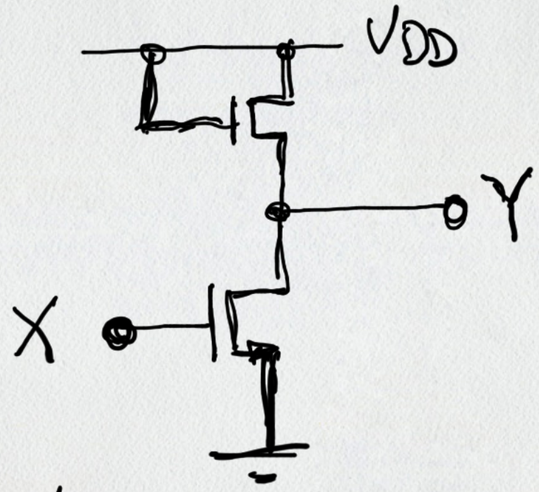
$V_I < V_{th}$



zonas de funcionamento

Inversor NMOS c/ carga Resistiva

Linear



$X = 0 \Rightarrow Y = 1$

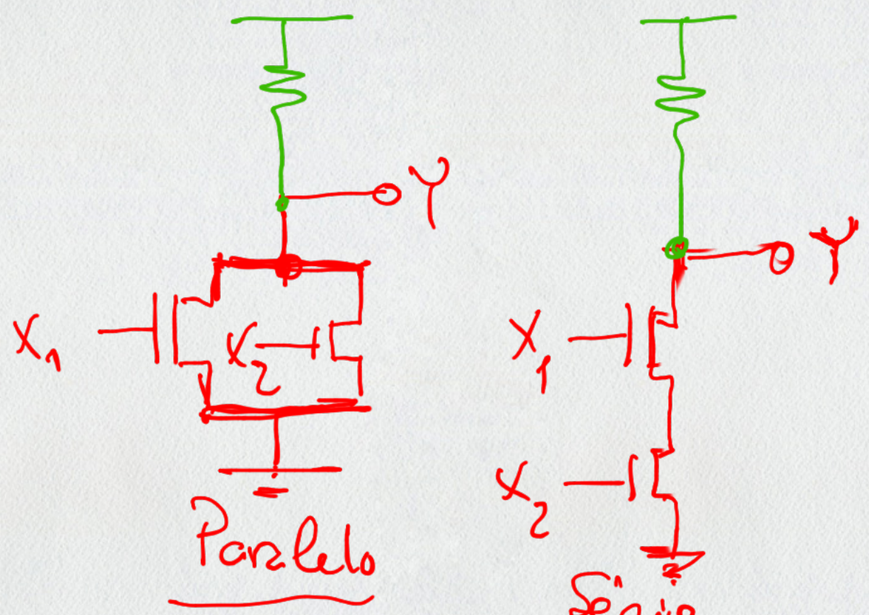
$X = 1 \Rightarrow Y = 0$

"1" Lógico = V_{DD}

"0" Lógico = $\frac{1}{\div}$

a) $Y = \overline{(X_1 + X_2) \cdot X_3}$

X_1	X_2	X_3	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0



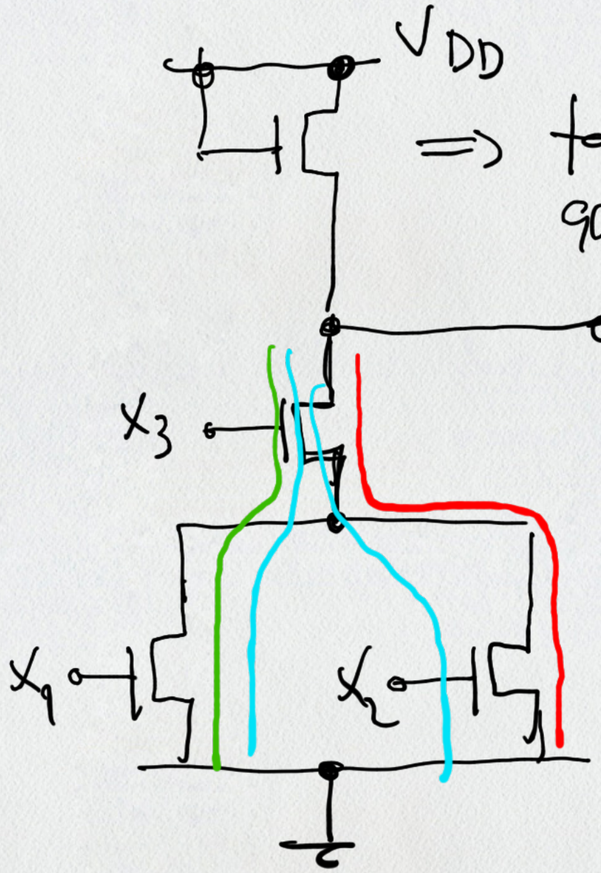
$Y=0 \Rightarrow X_1$ OU X_2 conduzir $\quad Y=0 \Rightarrow X_1$ E X_2 a conduzir

$X_1=1$ OU $X_2=1$ ou X_1 e $X_2=1$ $\quad X_1=1$ E $X_2=1$

X_1 E X_2 cortado $\quad Y=1 \Rightarrow X_1=0$ OU $X_2=0$ ou $X_1=0$ ou $X_2=0$

X_1 E X_2 - 0

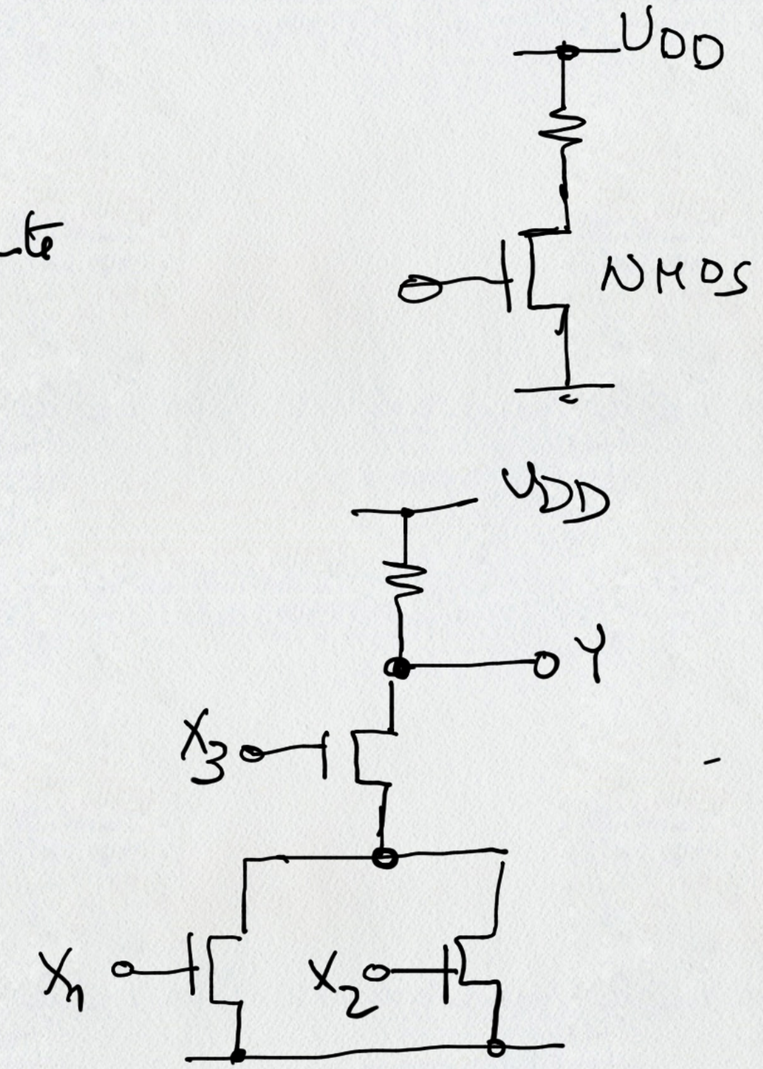
$$Y = (X_1 + X_2) \cdot X_3$$



$\Rightarrow$ fazer a ligação a V_{DD} qdo. não houver corrente no circuito de baixo

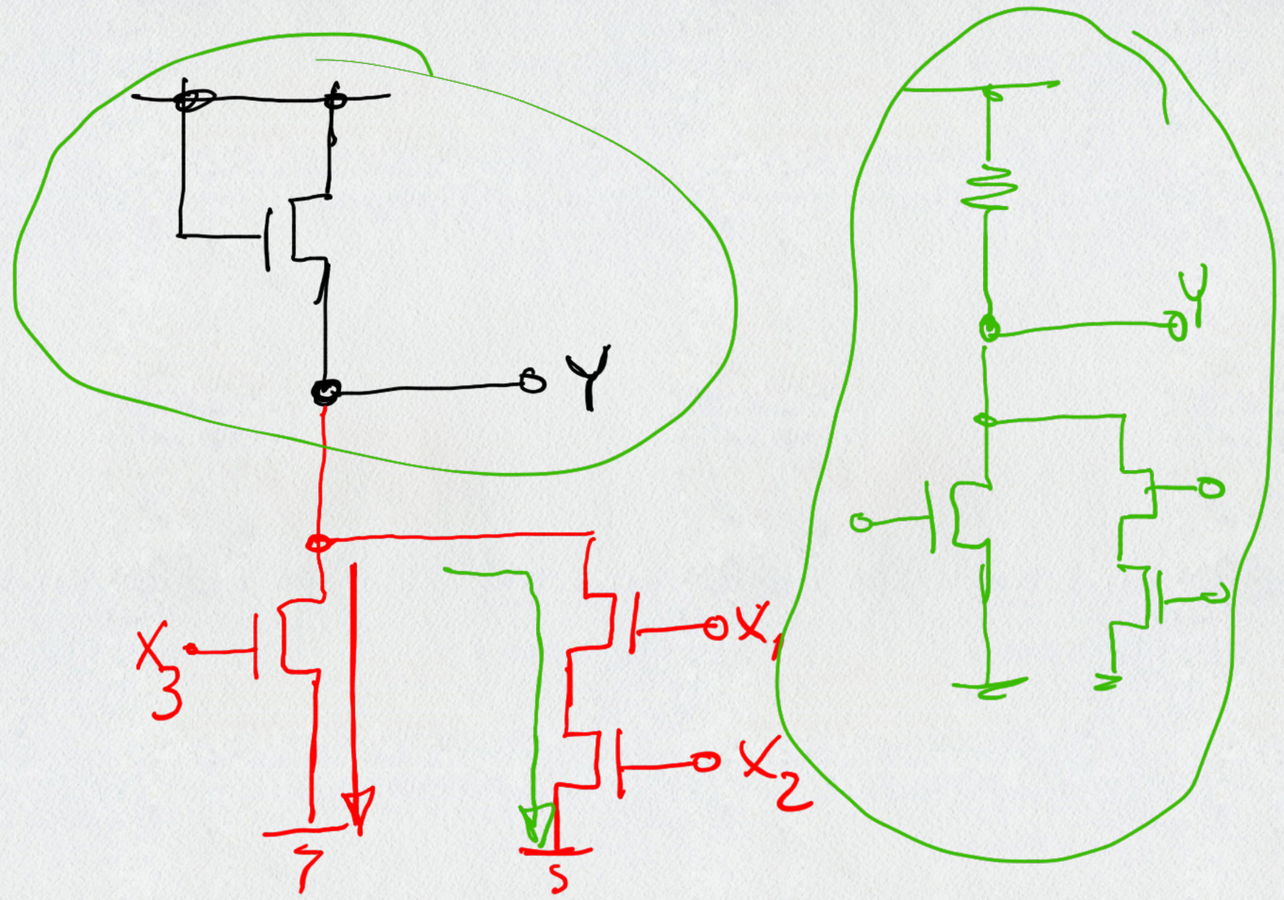
X_1	X_2	X_3	Y
0	0	0	
1	0	0	
0	1	0	
1	1	0	
1	0	1	
1	0	1	0
0	1	1	0
1	1	1	0

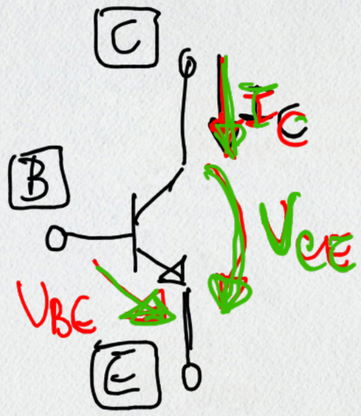
$$Y = (X_1 + X_2) \cdot X_3$$

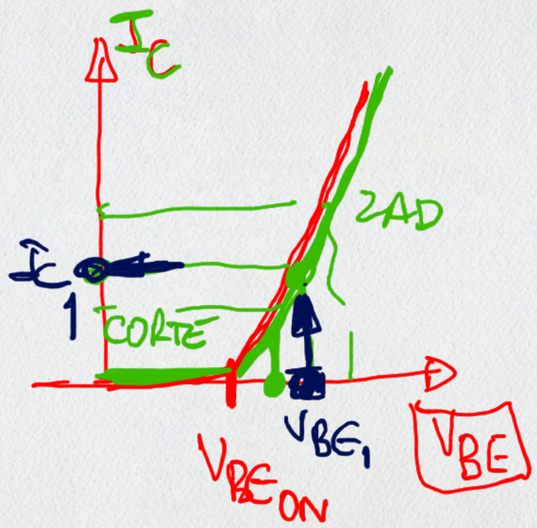


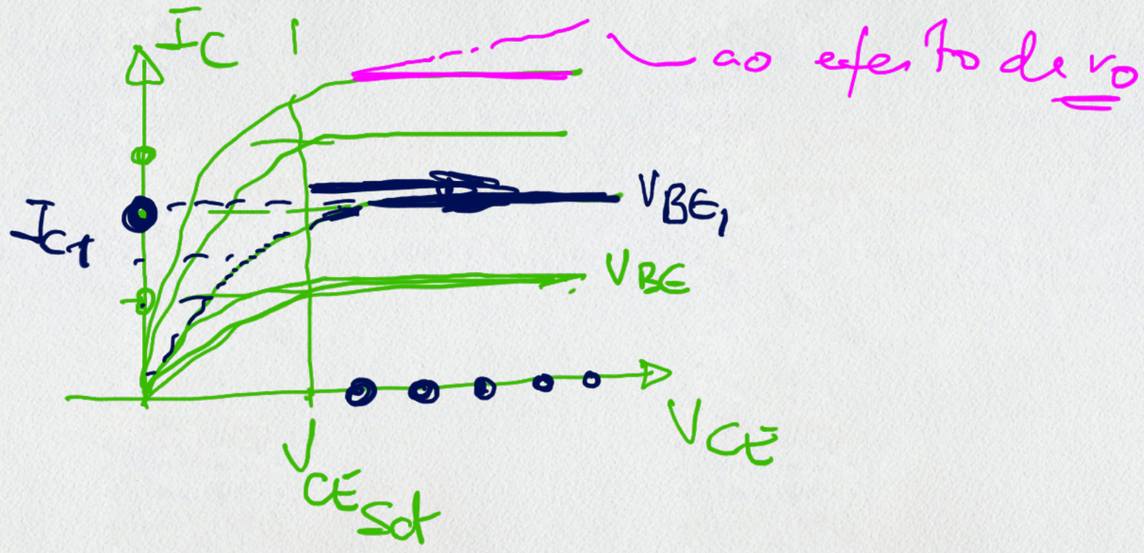
$$Y = \overline{(X_1 \cdot X_2) + (\bar{X}_3)}$$

X_1	X_2	X_3	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0



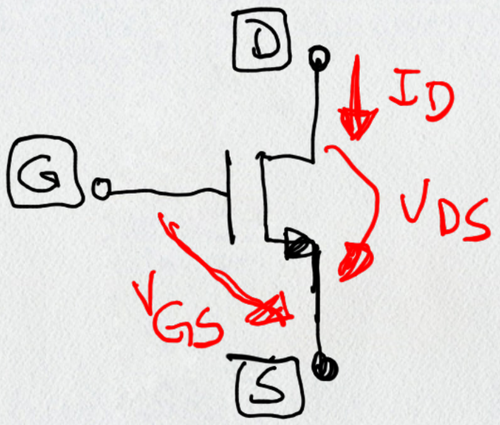


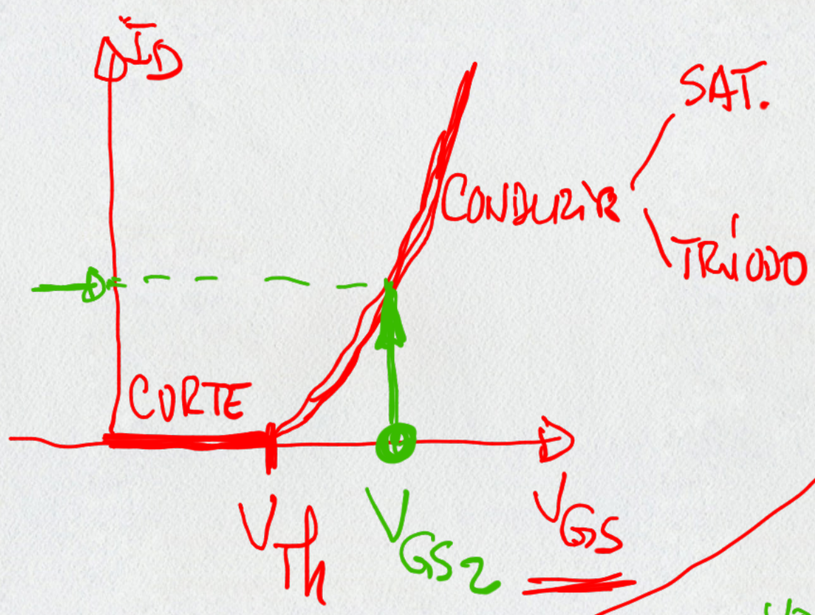


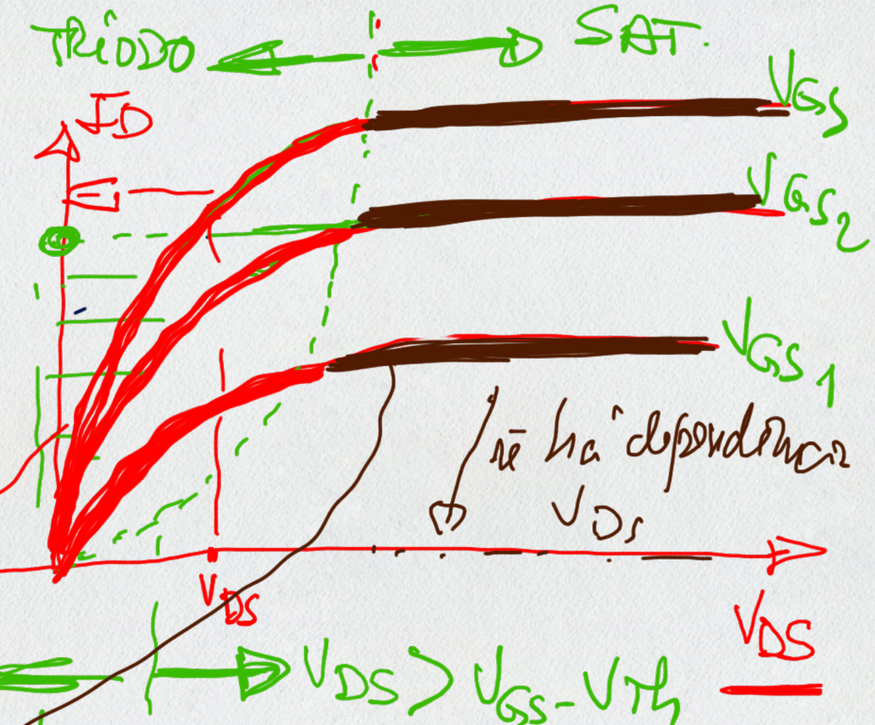


$> V_{CE_{sat}}$

FRONTEIRA







$V_{DS} < V_{GS} - V_{Th}$

$V_{DS} > V_{GS} - V_{Th}$

$V_{DS} = V_{GS} - V_{Th}$

$$I_D = k\left[2(V_{GS}-V_{Th})V_{DS} - V_{DS}^2\right]$$

$$I_D = k(V_{GS}-V_{Th})^2$$