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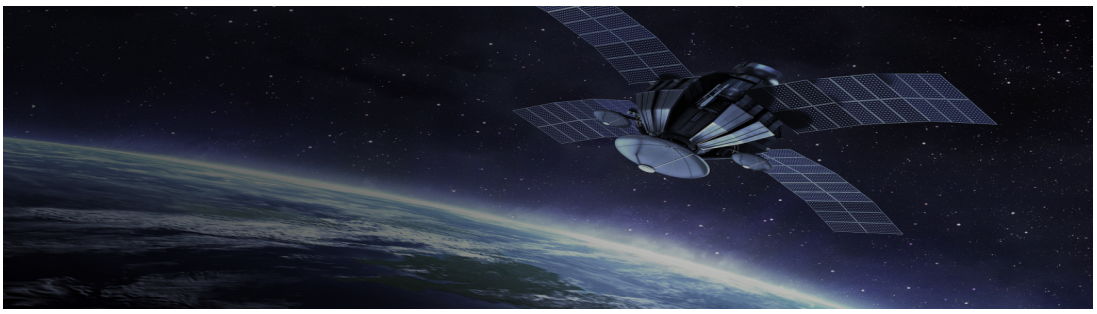

Radiation Hardened Comparator

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Thesis to obtain the Master of Science Degree in

Electrical and Computer Engineering

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November 2022

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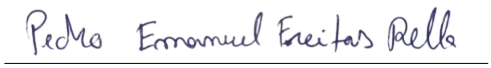

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Abstract

Comparators are an essential unit in many circuits, one of them being ADCs which are the electronic bridge between the real world and the digitized world. Adding to this fact, both low-power circuits and radiation hardened circuits are scientific areas with high and increasing interest.

Knowing the importance that a radiation hardened comparator has, especially prepared for low-power, in this work the objective is to implement a comparator with an offset cancellation technique capable of reducing its natural offset aggravated by radiation, during all its life cycle.

To do the proposed, some alternatives of comparator and calibration circuits were analyzed. The chosen comparator topology was the StrongARM Latch to which a calibration scheme that works through charge transfer was added.

Recurring to a Monte-Carlo Simulation with 5σ that accounts for fabrication (3σ) and radiation deviations (2σ), the circuit response was tested for both a comparator with 1.2 V of supply voltage working at 1.3 GHz and for a comparator working with 0.6 V of supply voltage at a speed of 20 MHz. The offset was significantly reduced in both cases, in most tests being able to turn an unusable comparator into a comparator with less than 0.1 mV of offset.

The offset calibration significantly reduces the offset that is natural and imposed to the circuit, providing a very good solution for circuits subject to radiation.

Keywords:

Comparator, Low-power, StrongARM Latch, Radiation-Hardened, Offset Cancellation, CMOS

Resumo

Comparadores são uma unidade essencial em muitos circuitos, sendo um deles os ADCs que são a ponte eletrónica entre o mundo real e o mundo digital. Adicionando a isto, ambos os circuitos de baixo consumo e circuitos fortalecidos contra a radiação são áreas científicas de grande e crescente interesse.

Sabendo a importância que o fortalecimento contra a radiação tem, especialmente para circuitos de baixo consumo, neste trabalho o objetivo é implementar um comparador com uma técnica de cancelamento da tensão de desvio capaz de reduzir o desvio natural agravado pela radiação, durante o ciclo de funcionamento do circuito.

Para realizar o proposto, algumas alternativas de comparador e circuito de calibração foram analisadas. A topologia de comparador escolhida foi StrongARM Latch à qual se adicionou um esquema de calibração que funciona através da transferência de carga.

Recorrendo a simulações de Monte Carlo com desvios de 5σ que têm em conta desvios de fabrico (3σ) e radiação (2σ), a resposta do circuito foi testada, tanto para um comparador com uma tensão de alimentação de 1.2 V a funcionar a 1.3 GHz como para um comparador com uma tensão de alimentação de 0.6 V a funcionar a 20 MHz. A tensão de desvio foi reduzida significativamente em ambos os casos, sendo possível na maioria dos testes tornar um comparador inoperacional num comparador com menos de 0.1 mV de tensão de desvio.

A calibração da tensão de desvio reduz significativamente o desvio natural e o imposto ao circuito, fornecendo uma muito boa solução para circuitos expostos a radiação.

Palavras-chave:

Comparador, Baixo Consumo, StrongARM Latch, Fortalecido Contra a Radiação, Cancelamento da Tensão de Desvio, CMOS

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List of Abbreviations

ADC - Analog-to-Digital Converter

CML - Current-Mode-Logic

DAC - Digital-to-Analog Converter

DR - Dose Rate

FOM - Figure-of-Merit

IC - Integrated Circuit

ICMR - Input Common Mode Range

IoT - Internet of Things

ISF - Input Sensitivity Function

LDD - Lightly Doped Drain

LSB - Least Significant Bit

LTV - Linear Time Varying

MC - Monte Carlo

MOSFET - Metal Oxide Semiconductor Field Effect Transistor

Opamp - Operational Amplifier

pdf - probability density function

RHBD - Radiation Hardened By Design

RHBP - Radiation Hardened By Process

RINCE - Radiation-Induced Narrow Channel Effects

RISCE - Radiation-Induced Short Channel Effects

SA - Sense Amplifier

SEL - Single Event Latch-up

SET - Single Event Transient

SEU - single Event Upsets

SRAM - Static Rapid Access Memory

STI - Shallow Trench Isolation

TID - Total Ionizing Dose

Chapter 1

Introduction

1.1 Background

In the interest of studying a Radiation Hardened Comparator, the first thing take into account is that there are two apparently distinct but ultimately interconnect subjects that have a underlying importance. Being these, the comparator circuit itself and its behavior, and the radiation effect on circuits.

1.1.1 Comparator

Comparisons exist in many forms, from the animal instinct that compares power and ability to survive, conducted by the natural selection, to the definition of which physical quantity is greater or lower than the other, as Epicurus once wrote " *The universe is infinite. All that is limited, ultimately, is the extreme point, and an extreme point can be discerned by comparison with others*".

While some comparisons are performed at a subjective level, like power or influence comparisons, others operate at a objective level like measuring distances, forces or electrical quantities.

In fact, comparators, which are the electronic circuits that perform the comparison between two voltages, are widely used especially in circuits that measure and digitize analog signals, namely analog-to-digital converters (ADCs), relaxation oscillators, memory sense amplifiers (SAs) and data receivers.

Regarding electronic circuits, its importance cannot be overstated. At the present time, the micro-electronics industry is one of the most (if not the most) influential industry.

With the construction of the first bipolar transistor by John Bardeen, Walter Brattain, and William Shockley [1, 2] and, two decades later, the field-effect transistor [3] by Julius Edgar Lilienfeld, together with the idea of integrating and building electronic circuits on a single semiconductor device (integrated circuit, IC, proposed by Werner Jacobi- Siemens [4]), the semiconductors industry has grown exponentially.

As a matter of fact, in 1965, Gordon E. Moore published an article in a business publication called Electronics, where he predicted that number of components of integrated circuits would double every

year for a 10 year period after that date, revising it later in 1975, to about 2 years [5] (image 1.1).

This prediction has been almost correct to date. However, with higher construction cost, especially lithographic process making harder to reduce costs with the reduction of the area, the fact that for technologies smaller than 100 nm there is no significant reduction in the power consumption and adding the fact that device area is rapidly approaching the atom dimension, thus reaching the limit imposed by the laws of quantum physics, this exponential growth may be reaching its end.

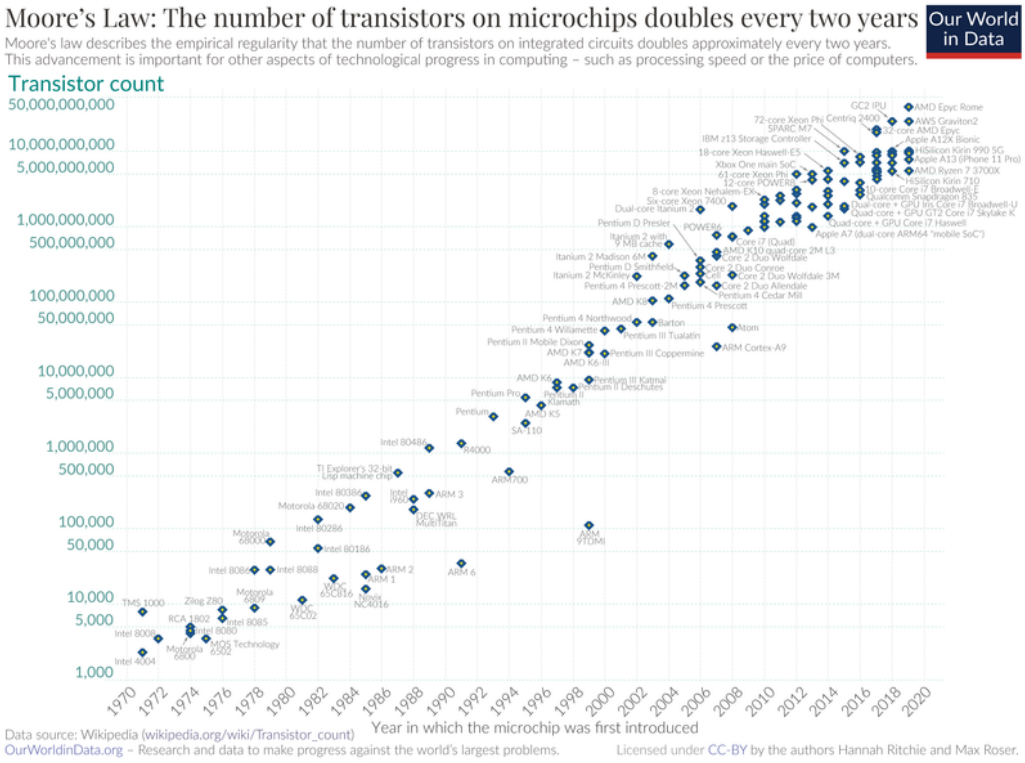

Figure 1.1: A semi-log plot of transistor counts for microprocessors against dates of introduction, nearly doubling every two years[6].

Taking into consideration the described evolution and conditions when designing circuits (reduced transistors dimensions and power supply voltages), and knowing that amplifiers are harder to design than comparators, this last circuit has gain an increased interest when designing ADCs.

The analysis of the importance of comparators cannot be done without briefly introducing ADCs, after all, these are one of their most common uses. Since every quantity in the world is analog, continuous in time and in amplitude, in order to process the world data with computers, which demand that the data is finite and so discrete in time and in amplitude, there is a great need for circuits which convert both an analog signal to a digital signal and a digital signal to analog one, being these the ADCs and DACs, respectively.

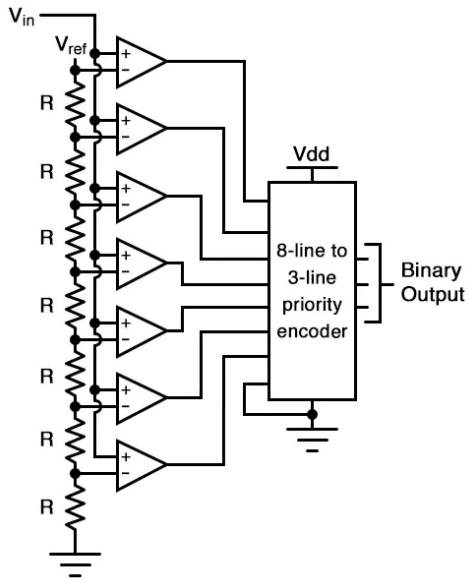

Figure 1.2: Flash ADC.

The performance of ADCs, hence of comparators as well (and for most circuits), is measured regarding the power required, the speed achieved and the resolution/quality of the result. Usually, depending on the requirements imposed by the application, some specifications can be inferred, and others should be maximized or minimized always regarding which is the best fit for the application.

Low power applications already have a great interest and have been gaining even more since portable devices, wireless communication, consumer electronics, medical equipment and topics such as edge-IoT demand low-power, high-speed circuits. ADCs with reduced transistor sizes, low-power dissipation and decreased propagation delay are essential for this kind of application with the comparator has a key element to satisfy these conditions.

Since comparators are decision-making circuits, their accuracy, which is commonly determined by its input-referred offset voltage, determines the resolution of high-performance ADCs. Furthermore, a faster and accurate comparator involves high gain and high bandwidth, therefore, latch comparators are used instead of static comparators, as they use positive feedback to drive the output nodes faster (higher gain).

CMOS dynamic latch comparators are widely used since they provide high-speed, low-power consumption, high-input impedance and full-swing output, benefiting from the positive feedback.

The StrongARM latch [22] was the first in the dynamic comparator class, and has been broadly used.

Other architectures have been developed and studied as the double-tail latch-type architecture [25] that provide a different solution from the StrongARM latch by separating the pre-amplifier stage from the latch, increasing the input common mode range and adding an extra degree of freedom by providing

separate tail transistors: one for the pre-amplifier and one for the latch stage.

To compare the performance of different comparators, a commonly used figure of merit (FOM) is presented in equation 1.1.

$$FOM = \frac{P_d}{2^n f_s} \tag{1.1}$$

where, P_d , is the power indulgence, n is the number of bits (resolution), and f_s is the sampling frequency of the comparator.

1.1.2 Radiation

Radiation discovery dates back to the end of the 17th century, when studies of Wilhelm Rontgen, Marie Curie and Henri Becquerel identify "*a new kind of invisible light*" which was "*clearly something new, something unrecorded...*" as the first of the three researchers wrote in [7].

Nowadays it is well known that radiation is hazardous, however, at that time this effects were unknown, hence there are multiple examples of health hazard caused by radiation. Examples like Marie Curie which died from problems caused due to exposure to ionizing sources [8] and some work-related objects still present signs of radiation. Or popular case of the "Radium Girls", workers whose job was painting watch dials with radium. After five of the workers sued the company (United States Radium), and thanks to the ensuing publicity, the health risks of radiation exposure were brought to the public attention [9].

Radiation affects not only human health, but also circuits normal operation. When subject to radiation, circuits deteriorate, changing permanently their characteristic. This degradation usually occurs due to the interaction between an impinging particle (proton, photon, heavy ion, electron, pion etc.) and the materials building the device. The type of damages is directly related to the energy of the particle and their relative ionizing proprieties (different radiation dose examples in figure 1.3).

Radiation damages can be divided into two categories: non-ionizing (e.g. displacement damages) or ionizing. The most relevant for this work is the ionizing damage, since it alters the circuit parameters without destroying it, more concretely the total integrated energy deposited by ionizing particles, called Total Ionizing Dose (TID).

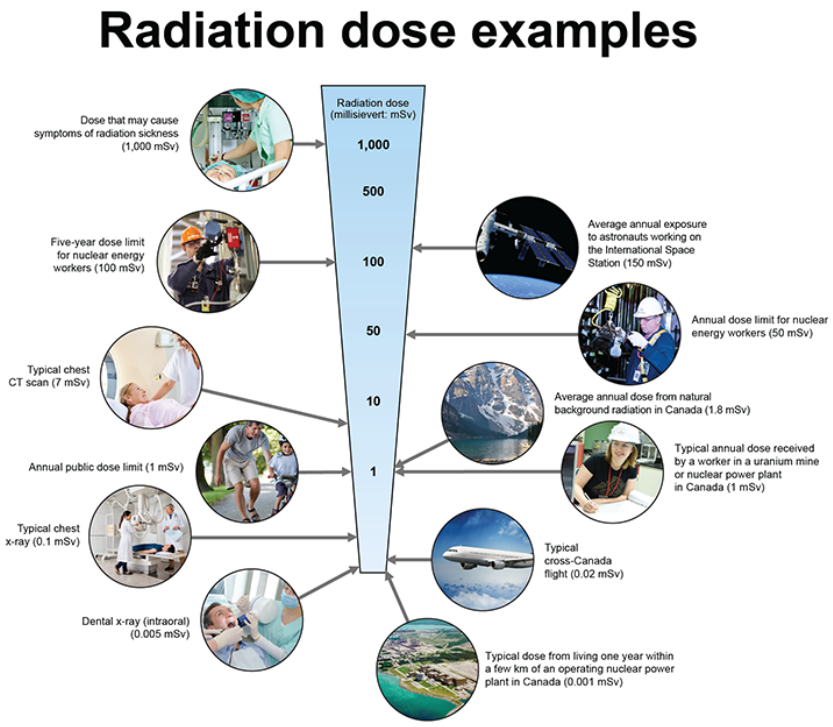

Figure 1.3: Radiation dose examples.

It is then clear that making integrated circuits resilient to radiation effects has a high importance. This circuits are used in areas such as space and nuclear applications, harsh domain electronics and the equipment used in high-energy physics measurement (medical equipment) that not just have high interest as high demands as well. In fact, these applications require that all circuits function precisely and continuously while being exposed to radiation. Taking the example of outer space, satellites are exposed to solar winds, cosmic rays and they orbit through Van Allen belts [10] (A deeper study on the effects of radiation on satellites in space applications can be found in [11]).

1.2 Problem description

Since a comparator circuit performs the comparison between two entries one important factor is that these are balanced, meaning that ideally there should not be a voltage difference between entries (with no voltage applied), and so for two slightly different voltages the result should not depend on the order in which they are connected. The Offset Voltage (V_{OS}) is defined as the differential voltage between inputs that must be applied to guarantee that for equal inputs the comparator is in the transition zone

(meaning that the inputs are balanced). As it is known real circuits do not have the ideal behavior and so the offset voltage is different from zero, playing an important role when designing a comparator (and many other circuits).

The main cause of the input offset voltage is the circuit mismatches that result of several random processes which occur during every fabrication phase of the devices. These mismatches include offset, gain and aperture mismatches which affect the circuit when pairing devices, and can be translated as different threshold voltages, V_t, current factors β ($=\mu C_{ox}\frac{W}{L}$) and parasitic capacitance for, ideally, equal MOS Transistors.

Moreover, when exposing a circuit to radiation, charges can get imprisoned in the MOS diffusions, altering the device characteristic. These changes can even be seen as aggravated mismatches, where quantities like threshold voltage, current factor and gain have a drastic change depending on the time being irradiated and the type of radiation.

Furthermore, with the supply voltage scaling in CMOS technologies and the increasing demand for low power consumption, as mentioned in the previous point, the signal power became significantly lower while random noises became worse, becoming a significant source of errors in comparators.

Naturally, with smaller voltage headroom for the signal and circuit, mismatches caused in fabrication and aggravated by radiation, increase comparator non-idealities as the offset voltage, having a serious impact.

1.3 Objectives

The objective of the thesis is to study clocked comparator topologies that performs self-calibration of their input offset voltage, studying their capability to react to deviations imposed by process mismatches and radiation effects. This calibration should guarantee a balanced comparison between entries during the circuit lifetime (since it also corrects aging deviations). Furthermore, this topology is very useful in ADCs because it allows to perform background calibration, correcting the deviations without interrupting the data flow.

Chapter 2

Comparator

2.1 Definition

Comparators are devices that compare two analog voltages, currents or charges and switch their output to indicate which one is larger, normally, through a logic level output. Following image 2.2, if V_p is greater than V_n, then the output V_o is a logic value '1', otherwise, with V_p lower than V_n the output is a logic value '0'. The case where the inputs are equal is usually avoided since this point represents the transition between logic levels. For this point, ideally, the gain of the comparator should be as close to infinite as possible but there are also other ways to deal with equality as introducing hysteresis or adding sub-circuits which detect equality.

In addition to the referred comparators that compare analog inputs, there are also the comparators which compare digital, binary values and are, generally, implemented in microprocessors. This type of comparator is out of the scope of this work.

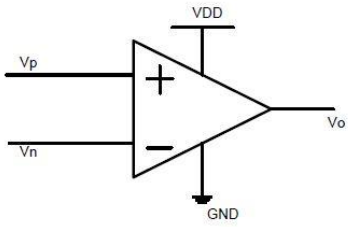

Figure 2.1: Comparator symbol.

Following the described, the ideal voltage function of a comparator is presented in figure 2.2 and equation 2.1.

Ideally, the transition zone corresponds only to the point where $V_p - V_n = 0$ and for every other difference between entries the result is a logic '0' if the referred difference is negative and a logic '1', otherwise.

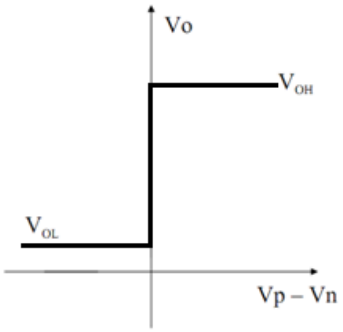

Figure 2.2: Voltage transfer function of the ideal comparator.

$$Vo = \begin{cases} 1 & V_p > V_n \\ 0 & V_p < V_n \end{cases} \tag{2.1}$$

Naturally in a real circuit this behavior cannot be obtained. Starting by the fact that it is not possible to achieve infinite slope and continuing with other non-idealities of the comparator response like offset voltage and noise, a response closer to what is achieved in real circuits is presented in figure 2.3.

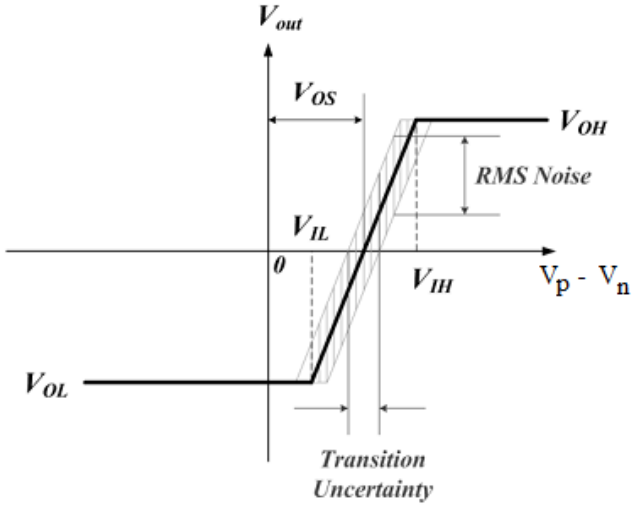

Figure 2.3: First order model of a comparator with input voltage and noise.

2.2 Characteristics

In order to analyze the comparator response, it's important to define the quantities that characterize it.

2.2.1 Gain

The gain is defined as in equation 2.2 and represents the capability of the comparator to react to smaller voltage difference between entries, ideally this quantity should be infinite which would mean that the transition would be only a point.

$$Gain = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \tag{2.2}$$

With ΔV = input voltage range.

2.2.2 Sensitivity

The sensitivity or minimal input resolution is the minimum input voltage (current or charge) difference that guarantees the proper functioning of the comparator.

Actually, noise interference prevent from a pure measuring of the sensitivity. If a noise, offset and hysteresis free comparator is considered, the sensitivity is defined by the minimal input voltage difference, at which the comparator in a distinct time still has a correct decision, that can be interpreted by following logic gates.

For a voltage input difference smaller than the sensitivity, metastability errors may. Additionally with the presence of noise, the comparator might give a valid but wrong decision.

As a example, for a simple ADC with N bits with 2^{N-1} comparators in parallel, every comparator needs to have a sensitivity of half of the LSB.

2.2.2.1 Metastability errors

Metastability errors occur when a comparator is not able to deliver a valid decision in a distinct time, smaller than the time slot for decision, given by the clock. Hence, the comparator remains in a metastable state during this time slot and a following logic gate cannot recognize a valid decision.

2.2.3 Input Common Mode Range (ICMR)

The input common mode range (ICMR) is defined as the range of input voltage for which the comparator has a normal operation and fulfils the required specifications.

2.2.4 Noise

There are different type of noise which affects circuits in general and can significantly change the behavior of the circuit if neglected. The influence of noise is well visible in images 2.3 and 2.4 as the uncertainty in the decision near the cross-over points of I_{NP} and I_{NN} (or V_P and V_N, respectively), where it causes random decisions.

When assuming that time constrains are enough to avoid metastability errors, the higher the difference between inputs, the lower is the chance of wrong decisions due to the influence of noise.

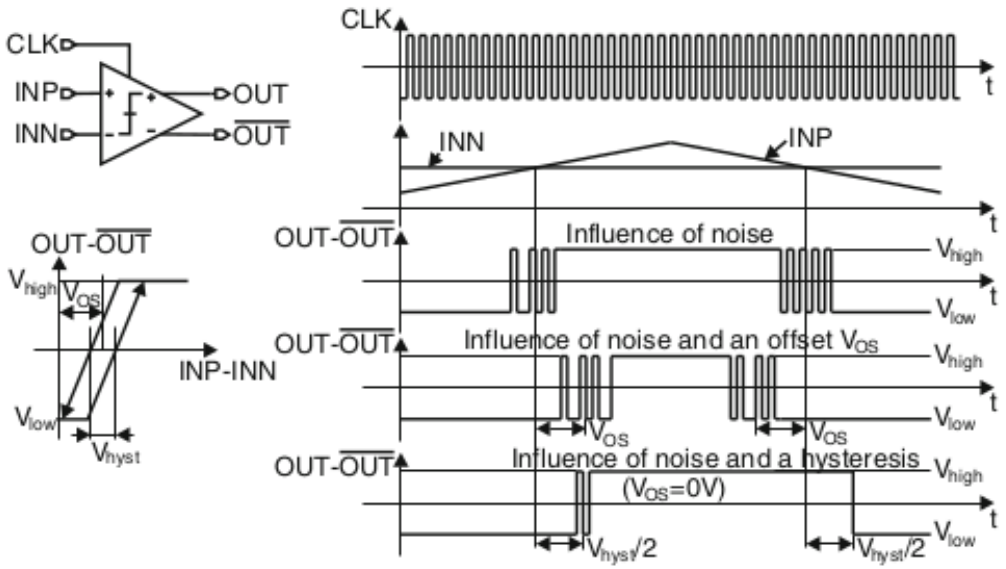

Figure 2.4: Offset and hysteresis of a comparator, which is affected by noise: It is assumed that noise dominates and no metastability error occurs.

Noise is described by a stationary random stochastic process, with probability density function (pdf) of the amplitude of the noise being mean free and Gaussian. There are many noise sources, which can be combined to an overall input referred noise source. The input signals may contain noise in amplitude or in time (jitter). Moreover, supply-voltage and ground-lines may also contain noise, mostly due to switching of neighboring circuit components. Lastly, CMOS devices also suffer from three sources of noise, being shot noise, thermal noise, and flicker noise.

2.2.4.1 Shot Noise

Shot noise is described as a random variation of a current, caused by fluctuation of charge carriers. The mean square $\overline{i_{sn}}$ is defined as in equation 2.3, where $e = 1.602\text{x}10^{-19}C$ is the elementary charge, I is the average current and Δf is the bandwidth.

$$\overline{i_{sn}^2} = 2eI\Delta f \tag{2.3}$$

2.2.4.2 Thermal Noise

Thermal noise occurs due to random thermal motion of electrons in a real resistor at absolute temperature θ. The equation 2.4 gives the mean square of the fluctuating voltage $\overline{v_{tn}}$ and of the equivalent current $\overline{i_{tn}}$. For a MOS transistor in saturation the approximation $R \approx \frac{3}{2gm}$ can be used.

$$\overline{v_{tn}^2} = \overline{i_{sn}^2}R = 4K\theta R\Delta f \tag{2.4}$$

2.2.4.3 Flicker Noise

Flicker (1/f) noise is caused by extra electron states at the boundary between Si and SiO_2, which trap and release electrons in a relatively fast rhythm. Hence, most of the noise energy is located at lower frequency. Equation 2.5 provides an approximation of the mean square of the gate referred noise voltage of a MOS transistor, where KF_F depends on the temperature and the fabrication process, C_{ox} is the gate capacitance per area and WL is the gate area.

$$\overline{v_{fn}^2} = \frac{KF_F}{C_{ox}WL}\frac{\Delta f}{f} \tag{2.5}$$

2.2.4.4 Kickback Noise

The comparator itself can produce noise when there is a fast transition either by the positive feedback in the decision phase, by pulling the nodes to predefined values in the reset phase or fast ramps of the clock. This type of noise is called kickback noise [15].

Generally, this type of noise can be neglected at comparator level, since it results in a common-mode disturbance at the inputs. There is also the fact that when the output nodes regenerate or reset, the comparator has already done most of the decision, hence, is immune to noise.

Even though generally this type of noise can be neglected, for a flash ADC for example where multiple comparators are applied in parallel, the interference between them can be sufficiently high becoming a

significant problem.

2.2.4.5 Static Noise

Static noise [16] is defined as the DC disturbance of the working point of a circuit caused by leakage currents. This noise can either be series-voltage noise, parallel-current noise, voltage noise at the ground or power supply lines and all of them combined.

The comparator can be affected by this type of noise. However, a decision from the comparator, normally, only lasts for half of a clock cycle and the clock period is small, hence the DC disturbance is not considered. In the opposite case of a SRAM (usually composed by latch circuits as some comparators) which holds a logic value for a significantly longer time, this type of noise can be very important.

2.2.5 Offset

The offset can be classified as systematic offset or as random offset. In comparators, the offset is, usually, generated by fabrication induced mismatches which can get even bigger due to the effect of radiation, as introduced in the first point of this work and as it's going to be deepened further on this work. Moreover, although with less impact, it can also be caused by gradients of temperature or stress introduced by neighboring circuits that influence the symmetry of the comparator. Furthermore, it can also be due to asymmetries in the circuit used, being this a case of systematic offset. And lastly, offset may also change for different clock frequencies (dynamic effects).

Also when analyzing offset, this can be input offset voltage, output offset voltage or input offset current. Input offset voltage is the voltage which must be applied between the two input terminals to balance the amplifier, meaning that the middle transition point is at $V_p - V_n = 0$, and it is the primary focus of this work (also represented in figures 2.3 and figure 2.4 as V_{OS}). Output offset voltage refers to the DC voltage present at the output of the comparator when both inputs are at ground. The input offset current is defined as the difference between the current flowing through each entry of a balanced comparator.

2.2.6 Hysteresis

Regarding hysteresis [17, 18], until now, it was assumed that there was only one transition region, even though it wasn't only a single point at $V_p - V_n = 0$, it was the same whether the voltage difference was increasing or decreasing. When hysteresis occurs the transition point for an increasing difference or for a decreasing one is different, as presented in image 2.4 with the voltage threshold represented by

V_{hyst}.

Sometimes this phenomena can be helpful, for example noise can make the output of a continuous comparator change, but it's normally unwanted, and with hysteresis this can be prevented. In the other hand, for ADCs, hysteresis might limit the performance because same voltage may create different digital codes depending on the input signal derivative.

In clocked regenerative comparator, a common cause of hysteresis are the reset switches if they are sized too small. In this situation, at the end of the reset phase, a considerable voltage difference still exists at the output nodes, which affects the next comparison phase establishing hysteresis.

2.2.7 Propagation delay

Propagation delay is defined as the delay between a change in the input and the response at the output, in other words, it is the time that the comparator takes to process the change at its inputs. In the case of a clocked regenerative comparator, it can also be described as the minimum time period from the beginning of the comparison phase (reset is released) until a valid logical value is available at the output. A graphical representation in figure 2.5.

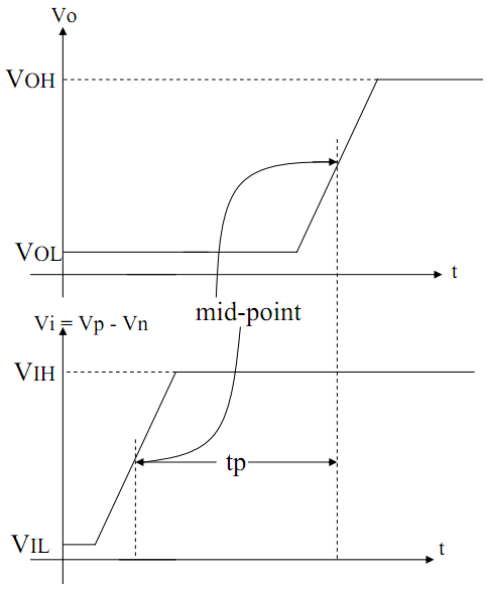

Figure 2.5: Propagation delay of a comparator.

2.2.7.1 Speed

The speed refers to how fast the circuit reacts and so comes naturally from the propagation delay as

expressed in equation 2.6.

$$Speed = \frac{1}{propagation\_delay} \tag{2.6}$$

2.2.7.2 Overdrive recovery Time

The overdrive recovery time [17] is the delay time that characterize a change from a large value at the input (where the gain of the comparator is saturated) to a small value of the opposite sign. Typically, this quantity is longer than the propagation delay time.

2.2.8 Slew Rate

The Slew Rate is defined as the change of voltage, current or any other electrical quantity per unit of time (equation 2.7), usually expressed in terms of microseconds(μs) or nanoseconds(ns). The specifications for a circuit may introduce a minimum or maximum limit for the slew rate of its inputs or outputs. For the outputs, it is normally given with the objective of guaranteeing that the speed of the output signal transition will be at least the given minimum, or at most the given maximum. As for the inputs, the objective is to indicate that the external driving circuitry needs to meet those limits to guarantee the correct operation of the receiving device. If either one of those limits, it's not met either for the input or for the output the correct functioning cannot be guaranteed.

$$SR = max|\frac{dv_{out}(t)}{dt}| \tag{2.7}$$

where $v_{out}(t)$ is the output produced by the amplifier as a function of time t.

2.2.9 Power Consumption

Power consumption is a very important factor in circuit design, especially in clocked regenerative comparators, which are highly focused on working for low-power applications.

Normally, a circuit have static power consumption and dynamic power consumption, which depend on the clock frequency and the capacitances of the circuit.

As briefly introduced at the beginning of this work, this quantity is an important factor in the FOM that distinguish comparators and their capabilities (equation 1.1).

2.3 Consequences of Device Properties on Circuit Design

Transistors are the fundamental unit in all circuits and their properties highly affect the response of any circuit.

2.3.1 Transistor Speed and Gain

One of the most significant effects of technology scaling both in digital, analog or mixed-signals circuits is the increase in speed and in the packing density. With gate length scaling, there is an increase in the gate resistance and a decrease in the parasitic capacitances. Furthermore, there is also an increase in the transistor transit frequency and in the maximum oscillation frequency.

The transistor speed and its intrinsic gain are directly related, being in direct competition, since high-speed transistors lead to low output resistance and consequently to a low intrinsic gain.

Although both can be improved by increasing the V_t or decreasing V_{GS}, operating in moderate inversion, this implies a drop in the transistor transit frequency and in the oscillation frequency.

2.3.2 Low-Frequency Noise

Flicker noise, as described in section 2.2.4.3, is caused by fluctuation of the total number of carriers and the fluctuation of mobility in the transistor channel. With the decreasing of the gate dimensions in CMOS technologies, this type of noise is reaching greater scales.

2.3.3 Matching

Matching is fundamental in analog and mixed signals, especially in differential structures. Normally, it is mainly dependent on the manufacturing process, but, as in the case of this work, also dependent on radiation effects. Since this is especially important to this work, a section will be dedicated to explain this phenomena.

2.3.4 Gate Leakage Current

The gate leakage current is especially important regarding the static power consumption. In CMOS nanometer technology, this quantity cannot be neglected neither in digital circuits, nor in analog circuits. The gate leakage current depends on the gate area, the oxide thickness, the gate-source voltage V_{GS}, and the gate-drain voltage V_{DS}. The gate leakage current affects the input bias currents, the gate leakage mismatch and the shot noise due to the gate current.

2.3.5 Linearity

With CMOS technology scaling, there is a reduction on the supply voltage and consequently in voltage headroom which worsens the linearity. Moreover, distortions in analog circuits are generally caused by the increased influence of series resistance and velocity saturation.

2.4 Matching

In an integrated circuit (IC), there are two variations to be considered, them being global and local variations. While global variations reflect the total variation of a component over a wafer or a batch, local variations, or mismatch, account for the variation in a component value comparing to an adjacent one within the same chip.

Mismatch is the process that causes time-independent random variations in physical quantities of identically design devices. It is especially important in analog-mixed systems as normally these are designed based on component ratios instead of their absolute value, but it can also be important in some digital circuits. With the reducing of device dimensions and used voltage supplies these random variations have a high importance in circuit design.

Starting by the MOS transistor equation that relate the drain current with the voltage in triode region given by

$$I_D = \beta[(V_{GS} - V_t)V_{DS} - \frac{(V_{DS})^2}{2}] \tag{2.8}$$

And the MOS transistor equation that relate the drain current with the voltage in saturation region, given by

$$I_D = \frac{\beta}{2}(V_{GS} - V_t)^2 \tag{2.9}$$

with

$$\beta = \mu C_{OX}\frac{W}{L} \tag{2.10}$$

Where I_D is the drain current, μ is the electron mobility, C_{OX} is the oxide capacity, W is the width of the MOS transistor, L is the length of the MOS transistor, V_t is the threshold voltage, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage.

In CMOS transistors, mismatches are categorized into threshold voltage mismatch, ΔV_t, and current factor mismatch, $\Delta\beta$. V_t mismatch is due to different charge quantities and the gate oxide capacitance per unit area. The variations in the dimensions, channel mobility, and gate oxide capacitance per unit area are measured as the mismatch in β. Since both V_t and β depend on the gate oxide capacitance per

unit area, the correlation between the mismatches in V_t and β may be an important measure. It can be seen in [20] and [21] that there is no significant correlation between the referred mismatches, meaning that V_t and β are almost independent. It is also known that at low V_{GS} the mismatch in the drain current is mainly due to the threshold voltage variation, and for bias levels approaching the mid-rail the conductance constant and the threshold voltage variations have similar influences.

The model that better approximates the MOS transistors mismatches are random variables with variance as described in equations 2.11 and 2.12.

$$\sigma_{vt}^2 \approx \frac{A_{vt}}{WL} + S_{vt}^2 D^2 \tag{2.11}$$

$$\frac{\sigma_\beta}{\beta} \approx \frac{A_\beta}{WL} + S_\beta^2 D^2 \tag{2.12}$$

Where the parameters A_{Vt} , A_β are area dependence coefficient of the technology used and their mean values are also provided in the datasheet, S_{Vt} and S_β are proportionality factors, WL the area of the gate of the device and D is the distance between the two devices.

However, the most used models for the MOS transistors mismatches are the simplified models described in equations 2.13 and 2.14.

$$var(\Delta V_t) = \sigma_{Vt}^2 = \frac{A_{Vt}^2}{WL} \tag{2.13}$$

$$var(\frac{\Delta\beta}{\beta}) = \sigma_\beta^2 = \frac{A_\beta^2}{WL} \tag{2.14}$$

2.5 Design

2.5.1 Continuous and Clocked Comparator

A continuous comparator is, as the name suggest, a comparator that at any time outputs a logic '0' or '1' depending on the applied inputs, and more importantly, changes its output as the inputs change, in a continuous way.

However, a continuous behavior may seem better, many applications only require the comparison in certain instants, such as ADCs and memories, for these the best solution is clocked comparators.

A clocked (or dynamic) comparator only functions on certain intervals of time, controlled by a clock signal, allowing for a higher accuracy and lower power consumption. These comparators are also called latched (or regenerative) comparators as they usually employ strong positive feedback through latch circuits for the "regeneration phase" when a clock is high, and have a "reset phase" when the clock is

low.

For comparators, it's important to have a short transition region. Clocked comparators have advantage at this point since they have reset phase and that way it is possible to employ stronger positive feedback. Adding this to the fact that most circuits don't require a continuous behavior and it becomes easy to understand why clocked comparators are, generally, the implementation choice.

Some examples of both of this type of comparator will be shown in the following points, based on the examples provided in [14].

2.5.2 Continuous comparators

When comparing the characteristics of an operational amplifier and the function implemented by a comparator, it can be seen that with a well balance difference input and a very high gain, these would be a way to implement a continuous comparator circuit. In fact, this is simplest way but only for application with low-performance requirements.

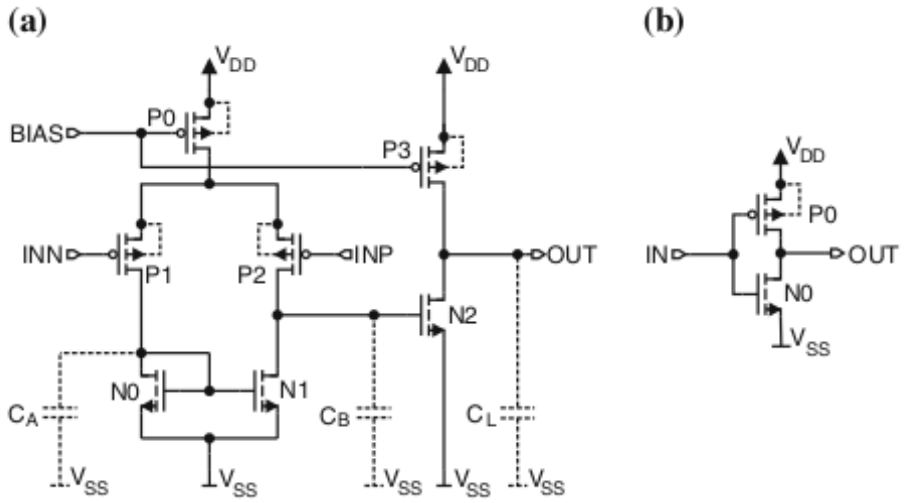

Figure 2.6: Continuous-time CMOS voltage comparators. **a** OpAmp comparator. **b** Simple inverter as comparator ([14]).

Opamps, as the example on figure 2.6a, are designed to operate in the linear mode with negative feedback (instead of open loop), hence, the recovery time from saturation zone is long. Furthermore, it is common in Opamp design to have a capacitor that imposes slew rate for high frequency signals, therefore, propagation delay for a comparator becomes even longer. There is also the problem of some Opamps having diodes between their inputs which in an amplifier helps entries follow each other but in comparators where the inputs are different can cause unexpected current through inputs. Lastly, a comparator is designed to easily interface with digital logic, which on the case of a Opamp must be

verified.

A simple inverter can also be used as a comparator[19], as presented in figure 2.6b. The transconductance and the output resistances of the transistors N0 and P0 define the amplification of the inverter and the minimal detectable voltage. The load capacitance of the output node joined with the parasitic capacitances of N0 and P0 define the speed of this topology. This circuit has the advantages of being composed by only two transistors, high switching speed and only dynamic current consumption. In contrast, has the disadvantages of suffering severely from mismatches, some changes imply layout modifications and, in most cases, high static current consumption.

Figure 2.7 shows an example continuous-time current comparators, where 2.7a is a current switch comparator that can be extended into the presented in 2.7b.

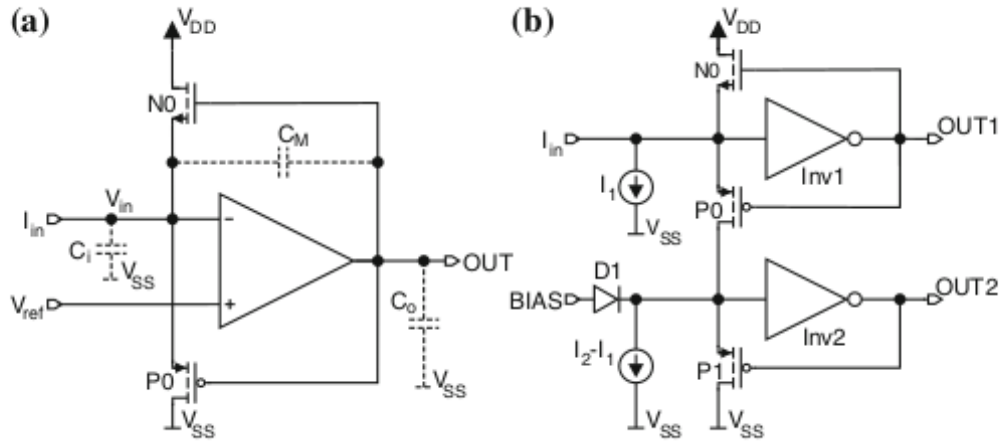

Figure 2.7: Continuous-time CMOS voltage comparators. **a** Current switch comparator. **b** Multilevel current comparator ([14]).

2.5.3 Clocked Comparators

As previously described, clocked comparators perform the comparison in well-defined timed slots, normally controlled by a clock signal. Although the fastest type of comparators use positive feedback as the one presented in 2.8b, the figure 2.8a is an example of a clock comparator where this is not employed. Figure 2.8c presents a charge comparator, which also has two n-MOS transistors N1 and N2 connected to positive feedback with the objective of measuring the charge.

Clocked, regenerative comparators are the most popular due to their fast switching and the inherent high gain with low power consumption, caused by positive feedback, and there are various implementations of this type of comparator.

Starting by the latched comparator present in figure 2.8b, this type of comparator employs the static complementary latch, which consists of two cross-coupled static inverters, to provide positive feedback.

The circuit present in figure 2.9 is obtained by adding a differential input amplifier pair (called the pre-amplifier stage added to the latch stage) that adds the advantage of having high-impedance in the input nodes (due to transistors N2 and N3) and lower propagation delay. The pre-amplifier achieves high speed with a wide bandwidth and small gain, this stage also decreases the effect of offset voltage and prevents kickback noise. On the other hand, the circuit presented, for example, does not produce a rail-to-rail output.

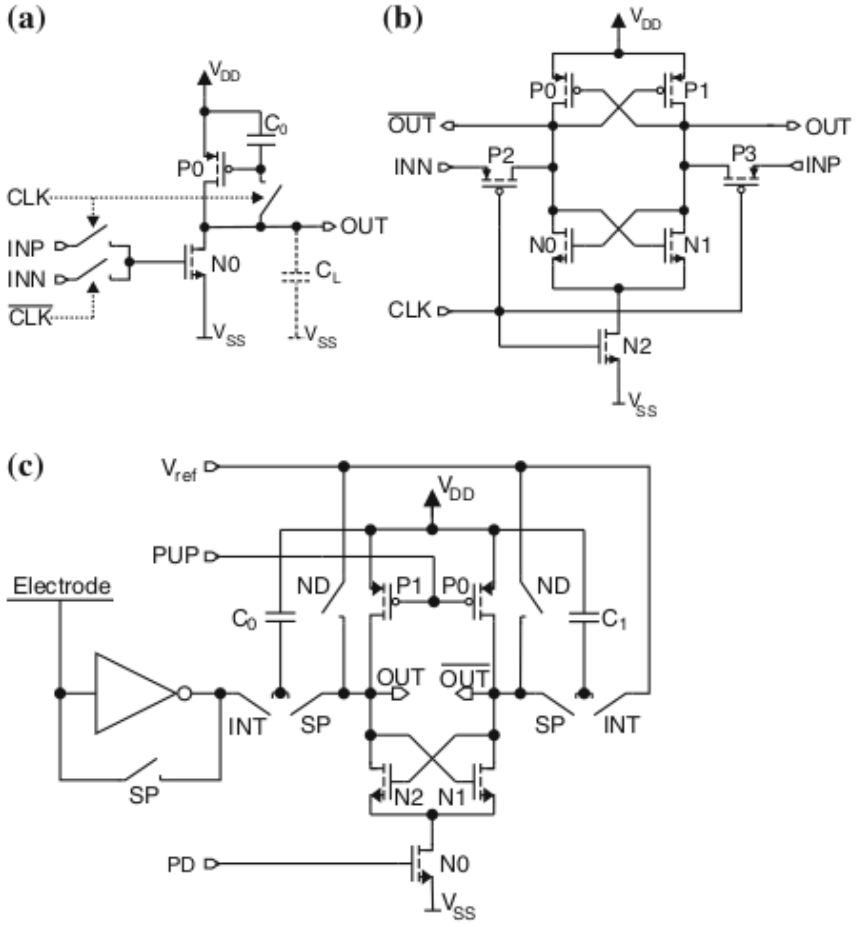

Figure 2.8: Clocked CMOS comparators. **a** Simple dynamic CMOS voltage comparator. **b** Dynamic CMOS latch. **c** CMOS charge comparator ([14]).

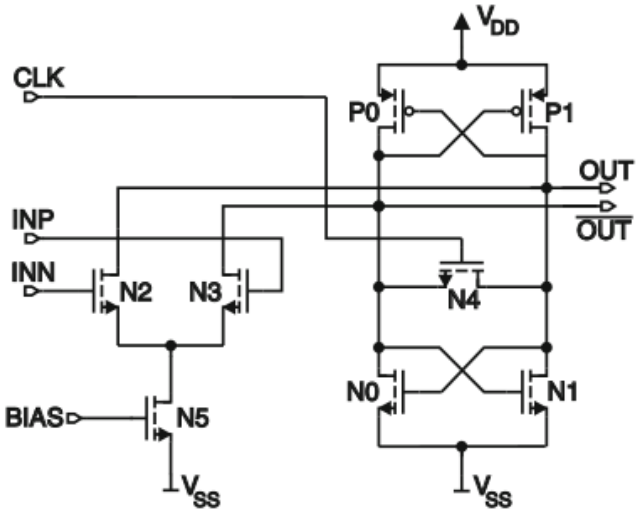

Figure 2.9: Clocked regenerative comparator using a static latch with input differential pair ([14]).

The comparator, shown in figure 2.10, uses the current difference generated by the input differential pair and then mirrored by transistors P0, P1, P2 and P3 to drive the final latch N0, N1. This topology has the advantage of having higher immunity to distortions caused by fast switching of the latch, because devices are coupled back via serial parasitic capacitances, and also the output resistance of the pre-amplifier is lower due to the diode connected loads. One disadvantage is that there is always current flow through P0 or P1, thus VSS can't be reached.

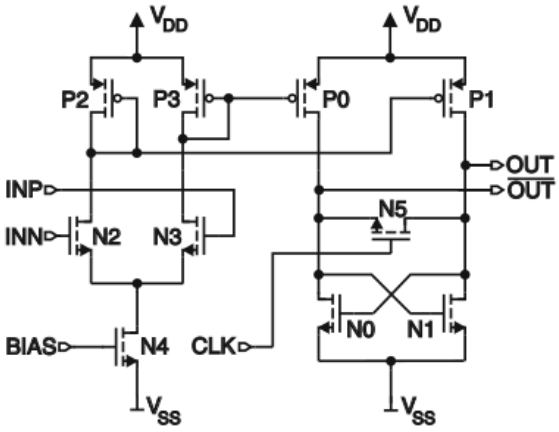

Figure 2.10: Clocked regenerative comparator with current mirrors ([14]).

A Current-Mode-Logic (CML), specifically a MOS-Current-Mode-Logic (MCML), latch is shown in figure 2.11 and can be also used as comparator. This circuit is in essence fast, because of its lower than rail-to-rail output voltage swing.

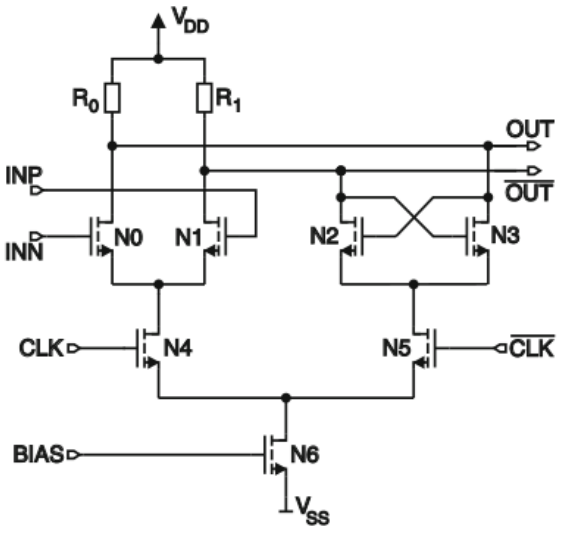

Figure 2.11: Clocked regenerative CML latched comparator ([14]).

Moreover, the implementation of the reset switches in a clocked comparator can be done in several ways.

One of this is to implement the reset switches such that it shorts both output nodes together to force a metastable working point. This has the disadvantage that this metastable point is middle between V_{DD} and VSS which, typically, doesn't represent a valid logical.

Other possibility is to pull both output nodes to V_{DD} or VSS, defining a valid logic value which can be treated accordingly. The disadvantage of this implementation choice is that an additional discharging or pre-charging of output nodes before the latch regenerates is necessary, which might take longer.

Lastly, there also the possibility of using two transistors in the input differential pair which implement the possibility to compare two voltage differences.

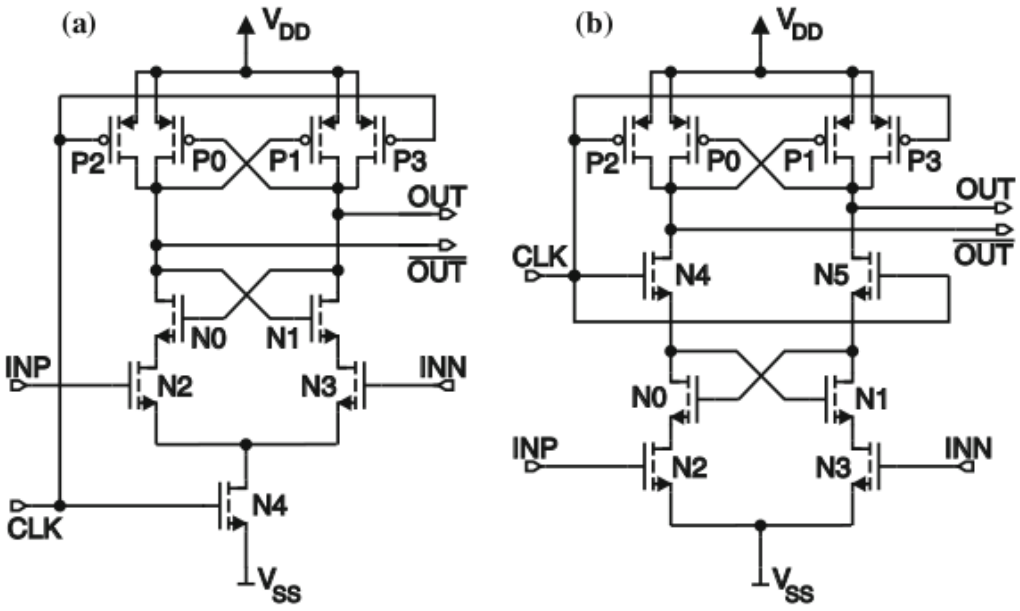

Figure 2.12: Clocked regenerative comparators. **a** Comparator with input transistor pair below the latch. **b** Comparator of (a) with changed arrangement of switches ([14]).

2.6 State-of-the-art

In literature, there are multiple studies of comparators. Normally, application oriented, the topology used, and design implemented naturally varies significantly depending on the application. Particularly [14] makes an excellent revision of the state of the art from a generic point of view. In this work, the focus will be in designing a comparator for a low-power ADC, hence the study will focus on two topologies that fit this application. Furthermore, many papers aim to reduce the offset voltage either in a static way or in a dynamic one which in the case of this work will be studied further on (a dynamic calibration scheme), and so the objective of this section will be the comparator itself.

2.6.1 StrongARM Latch

The StrongARM latch topology [22] is widely used as a comparator, even though it can also be used as a sense amplifier or a robust latch with high sensitivity. The name "StrongARM" was given to commemorate the Digital Equipment Corporation's StrongARM microprocessor [23], although the circuit was introduced by Toshiba's Kobayashi et al. [24].

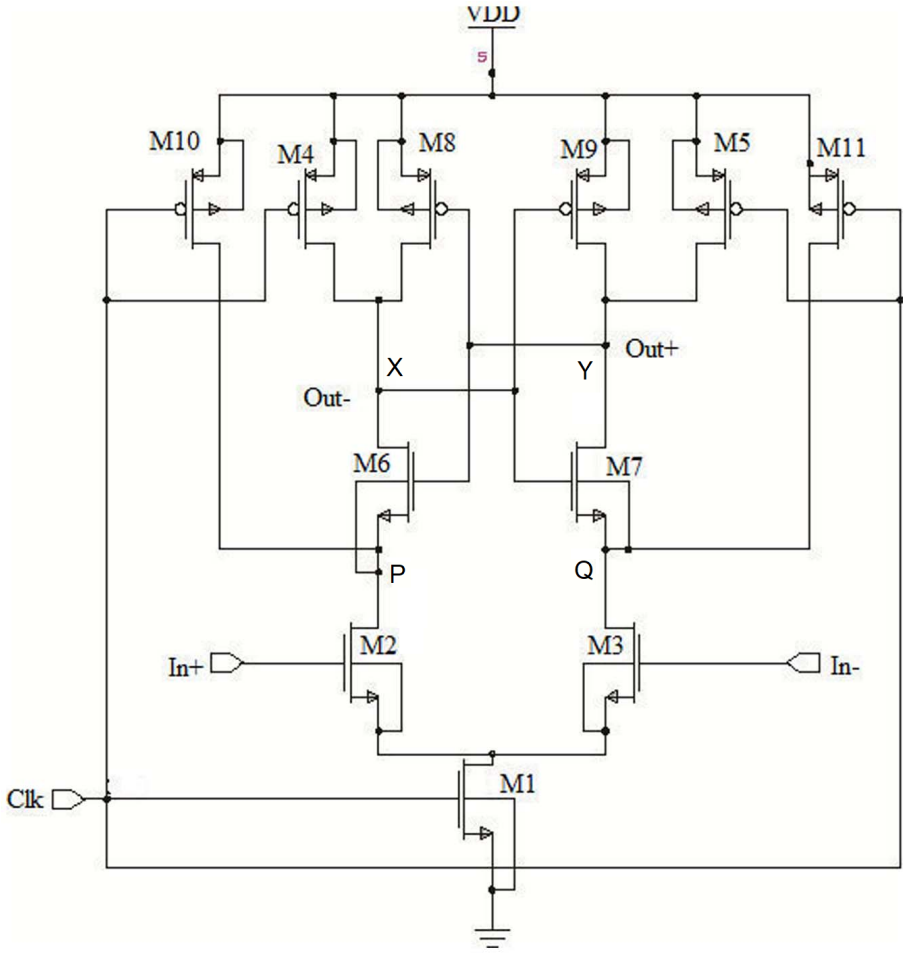

Figure 2.13: Conventional dynamic latch comparator[12].

This topology has become popular due to its high input impedance, the fact that its input-referred offset arises primarily from the input differential pair, it has zero static power, high-speed and full swing output.

The architecture of [24] present in figure 2.13 has only transistor M1 at the tail to control the current flow provided to the input differential pair M2 and M3, and that drives the two cross-coupled pairs, M6 – M7 and M8 - M9. The switches M4-M5, M10-M11 are responsible for the pre-charge of the circuit in the reset phase.

Following the analysis performed in [22], the operations of this circuit can be divided in four phases.

In the first phase (reset phase), CLK is low; M2-M3 are off; nodes P, Q, X and Y are precharged to V_{DD}.

In the second phase (beginning of the evaluation phase), CLK goes high, M4-M5 and M8-M9 (switches) turn off and M2-M3 turn on, drawing a differential current in proportion to V_{in+} - V_{in-}.

With the latches initially off, the nodes P and Q start charging, allowing V_P and V_Q to grow and possibly exceed V_{in+} - V_{in-}, hence, there is a voltage gain, reason why this phase can also be called amplification phase, lasting for approximately $(C_{P,Q}/I_{CM})$ V_{THN} seconds with the voltage gain of $Av \approx \frac{gm_{1,2}V_{THN}}{I_{CM}}$, where I_{CM} is the common-mode (CM) current. Since the tail current is approximately constant during this period, it can be written that $|V_P - V_Q| = (gm_{2,3}(V_{in+} - V_{in-})/C_{P,Q})t$, where $gm_{2,3}$ denotes the small-signal transconductance of M2 and M3, and $C_{P,Q} = C_P = C_Q$.

The third phase starts as V_P and V_Q fall to $V_{DD} - V_{THN}$, allowing the current to start charging nodes X and Y. This phase can be analyzed by summing the currents at the four nodes P,Q,X,Y as done in [22] from where the natural response can be described as in equation 2.15.

$$\tau_{reg} = \frac{C_{X,Y}}{gm_{6,7}(1 - C_{X,Y}/C_{P,Q})} \tag{2.15}$$

The fourth phase is reached when V_X and V_Y charge pass $V_{DD} - V_{THP}$, at which point M8-M9 turn on and the positive feedback brings one output node to V_{DD} and the other fall to zero.

2.6.1.1 Offset

As previously presented, the input offset voltage is one of the most important quantities in a comparator characteristics and it should be as small as possible.

Following the proceeding from [22], the precharge action of M4-M5 and M10-M11 keeps M6–M9 off initially, thereby reducing their offset contribution. Typically, the mismatches of M6-M7 are divided by the gain and those from M8-M9 by the square of the gain, thus the dominant factor for mismatches arises from the input differential pair. Writing the drain current of each transistor as the sum of a component proportional to $V_{in+} - V_{in-}$ and a CM component, I_{CM} (present in equations 2.16 and 2.17).

$$V_P = V_{DD} - \frac{gm_2(V_{in+} - V_{in-})}{2C_P}t - \frac{I_{CM}}{C_P}t \tag{2.16}$$

$$V_Q = V_{DD} - \frac{gm_3(V_{in+} - V_{in-})}{2C_Q}t - \frac{I_{CM}}{C_Q}t \tag{2.17}$$

Equation 2.18 can be obtained by combining equations 2.16 and 2.17.

$$V_P - V_Q = -\frac{gm_{2,3}}{2}\frac{C_P + C_Q}{C_P C_Q}(V_{in+} - V_{in-})t + \frac{C_P - C_Q}{C_P C_Q}I_{CM}t \tag{2.18}$$

During this step, $V_P - V_Q$ accumulates an offset equal to $(C_P - C_Q)/(C_P C_Q)I_{CM}t$, which can cancel the latch's random offset. The amplification mode ends when V_P and V_Q fall below $V_{DD} - V_{THN}$, and its

duration is given by $t.V_{THN}(C_P + C_Q)/(2I_{CM})$, where $(C_P + C_Q)/2$ is used as an approximation. The built-in offset is therefore equal to $V_{THN}(C_P/C_Q - C_Q/C_P)/2$.

2.6.1.2 Eletronic Noise

Following the noise analysis from [22], it is observed that most of the input-referred noise originates from the input differential pair (as with the offset) and from the thermal noise from the switches M10-M11 because all the other devices only turn on after a significant gain was already reached. In the amplification mode, the circuit behaves as an integrator, generating output noise from the noise of M1 and M2. The variance of this voltage grows with time as expressed in equation 2.19.

$$E(V_{PQ}^2) = \frac{8kT\gamma gm_{2,3}}{C_{P,Q}^2}t \tag{2.19}$$

Since the amplification mode lasts about $(C_{P,Q}/I_{CM})V_{THN}$ seconds, the final output noise variance due to M2 and M3 in this mode is presented in equation 2.20.

$$\sigma_{2,3}^2 = \frac{8kT\gamma}{C_{P,Q}}\frac{gm_{2,3}V_{THN}}{I_{CM}} \tag{2.20}$$

Adding the kT/C noise contributed by M10 and M11, dividing the result by the square of the voltage gain, and writing $gm_{2,3}.2I_{CM}/(V_{GS} - V_{THN})_{2,3}$, the total (integrated) input-referred noise observed in this mode is presented in equation 2.21.

$$\overline{V_{n,in}^2} = \frac{(V_{GS} - V_{THN})_{2,3}}{V_{THN}}[\frac{4kT\gamma}{C_{P,Q}} + \frac{(V_{GS} - V_{THN})_{2,3}}{V_{THN}}\frac{kT}{2C_{P,Q}}] \tag{2.21}$$

M1 and M2 are responsible for the noise represented by the first term within the square brackets and it is typically four to eight times greater than the second.

The simulation of noise in comparators is not trivial. Unlike small-signal analog circuits, a comparator does not directly provide an output noise and a gain by which the noise should be divided. For simpler topologies, the comparator can be placed in a metastable condition and a small-signal analysis can be performed, but the StrongARM latch completes switching actions and noise injections even before the output begins to change.

2.6.2 Double-tail Comparator

The double tail comparator is widely used in low voltage, low-power and high-speed applications. This topology works in a similar way as the StrongARM architecture described in the previous point with the main difference that the amplification and latch stage are separated, which enables it to employ low tail current in the former and high current in the latter leading to low power dissipation and high-speed, respectively, and does not require a voltage headroom as high as in the previously described architecture. However, increasing the speed and reducing power dissipation, also means that the offset and kickback noise are increased which are very important in comparators.

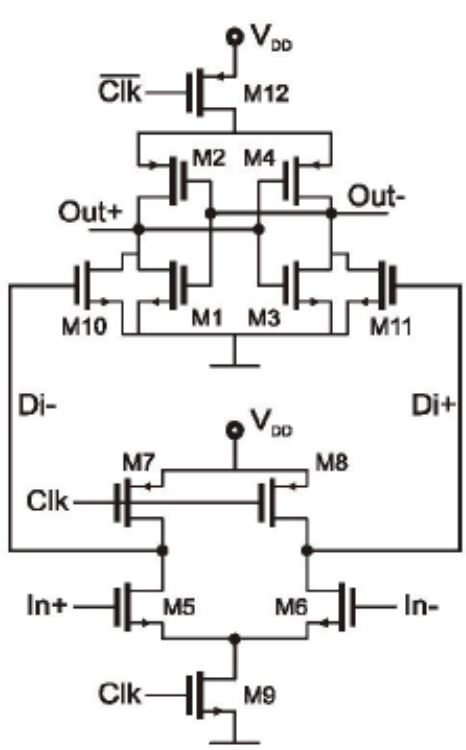

Figure 2.14: Double-tail latch-type voltage sense amplifier[25].

During the reset phase, transistors M7 and M8 pre-charge the Di nodes to V_{DD}, which makes M10 and M11 to discharge the output nodes to ground. When the amplification phase starts, the tail transistors M9 and M12 turn on, the common-mode voltage in the Di nodes drops and the input dependent differential voltage builds up. The intermediate stage formed by M10 and M11 passes the gain to the cross-coupled inverters and provides additional shielding between input and output, hence less kickback noise. Lastly, the inverters start to regenerate the voltage difference as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground.

In conclusion, the double-tail topology has an added degree of freedom that enables better optimization of the balance between speed, offset, power and common-mode voltage.

Chapter 3

Radiation

As formerly introduced, radiation highly affects all systems, including electronic circuits. It's clear that to a circuit that is under radiation effects has to be strengthened against these effects and its correct functioning has to guaranteed during the lifespan of the device.

It's important to start by realizing that the reducing of devices dimensions (shorter channel devices) allows for greater computational power in less area, but also improves radiation-hardness[27]. There are also negative aspects, since the quick scaling enhances the device-to-device variability, which is nowadays one of the crucial issues encountered in radiation qualification processes [28]. With fewer atoms, the absence of a single atom can produce significant changes in the threshold voltage of a MOSFET [30].

Furthermore, radiation assurance analysis are becoming even more expensive with the technology shrinking, since multiple test are required to obtain results with enough statistic confidence.

The work performed in [26] conducts an analysis on the effect of radiation in 65-nm technology node, more specifically submitting these devices to low dose-rates and measuring the produced deviations. The work developed in this thesis will use these results not just as a good approximation of some deviations induced by radiation but also as a upper bound, since the application and type of radiation studied in [26] represents an extreme case (low dose-rates cause a higher degradation when compared with high DR). The analysis in this chapter is based on the one performed in [26].

Note: The dose-rate (DR) is the dose absorbed per unit of time. For a constant DR, if this is integrated over the irradiation time, then the Total Ionizing Dose (TID) deposited is obtained.

3.1 Radiation and circuits

There are two significant radiation damaging effects on integrated circuits that can be categorized as cumulative effects, due to long time exposure, and single event effects (SEE), caused by a single particle.

Cumulative effects can be divided into displacement damage dose (DDD), generated by big particles (e.g. heavy ions, protons and neutrons), and total ionizing dose (TID) caused either by photons (X and Y rays), or by charged particles (e.g. protons or electrons). In TID, the particles create electron-hole

pairs in normally isolated layers, separated by an electric field, leading to unwanted charge build-up and insulator degradation. This effect leads to variations in transistors parameters, like variation on the threshold voltage (V_t), increase of parasitic currents and variation of the trans-conductance which has an extra high impact on analog circuits, since analog functions are highly affected by the transistors transconductance and output resistance.

Single event effect are usually due to the impact of an energetic heavy ion or proton, normally caused by cosmic solar particles, galactic cosmic rays and trapped protons in radiation belts. There are two categories of errors caused by SEE, them being soft-errors that can be solved during the device operation (Single Event Transient and Upsets, SET and SEU, respectively) and hard-errors that needs reconfiguration or a power-cycling (Single Event Latch-up, SEL). SEU can be a concern in digital circuits since the state of a bit can be flipped, while in analog circuits a transient pulse can be observed but quickly subsides (in data converters once they are mixed signals this can still be a problem). SEL can cause permanent-errors such as broken transistor both in analog and digital circuits (a detailed analysis on latch-up events on MOS is performed in [38]).

3.2 Total Ionizing Dose Induced Degradation

To understand the effect that radiation produces in devices, the first important factor is to understand how radiation and matter interact.

3.2.1 Interaction between Radiation and Matter

The interaction between matter and radiations depends on the mass, charge state and kinetic energy of the impinging particles, and on the atomic mass, atomic number and density of the material. Since MOS devices are mainly composed by silicon (Si) and silicon dioxide (SiO_2), the analysis will be performed to these materials.

There are three type of interactions between photons and target materials, these being photoeffect, compton effect and pair production effect, each of them produces energetic free electrons.

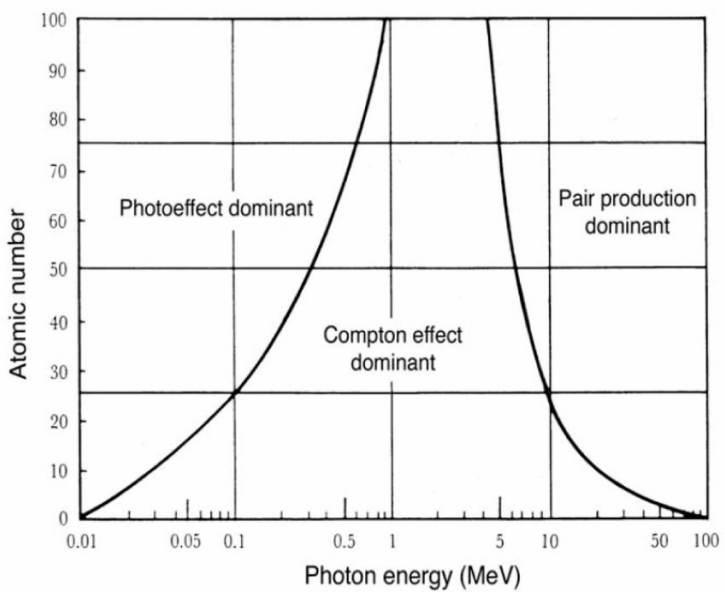

Figure 3.1: Importance of three photon interactions as a function of atomic number and photon energy. Solid lines correspond to equal cross sections for neighboring effects (taken from [26]).

For a relatively low atomic number the only effect caused by radiation is the photoeffect effect, since there is not enough photon energy for the other effects. The interaction between a photon and the insulating layer of the device generates an electron-hole (e-h) pair, a low-energy photon and sometimes an Auger electron (very low energy electrons that are emitted by radionuclides that decay by electron capture [29]). The freed photoelectron, passing through the material, deposit a portion of its energy as ionization, and the remaining as atomic lattice displacement. For charged particles, as electrons, most of the energy loss occurs through ionization.

3.2.2 Holes Transport And Oxide-Traps Formation

For MOSFET devices, ionizing radiation affect both the silicon bulk and the oxide. When these effects occur in parts of the device capable of retaining charges as the silicon dioxide, multiple interactions can affect and accumulate over time. Charge trapping in the oxide layers is as described below:

1. Ionizing radiation creates electron-hole pairs
2. Transport of holes via polaron hopping through localized states in SiO_2 bulk
3. Deep hole trapping in the SiO_2 bulk, and near Si/SiO_2 interface
4. Interface traps depassivation at the Si/SiO_2 interface

Moreover, the photoeletron can ionize other particles generating e-h pairs. Once generated, some of them are instantaneously recombined. In this process it's known that electrons are much more mobile than holes, fact that is even more evident as technology nodes get smaller, thus the radiation induced effects are attributed exclusively at the presence of holes.

3.2.3 Holes Transport in SiO2

After the impact of the radiation source, it takes only a few picoseconds before the charge generation and recombination are completed. After this phase, the fraction of holes that escaped recombination process are transported in SiO_2.

After some time, holes move toward the negative electrode, becoming trapped in the silicon substrate or captured in deep trapping sites. The hole transport is known to be anomalous in nature since it lasts over decades. The holes that don't move through the oxide cause a negative flatband voltage shift, and therefore a negative threshold voltage shift.

As the technology shrinks, the oxide thickness decreases and the shift decreases as well. This tendency as led to a reduced sensitivity of the gate oxide in modern technologies which prove able to bear with ultra-high level of total dose.

3.3 Total Ionizing Dose Effect on Modern CMOS Technologies

In recent CMOS technology, the gates are almost immune to ionizing process because of their reduced thickness. However, they are still strongly affected by TID damages, since thick auxiliary oxides, such as Shallow Trench Isolation [31] and spacers [32], are present and the charge trapped in these can lead to significant variations on MOSFETs.

The two dielectric structures are responsible for different types of damages.

First, STI oxides, used to isolate adjacent MOSFETs, are responsible for the generation of a radiation-induced drain to source leakage current path [33, 34] and the radiation-induced narrow channel effects (RINCE) [35].

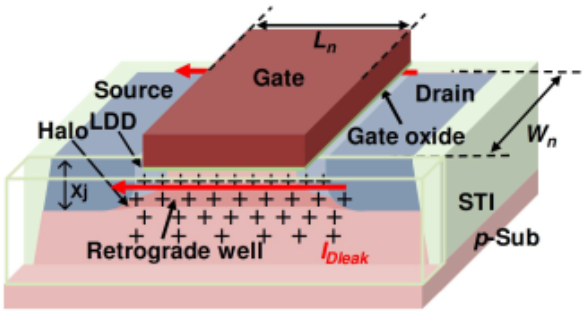

Figure 3.2: Parasitic path between source and drain, due to charge trapped in the STI.(taken from [26]).

Secondly, the spacers, located along the sides of the polysilicon gate to allow the implantation of Lightly Doped Drain (LDD) extensions [32], are responsible for the radiation-induced short channel effects (RISCE) [35]. Spacers have also a key role in the dose-rate effect.

3.3.1 Shallow Trench Isolation - Related Effects

3.3.1.1 Radiation-Induced Narrow Channel Effects

This effect is caused by the electric field generated by the positive charge trapped in STI region close to the interface which reduces the effective width of the channel, resulting in a reduced current output. This effect can be neglected for larger channels, since a smaller percentage of the channel is affected by the trapped charge.

3.3.1.2 Radiation-Induced Drain to Source Leakage Current

This effect as the name suggests is defined as the increase in leakage current provoked by radiation. Leakage current, defined as the current flowing from the drain to the source with the transistor off ($V_{GS} = V_{DS} = 0V$) is one of the most important problems caused by TID as it can significantly increase the static power consumption.

The positive charge that gets trapped in the STI attract a considerable amount of electrons from the silicon bulk, forming a conductive path between the source and the drain. PMOS devices have their carriers positively signed, same as the charges trapped in the oxide, and so are immune to this effect. If the gate bias is absent during irradiation, the device exposed to it doesn't present signs of increase in the leakage current, which means that with the imposition of the positive gate voltages, the positive charge trapped close to the STI-gate corner is repelled further in the STI structure.

3.3.2 Spacers-Related Effects

Spacers are located along sides of the polysilicon gate and are the heterogeneous insulator layers used in advanced CMOS technologies. These oxides allow the implantation of Lightly-Doped Drain(LDD) extensions.

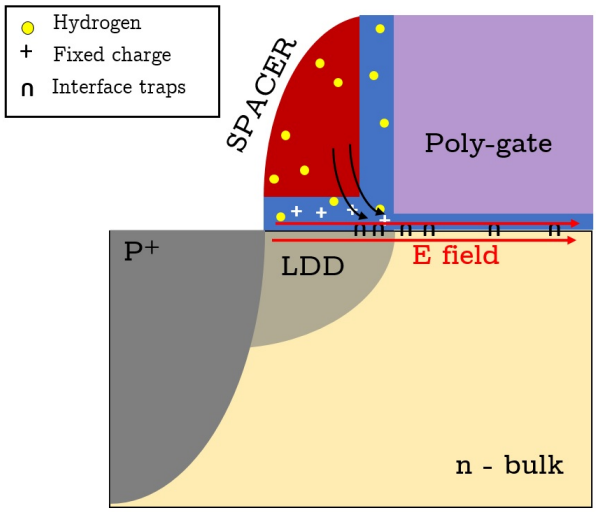

Figure 3.3: V_{DS} helps the drift of H^+ and promotes the depassivation of Si^-H bonds. The hydrogen ions are reported in yellow, while the positive fixed charge is represented by a + sign ([26]).

Note: The closest layer to the silicon interface is composed by SiO_2 and then a thick layer of Si_3N_4 surmount the silicon dioxide.

One of the spacers-related effects was reported in [35] is called Radiation-Induced Short Channel Effect, or RISCE, that characterizes the channel length dependence in the evolution of the drain current in irradiated devices.

There are multiple stages in the irradiation process in the presence of spacers.

Firstly, the holes generated by radiation get trapped in the bulk of the dielectrics and free H^+, which depassivate the interface traps located at the spacer/drain interface. The drain-to-source resistance, R_{SD} rises for pMOS since positive oxide- and interface-trapped charges repel holes in the LDD extensions, causing a rise in the series resistance, while, for nMOS, the net evolution of this parameter is determined by the balance between the positive charges trapped in the oxide and the negative interface traps.

Secondly, the presence of bias pushes the hydrogen ions into the gate oxide, where they depassivate the Si-H bonds and create interface traps. These interface traps located along the gate Si/SiO 2 interface and produce a significant threshold voltage shift.

3.4 Effect of radiation in 65 nm transistors

Since the technology that will be used is 65 nm MOS transistors, a detailed study of the radiation effect in transistors from this technology, especially for low dose-rates, is performed in [26], from where some interesting results are obtained.

In order to understand how significant this radiation effects can be in the variation of the transistor parameters, the figures 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10, and 3.11 were presented in [26].

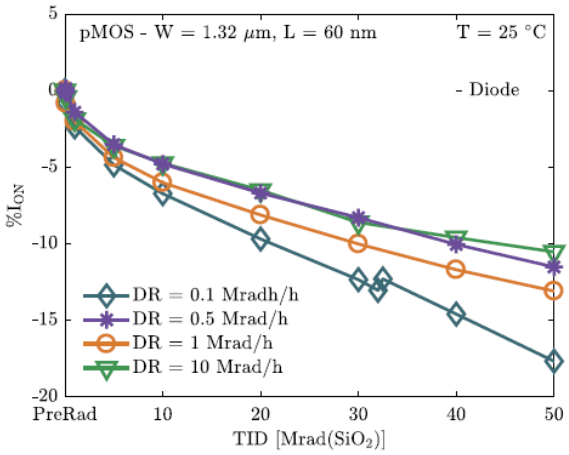

Figure 3.4: ON current percentage variations in function of TID for the W = 1.32 μm and L = 60 nm PMOS transistor, irradiated with different DRs(dose rates) up to 50 Mrad(SiO2) (taken from [26]).

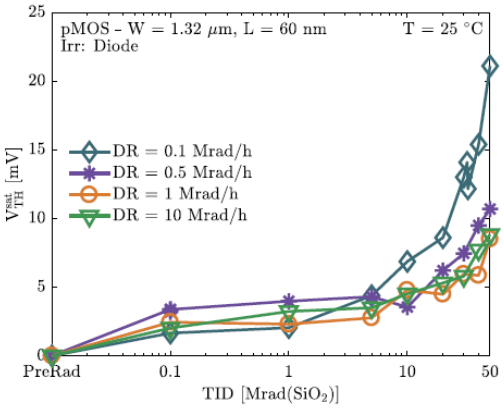

Figure 3.5: Threshold voltage variations for the W = 1.32 μm and L = 60 nm PMOS (taken from [26]).

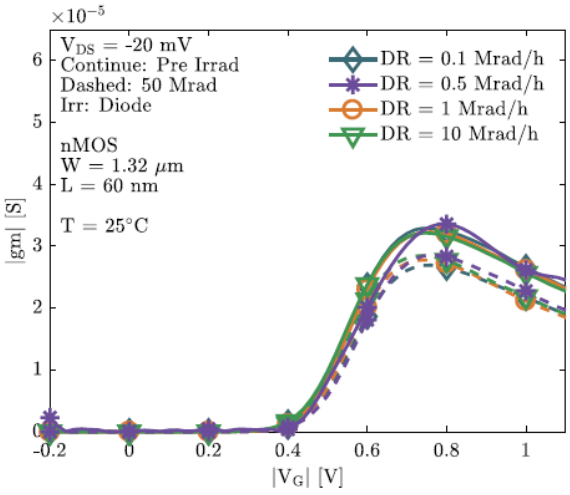

Figure 3.6: Pre- and post-irradiation transconductance curves for the W = 1.32 μm and L = 60 nm PMOS (taken from [26]).

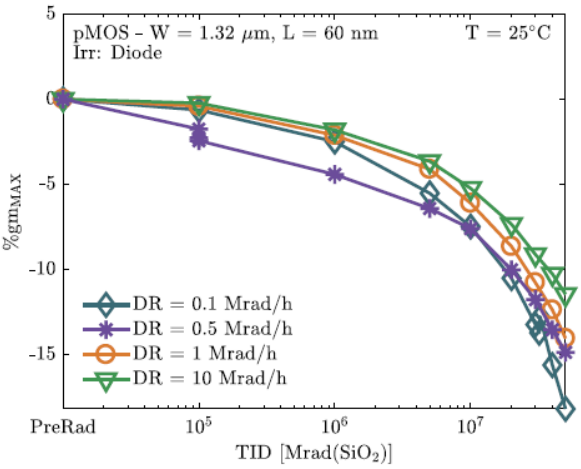

Figure 3.7: Evolution of the peak of the transconductance for the W = 1.32 μm and L = 60 nm PMOS (taken from [26]).

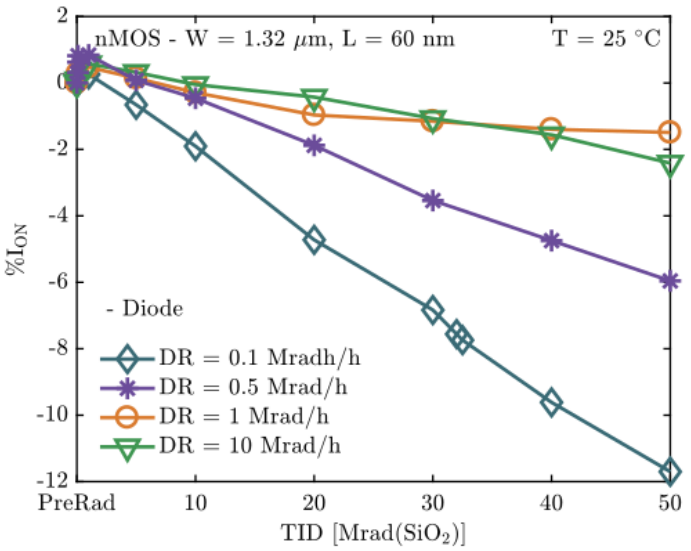

Figure 3.8: ON current percentage variations in function of TID for the W = 1.32 μm and L = 60 nm NMOS transistor, irradiated with different DRs(dose rates) up to 50 Mrad(SiO2) (taken from [26]).

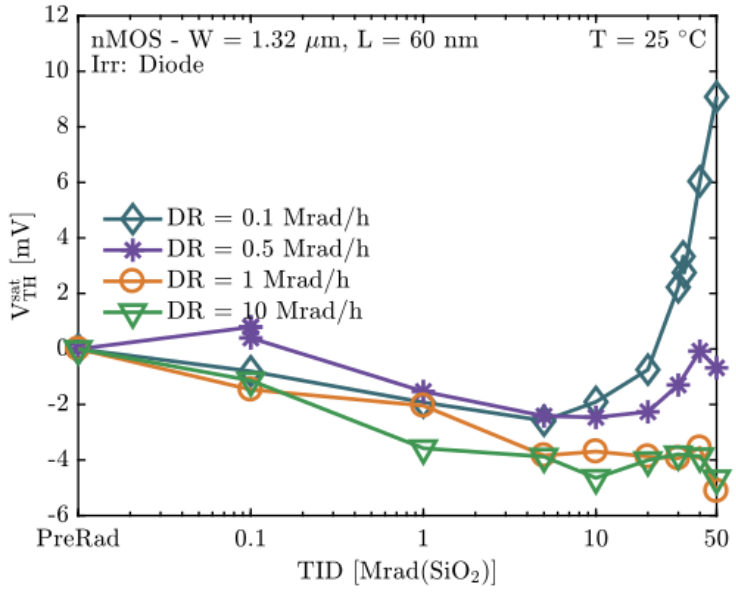

Figure 3.9: Threshold voltage variations for the W = 1.32 μm and L = 60 nm NMOS (taken from [26]).

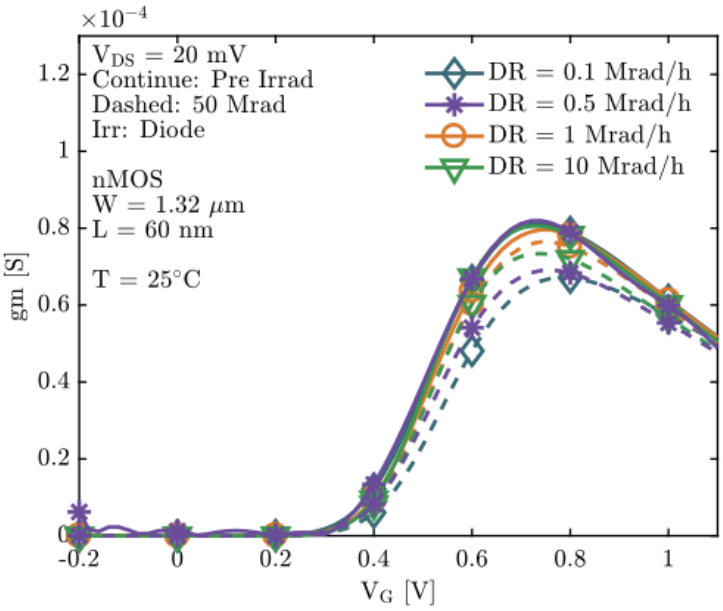

Figure 3.10: Pre- and post-irradiation transconductance curves for the W = 1.32 μm and L = 60 nm NMOS (taken from [26]).

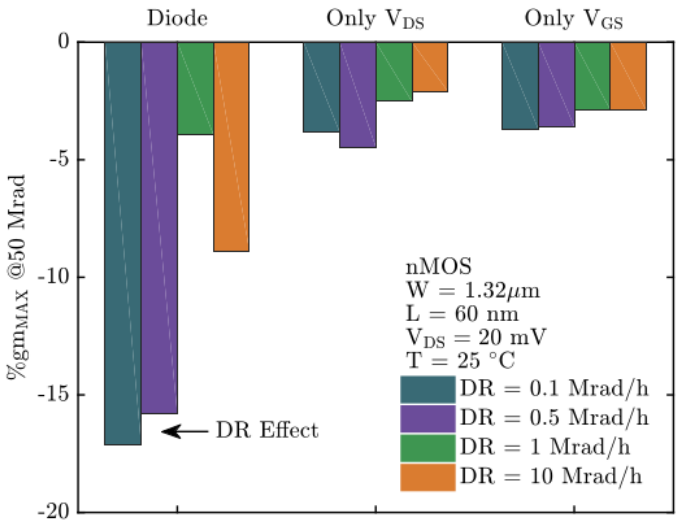

Figure 3.11: Evolution of the peak of the trans-conductance for the W = 1.32 μm and L = 60nm NMOS (taken from [26]).

Through these graphics, it is possible to clearly see that with the variations of threshold voltage, transconductance and current with the device ON being around 21 mV, 20% and 17.5%, respectively, for PMOS devices, and 9 mV, 17% and 12% for NMOS devices. The effect of radiation in the operation of a circuit, more specifically in a comparator, is huge. These effects add up with the mismatch described before, increasing significantly the offset voltage of a comparator.

3.5 Ways to reduce radiation effects on circuits

In order to reduce the radiation effects on integrated circuit, two proceedings can be used.

Radiation Hardening-By-Process, RHBP, this technique studies ways to improve the process used in the manufacture of integrated circuit making them more resilient to radiation. RHBP has been losing popularity in radiation-hardened circuits since these have high complexity and low request from the market.

And Radiation-Hardness-By-Design (RHBD), this procedure consists in using layout and circuit design techniques to design a radiation tolerant circuit with standard CMOS technology. The disadvantage of this technique is that usually to make circuits more resilient, there is more area usage and less speed.

In the thesis, the objective is by applying RHBD techniques to design a comparator capable of resist to radiation (within certain limits that will be studied in the thesis).

Chapter 4

Radiation Hardened Comparator

With the interest of designing a circuit capable of contradicting radiation effects, it is important to traduce the radiation effects into circuit variations, study the deviations imposed by these effects, and then use the available techniques to contradict the unwanted behavior.

4.1 65 nm CMOS Technology

For this study, the CMOS technology node that is used is 65 nm, widely adopted for either logic, SRAM, mixed-signal, mixed-voltage I/O applications or embedded DRAM applications.

Furthermore, this technology provides not just the standard process devices, but also a low and high V_t processes that provide devices with a different characteristics for different applications.

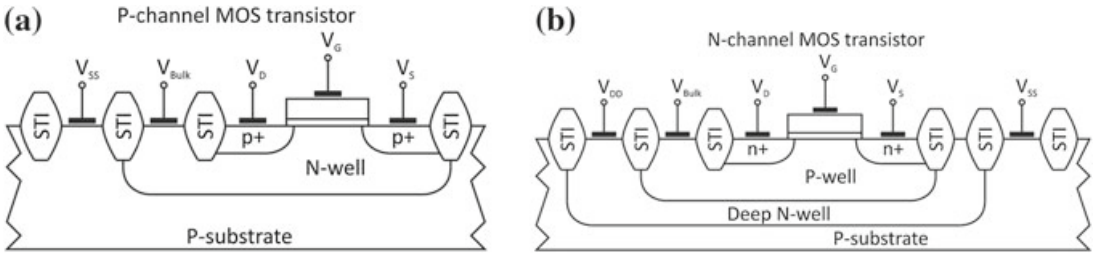

Figure 4.1: Cross sections of MOSFET transistors in 65 nm triple-well CMOS. **a** P-channel MOSFET transistor. **b** N-channel MOSFET transistor (taken from [14]).

For the low-V_t and high-V_t technology, the devices use triple-well on p-substrate CMOS technology as represented in figure 4.1, where PMOS transistor is located in an isolated N-well and the NMOS transistor is placed in an insulated P-well, which is itself embedded in a deep N-well. For the standard 65 nm CMOS, there is no deep N-well, the diffusions are directly on the P-substrate.

In the three cases, the devices are separated by a shallow trench isolation (STI). Inside the wells are the appropriate N+ and P+ diffusion regions. The gate oxide isolates the polysilicon gates from the transistor channels. The spacers ensure the isolation between gate and source/drain areas. Self-aligned silicide, also called salicide, forms the interconnect between the semiconductor and metal layers. The contacts connect

the salicide to the metal layer 1 (M1). The remaining metal layers are also interconnected through the appropriate contacts.

This technology has a nominal supply voltage of 1.2 V and a maximum supply voltage of 1.32 V.

For this work, since it is meant for low-power the high-V_t technology could provide a better solution regarding leakage current at the cost of speed, with the low-V_t technology doing the opposite. The chosen solution was the standard technology since it stands a middle point for speed and for leakage current, and it is the most common one.

4.1.1 Transistor Characteristics

The progress of scaling is noticeable in several transistor parameters and properties. Figure 4.2 shows the output characteristics of an NMOS transistor with varied gate length L in standard 65 nm CMOS technology. The transistor width W is 5 μm and the gate source voltage V_{GS} of 600 mV is applied.

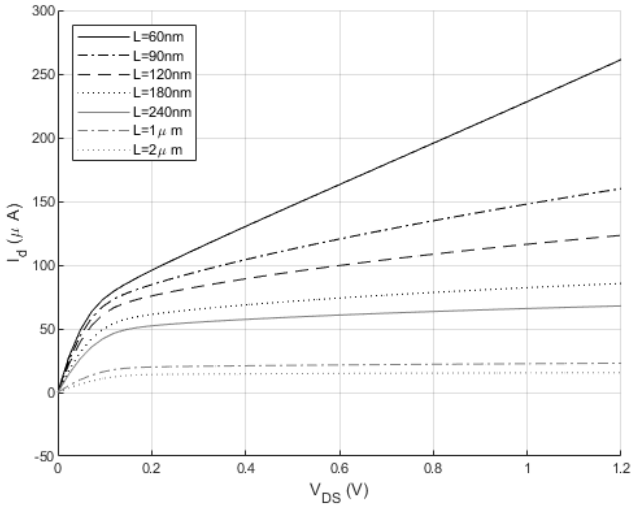

Figure 4.2: NMOS output characteristics at varied gate length L.

Figure 4.3 presents the output conductance g_{DS} against the drain-source voltage V_{DS} which is decreasing with increasing gate lengths (for $V_{DS} > 0.4V$). The transconductance gm of an NMOS transistor with the gate width of 5 μm is shown in Fig. 4.4. V_{DS} is 1.2 V. gm is decreasing with larger lengths L as well as g_{DS}.

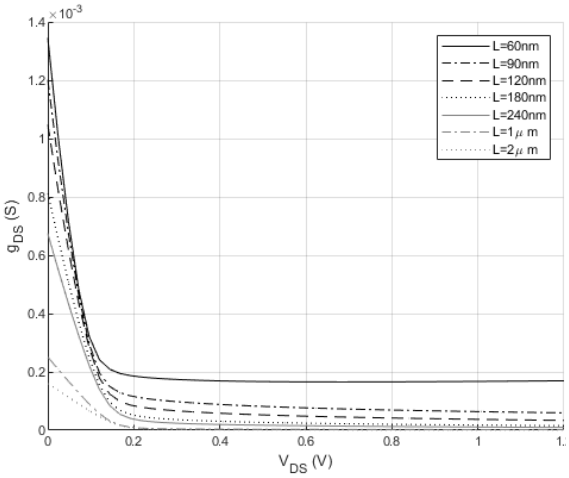

Figure 4.3: NMOS output conductance g_{DS} at varied gate length L.

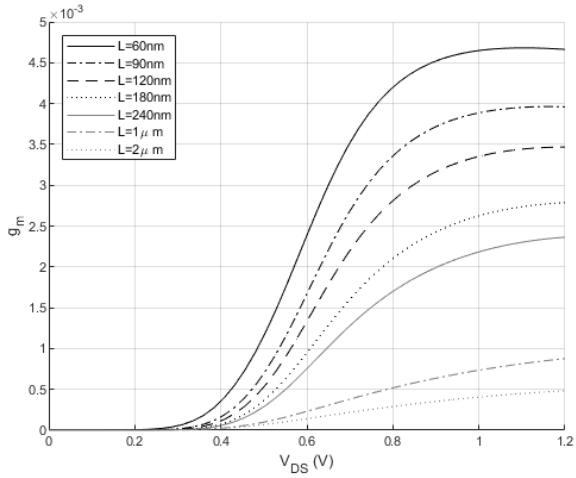

Figure 4.4: NMOS transconductance gm at varied gate length L.

4.2 Mismatches imposed by fabrication and radiation

As briefly mentioned before, firstly, it is important to understand the standard deviations from the fabrication process, and secondly add the radiation effects to these. The type of radiation effect considered for the following sections of this works is always TID, since this type changes the parameters of the circuit without destroying the device. Random single events may occur and produce a wrong comparator response at a given time but these effects are unpredictable and unavoidable and so out of the scope of this work.

Starting by the standard values of V_t and β, since this values have variations for different dimensions of the gate of the MOSFET, the values presented in the table 4.1 were obtained through simulation for devices with 60 nm for the length and 350 nm for the width, which are the most used in the circuit that is going to be presented in the following points of this work.

The standard deviation that represents the variation of the V_t caused by the fabrication process is obtained through the simplified model presented in equation 2.13.

The radiation induced deviations are based on the worst deviation presented in the section 3.4 expressed in its absolute value and in how many standard deviations they represent (useful in future simulations). The V_t variation is directly obtained from the graphics. The β variation is obtained through the transconductance variation and equation 4.1, and is calculated as in equation 4.2.

$$gm = \sqrt{2(\mu C_{ox})(\frac{W}{L})}\sqrt{I_d} = \sqrt{2\beta}\sqrt{I_d} \tag{4.1}$$

$$\Delta\beta = (\Delta gm)^2 \tag{4.2}$$

The total deviation takes into account 3σ for the fabrication process which includes 99.7% of total fabricated devices and adds the deviation imposed by radiation.

Parameter	**W/L** ($\mu m/\mu m$)	**Typical**	A_{vt}	σ	**Radiation Deviation**	**Total Deviation**
Vt_{NMOS}	0.35/0.06	422.7mV	3,5mV/μm	24.15mV	9mV = 0.37σ	3.37σ
β_{NMOS}	0.35/0.06	-	-	-	1.44%	-
Vt_{PMOS}	0.35/0.06	-363.2mV	2,0mV/μm	13.80mV	21mV = 1.52σ	4.52σ
β_{PMOS}	0.35/0.06	-	-	-	3.0625%	-

Table 4.1: Standard and radiation deviations on parameters that suffer from mismatches.

Although, radiation can produce a change in the current factor around 3%, both the ON current and the offset voltage are strongly affected by the V_t variation, and so this is considered the dominant factor for deviation. The deviations applied to the circuit are 5σ considering both type of deviations.

4.3 Offset reduction and compensation

Given all the deviations in devices characteristics considered in the previous section, it's clear that it is very difficult to perfectly pair the devices and obtain the perfect response of a circuit. These effects are even more important for relations between transistors that are based in ratios.

For comparators, specifically the presented type that have a input differential pair, this deviations significantly increase the input offset voltage that highly changes the comparator response, producing errors that can even dictate the inoperability of this circuit.

It's essential in this case, due to the unpredictable increase in errors imposed by radiation, to have a way correct this errors and cancel the input offset voltage. It's also very important to reduce this error by design and by layout techniques that aim to reduce the mismatches effect and that increase radiation resilience.

4.3.1 Offset calibration

In clocked regenerative comparators, there are two main ways to compensate the offset.

In one hand, there is the static offset cancellation (trimming), where additional transistors are added to the circuit in order to introduce an additional current to compensate mismatch. This current is

adjusted only one time in a separate offset cancellation run, with a bias voltage or current applied from outside the chip and stays constant when the comparator does its assigned task. Other possibility of static cancellation is to program the floating gate of p-MOS input transistors of a comparator in a separate offset cancellation run with the help of hot-electron injection by raising the supply voltage. This technique has the advantage of being transparent to the user and the disadvantage of being unable to track variations over time.

On the other hand, there is the dynamic offset cancellation technique. This technique has a much higher interest in general, but particularly in the interest of this work since it allows to correct the offset voltage during the lifespan of a device. The usual way of performing this calibration is by having an input voltage storage that contradicts the offset of the circuit. When analysis the dynamic calibration, it's important to understand if the calibration interrupts the functioning of the circuit case of the comparator from this work (foreground) or, otherwise, if it doesn't (background). Although this comparator needs specific clock cycles to calibrate, it is still possible to use this comparator in ADCs using background calibration, if the calibration is done only in cycles where a comparison is not needed. A deeper analysis on this factor is performed on section A.

4.3.2 Layout techniques

Furthermore, it is well known that the layout has a huge impact on the integrated circuit resilience. Some layout techniques that improve the circuit matching and radiation hardness will be listed below.

- Increase MOS transistors area: this practice can be obtained directly from equations 2.13 and 2.14, since the variation of both V_t and β are inversely proportional to the area of the transistors, by increasing the area, the deviations decrease. The disadvantage of this is that not just the overall circuit area increases but also the MOS devices capacitances, making that for the same speed of operation there is higher power consumption.

- Matrices making and Symmetry in the devices: Dividing one single transistor in a matrix and using inter-digitated, Common centroid or other symmetry techniques are usually used to improve matching in transistors with a common node.

- Dummy transistors: During the process of fabrication of integrated circuits, the transistors from the edges of a matrix suffer from more deviations. To protect transistors with high sensitivity (like a differential pair), transistors with all terminals connected to a supply (called Dummy) are usually used and placed at the edges of the matrices, protecting the important ones.

- Shorten the distance between supplies and the center of the matrix: when designing big matrices sometimes there is the need to polarize devices in the middle, if a big metal line is used in this polarization is used, then the resistance of this line can cause unwanted deviations. To solve this a polarizing line can pass through the matrix shortening the referred distance.

- Separate oscillating signals from stationary biasing signals: To avoid cross-talk between signals that increase of noise.

- Polarizing rings: In order to avoid latch-ups, a good polarization has to be performed by using polarizing rings around each analog and digital block.

- Decoupling capacitors and supply and ground pad/pin placed side-by-side or top/bottom: decoupling capacitors (also known as bypass capacitors) reduce power ripples by providing a low impedance path from the power supply to ground. This is also the reason why supply and ground should be side-by-side but ideally on top/bottom configuration.

- Ring-shaped/Edgeless MOS: Some different transistors shapes are used in order to reduce the effect of radiation.

The referred techniques not only apply to comparator circuits but also to most analog circuits and are one important step to reduce mismatches and improve radiation hardness.

4.4 State-of-the-art of comparator offset voltage cancellation

Focusing the analysis on the dynamic comparator input offset cancellation, there are multiple different techniques that aim to solve this problem. Whether analog or digital offset cancellation, through current, charge or voltage cancellation. The main idea of this calibrations is to insert imbalances to compensate the natural deviation. Although these techniques solve a big problem of comparators, it is worth noting that usually this implies a larger and more power consuming circuit.

Three different comparator topologies with self-calibration of the offset will be studied in the next points of this work.

4.4.1 Taimur Rabuske *et al.*, 2015

In [39] and [40], a very low-power background calibration technique to nullify the comparator offset caused by process, voltage and temperature (PVT), is presented.

The comparator circuit is composed by a Strong-Arm latch dynamic comparator [22] combined with differential offset calibration circuits (presented in figure 4.5).

Regarding the Strong-Arm latch dynamic comparator, it has the advantages of consuming zero static power, producing rail-to-rail outputs and, very important in this context, the offset voltage arises primarily from the input differential pair. In this circuit, the difference between inputs drives a differential current which activates the latches, leading to positive feedback that bring one output to 0 and the other to V_{DD}.

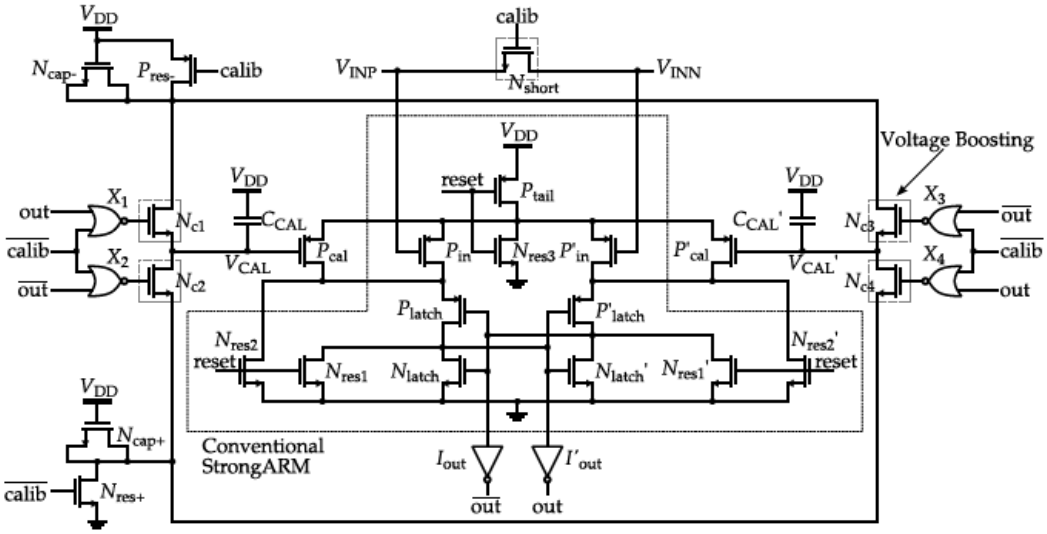

Figure 4.5: StrongARM latch with offset cancellation from [39].

In this circuit, the difference between inputs drives a differential current which activates the latches, leading to a positive feedback that bring one output to 0 and the other to V_{DD}.

The calibration process in this circuit increases or reduces VCAL by a small step $\Delta VCAL$ until the offset is cancelled or the calibration process ends. This technique works in the following way (as described in [39]):

1. With C_{CAL} and $C_{CAL'}$ initially discharged, V_{CAL} and $V_{CAL'}$ are at V_{DD}, and since P_{CAL} and $P_{CAL'}$ are cut-off, they have a reduced effect on the calibration threshold. Also since "calib" is '0', P_{res-} and N_{res+} are ON and that way N_{cap-} is discharged to ground and N_{cap+} is charged to V_{DD}.

2. When "calib" turns to "1" (indicating a calibration sequence), N_{short} shorts the inputs V_{INP} and V_{INN}, making the differential voltage from the comparator equal to 0. When the inputs have stabilized, a comparison is requested by pulling down the "reset" signal and the obtained results (a digital "0" and "1") are used, jointly with the fact that "not calib" is "0" to identify which is the

lower and the higher side (one MOS switch among N_{c1} and N_{c2} and one MOS switch among N_{c3} and N_{c4} are closed).

3. In the last part of the calibration process, part of the charge stored in N_{cap+} is redistributed to C_{CAL} or $C_{CAL'}$ and part of the charge stored in C_{CAL} or $C_{CAL'}$ is lost to N_{cap+}. This reduces the voltage of the slower branch, V_{CAL} or $V_{CAL'}$, increasing the current in P_{CAL} or $P_{CAL'}$. Since this circuit works with negative feedback, the comparator offset is reduced and with enough cycles cancelled. The process can be stopped when the output starts oscillating between "0" and "1", which means that the minimum step was reached. However, if continuously performed it corrects PVT errors on-the-fly.

4.4.2 Xiaopeng Zhong *et al.*, 2017

In [41] and [42], a low-offset two-stage dynamic comparator for multi-channel processing is presented.

In this comparator, low offset is obtained through 1st stage offset cancellation (cancelled by an improved input-offset-storage scheme, [43]) and 2nd stage offset suppression (suppressed by high gain of the 1st-stage dynamic amplifier). The advantages of this circuit are high flexibility, low kickback noise, high speed, low supply voltage and the fact that the offset can be reduced with low dependency on common-mode voltage.

The circuit used in [41] is presented in figure 4.6. The 1st stage, composed of the transistors M1-M7, amplifies the input signal difference between nodes In_+ and In_- by differentially discharging the output nodes Do_+ and Do_-. The second stage drives the latch generating full-swing digital outputs (Out_+ and Out_-) by positive feedback.

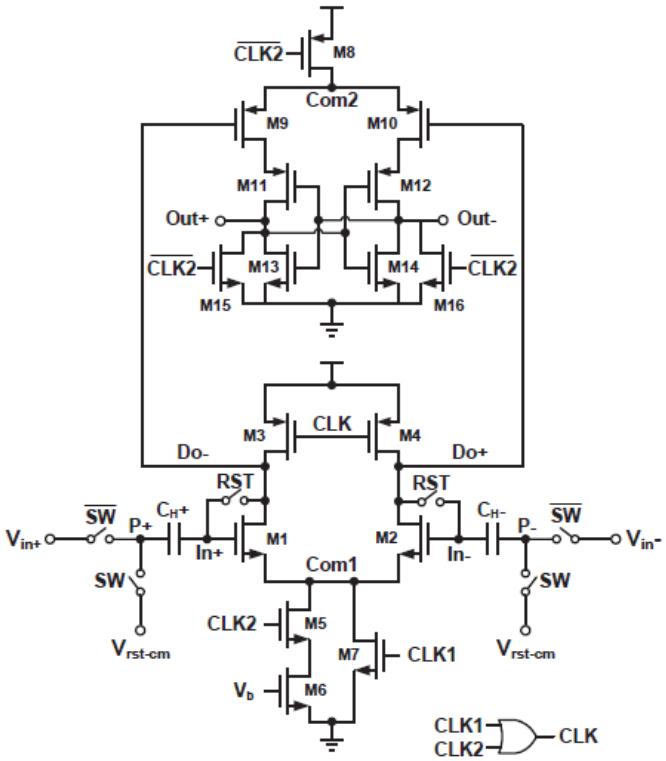

Figure 4.6: Two-stage dynamic comparator (scheme from [41]).

The operations of this comparator is separated into two phases: Reset and Comparison. The operation principle of this comparator is (as described in [41]):

1. A complete operation starts by turning on the reset switches using RST. In+ is connected to $Do-$ and $In-$ is connected to $Do+$.

2. CLK1 rises up after voltage reset is completed. It disables M3 and M4 and enables M7. CH± start to discharge through M1 and M2 respectively to ground.

3. After some time, M1 and M2 enter the sub-threshold region and I± are drastically reduced. RST falls down to sample reset voltages in $CH+$ and $CH-$ respectively. Offset is contained between the reset voltages and stored.

4. $Do+$ and $Do-$ are reset to V_{DD} again for comparison. At the same time, SW goes down to input $Vin+$ and $Vin-$.

5. Evaluation starts. $In+$ and $In-$ are compared by discharging $Do+$ and $Do-$ through a common current source I_b. Then $Do+$ and $Do-$ drive the 2nd stage to generate latch outputs $Out+$ and $Out-$.

4.4.3 M. Nasrollahpour *et al.*, 2017

In [44], a low-power current based preamplifier and latch circuit comparator is presented. This circuit is composed by a cascade amplifying stage along with a latch stage providing a better control over the trade-off between offset voltage and power consumption. The circuit from [44] is presented at figure 4.7.

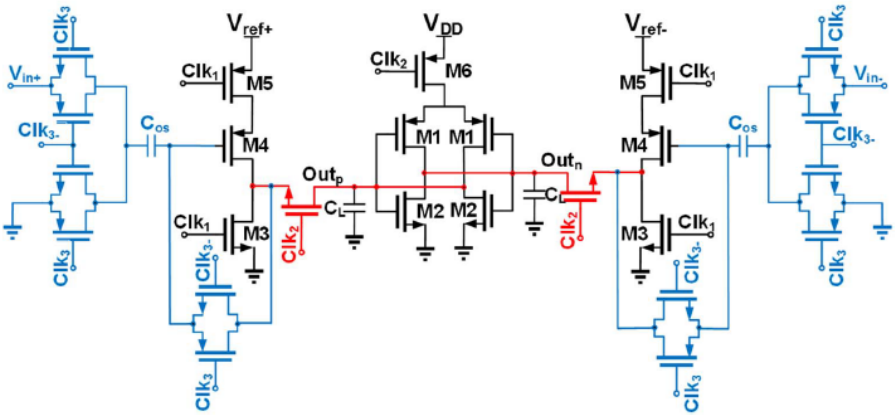

Figure 4.7: Low-power current based preamplifier and latch circuit comparator (scheme from [44]).

The comparator works in three phases, determined by two separate clock signals applied to the circuit, CLK1 and CLK2. The amplification phase and the comparison phase are isolated using the clock pulse which guarantees that the offset caused by internal node mismatch in the latch circuit is cancelled by the amplification provided in the input transistors. The functioning of the comparator is as explained in [44]:

1. In the first phase (reset), both clocks signals are high which causes M3 transistors to discharge the outputs to ground.

2. In the second phase (1st phase of comparison), as soon as CLK1 becomes low, the transistors M5 which are biased in deep triode region causing them to act as small resistors at the source of the input transistors, turn on. Since the entire reference voltage is present across the source of the input transistor and the decision point, the input gate of the transistors is also greater than zero, the drain source voltage (V_{DS}) becomes higher than the gate source voltage (V_{GS}), leading to the input transistors acting as a current source in the saturation region. These current charges the latch circuit which leads to the third phase.

3. In the third phase (2nd phase of comparison, regenerative phase), as soon as CLK2 becomes low, the transistor M6 turns on and the latches begin to regenerate, depending on the voltages of the

internal nodes which are proportional to input currents.

Furthermore, to minimize the offset and defects on the decision making of the comparator, a offset cancellation technique is added, composed by a CLK3 which during its cycle stores the offset voltage on a capacitor and then discharges to ground.

4.5 StrongARM Latch with Offset Calibration

The comparator circuit presented in figure 4.8 is the comparator circuit described in section 2.6.1, and that presents as primary advantages of high input impedance, input-referred offset arises from primarily one differential pair, zero static power, high-speed and full swing output, with the calibration employed in [39] that if given enough time corrects the input offset voltage of a comparator and that can be used as background calibration in ADCs.

This topology is identical to the employed in the low-power ADC from [39], and, in this section of this work, its capability to correct, not just fabrication mismatches and aging effects, but also radiation effects will be tested, as well as the limits in which this circuit can operate.

The Double Tail Comparator topology with the calibration scheme of [39] was also tested to compare the results with this one, but since the results were significantly worst and less consistent, the following studies were only performed to this configuration. It is possible to see the circuit employed for the Double Tail in appendix B.

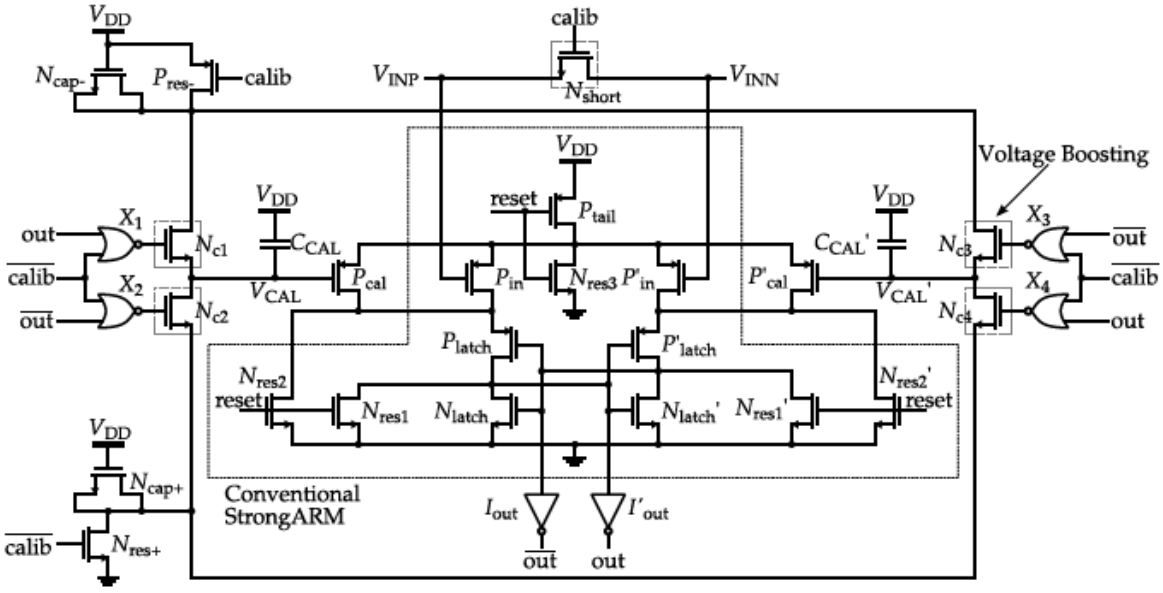

Figure 4.8: StrongARM latch with offset calibration. (scheme from [39]).

The StrongARM Latch topology was already studied in the section 2.6.1 of this work as well as the calibration circuit which is presented in section 4.4.1.

4.5.1 Sizing

Regarding the sizing of circuits, in general, this step is highly dependent on the circuit application, meaning a given choice may improve the circuit speed and worsen its output quality or require more power. This is why these trade-offs have to be carefully taken in account in order to perform the best fitting circuit for a given application.

The normal trade-offs when designing a circuit are:

- Speed of the circuit
- Area of the circuit
- Quality of the Output
- Power needed/Voltage level required
- Power consumption - static and dynamic

In the comparator case since it is a mixed-signal device, with analog inputs and a digital output, the quality of the output has less importance than it would have in an amplificator for example. For the studied device, the reasoning of the sizing follows the logic that, for a given voltage level, the circuit should be as fast as possible while keeping the other quantities in acceptable levels. Naturally, a faster circuit usually means less area, considering that the transistors capacities are proportional to the device area, hence, with higher area comes higher capacitance in the nodes of the circuit, and so more time to charge those nodes is needed (all CMOS parasitic capacities are directly proportional to the area of the devices). This analysis is very simplified as in some cases having higher gain which depends on the W/L ratio (meaning an increase in area), also improves the speed of the circuit.

Analyzing the MOS devices present in figure 4.8, there are multiple transistors whose function are to implement either a simple switch, namely transistors P_{res-}, N_{res+}, N_{c1-4} and N_{res1-4}, or a logic gate (inverter and nor). When implementing these, transistors normally operate either in cut-off region or driven by V_{DD}, which means that these working points don't require high device gain, hence, the speed of the circuit highly benefits from the minimum dimensions possible.

In this work, the minimum dimensions are assumed to be a length of 60 nm and a width of 350 nm which allow the devices to have two contacts when performing the layout of the circuit, guaranteeing redundancy in the contacts.

Figure 4.9 confirms the behavior described above since it is clearly possible to see that for the same gate length, which is 60 nm, for larger widths the response of the comparator worsens to the point where is possible to see that the circuit doesn't work properly at the same speed (for W = 2.5 μm at f = 1 GHz).

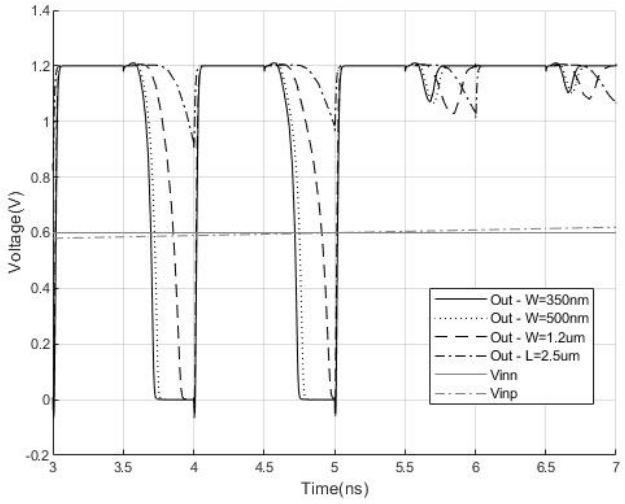

Figure 4.9: Output of the StrongArm latch comparator for different widths of the transistors in switches and logic gates.

On a second notice, the transistors that receive the calibration voltage and produce the current that corrects the offset (P_{cal} and P'_{cal}) are not required to react as fast, since during the normal comparison cycle they have a constant bias and so following the same reasoning, they wouldn't benefit from larger width since they don't need high gain to contradict a fast switching.

Furthermore, these devices are in parallel with the input differential pair, in case these are on, due to calibration, the current will drive the latch nodes. Being both helpers and competitors, these should be as small as possible to keep the input differential pair as the primary charger of the latch nodes.

The chosen dimensions for these devices are also the minimum ones. As it can be seen in figure 4.10, similar to what was presented above, when increasing the width of these the result is even more significant since for some cases (W = 1.2 μm and W = 2.5 μm) it completely shifts the transition point.

Moreover, the most important transistors are the ones from the input differential pair (P_{in} and P'_{in}) since these are responsible for driving the nodes above the latches as quickly as possible based on the differential inputs, being not just a critical element for speed but also for the input offset voltage since, as already referred before, it arises mainly from this transistors.

Normally, these transistors could be designed assuming that the difference in V_t is the main contributor

for the offset voltage, then defining an acceptable level of offset and through mismatch equation 2.13 obtaining the minimum area, which joined with the natural need for speed would grant the devices dimensions.

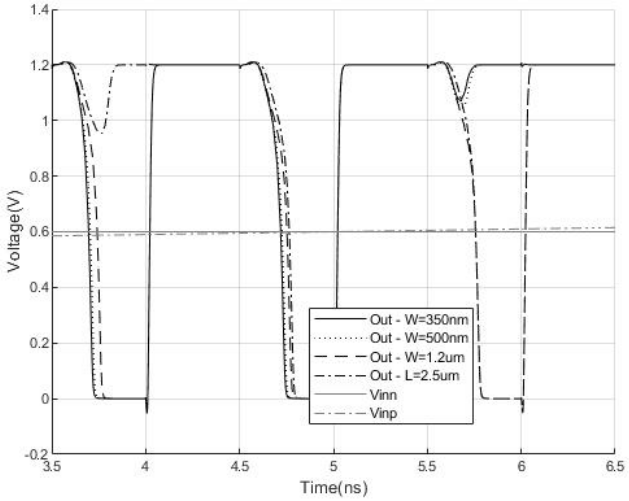

Figure 4.10: Output of the comparator for different widths of the calibration transistors.

In this case, since as referred before and will be demonstrated later the offset will be compensated through a compensation circuit and so that condition isn't required, being speed the only focus point. As said before, these transistors drive the differential nodes so they need higher gain, even though this also increases the parasitic capacitances.

In figure 4.11, the described behavior can be seen and it can be concluded that adopting a width of 5 μm with a length of 60 nm helps achieve a speed as good as for lower widths with the advantage of lower leakage current.

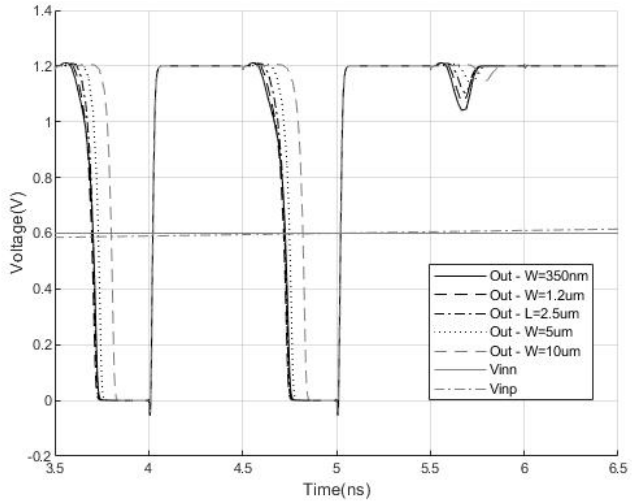

Figure 4.11: Output of the comparator for different widths of the input differential pair.

Lastly, for the transistors that form the crossed latches (P_{latch}, P'_{latch}, N_{latch} and N'_{latch}), these follow a similar reasoning of the differential pair, although with less need for device gain. These devices benefit from having slightly larger widths, not just because helps them charge the latch nodes faster, but they also are highly affected by the increase of parasitic capacitances. In figure 4.12, it can be seen that the middle point for both effects referred is for a width of 500nm where the circuit has approximately the same speed as for 350nm but is less affected by leakage.

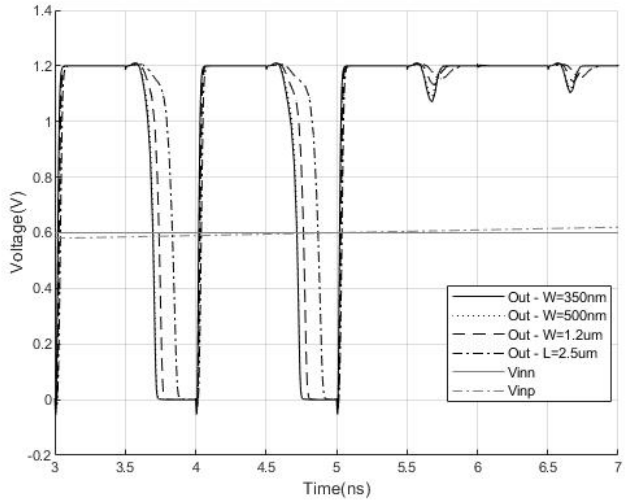

Figure 4.12: Output of the comparator for different widths of the latch transistors.

Regarding calibration capacitors in the circuit, these come in two forms, two smaller capacitors (N_{cap-}

and N_{cap+}), implemented using NMOS devices, which define the charge step that is passed to two larger capacitors (C_{cal} and $C_{cal'}$), implemented with MIMCAPs that store this charge in order to contradict the offset voltage in the circuit.

Towards performing the sizing for these units, one very important thing to realize is that the normal behavior of a capacitor, described by its charging/discharging equation over time has little weight, since in this case, the main concern is defining the charge step that is being passed in each cycle to the bigger capacitor and the voltage difference that this represents in the voltages V_{cal} and $V_{cal'}$, that is defined through the ratio between the smaller and bigger capacitors. Hence, even if the capacitors were slow to charge/discharge and this process was interrupted by the clock cycle, this would only mean that the charge passed in each clock cycle was smaller. One important aspect regarding the definition of this charge step that is traduced in an offset voltage step is the trade-off between definition and calibration time. For a smaller step the definition can be highly improved at the cost of more cycles needed to correct the offset.

There is also another aspect that can be important when sizing the larger capacitors which is the discharge over time by leakage, this effect can mean that after calibration, this calibration is progressively lost through leakage. A larger capacitor can hold the calibration for longer, which could signify that larger capacitors were needed, but since this circuit can perform calibration in periods smaller than a significant discharge period and this effect was not significant for any of the tests performed, the main concern when sizing these units is the calibration time as well as the charge step (traduced in a voltage step).

Figures 4.13 and 4.14 supported by the table 4.2 represent different dimensions for both type of capacitors and how that traduces in the important referenced quantities, calibration time and offset voltage step (that in this case is obtained giving enough time to fully calibrate the offset so that the only offset remaining is the minimum step of calibration).

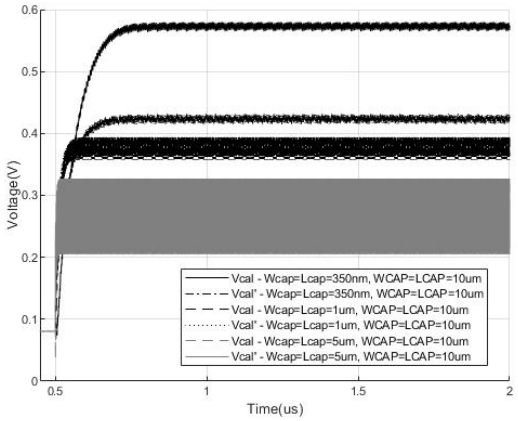

Figure 4.13: Calibration voltages for different W_{cap}=L_{cap} and W_{CAP}=L_{CAP} = 10μm.

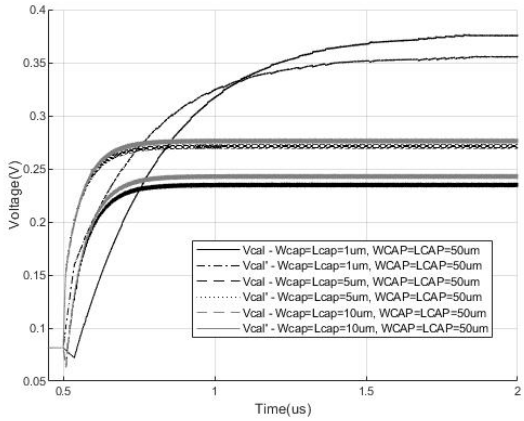

Figure 4.14: Calibration voltages for different W_{cap}=L_{cap} and W_{CAP}=L_{CAP} = 50μm.

W_{cap}/L_{cap} (μm/μm)	W_{CAP}/L_{CAP} (μm/μm)	Offset before calibration(mV)	Calibration time(ns)	Offset after calibration(mV)
0.350/0.350	10/10	177.6	78	3.7
1/1	10/10	177.6	70	58.4
5/5	10/10	177.6	14	134.4
1/1	50/50	177.6	1345	0.1
5/5	50/50	177.6	400	0.4
10/10	50/50	177.6	350	2

Table 4.2: Calibration time and offset analysis for different areas.

Note: $W_{CAP} * L_{CAP}$ is the area of C_{cal} and $C_{cal'}$ and $W_{cap} * L_{cap}$ is the area of N_{cap-} and N_{cap+}.

The described behavior is easily observed, for smaller ratios $(W_{CAP} * L_{CAP})/(W_{cap} * L_{cap})$, the calibration is much faster but the remaining offset is also bigger. This sizing choice is highly application dependent, since the most important factor could be calibration time or remaining offset. For this work, the sizes $W_{CAP} * L_{CAP} = 50\mu m * 50\mu m$ and $W_{cap} * L_{cap} = 1\mu m * 1\mu m$ were chosen.

Table 4.3 provides the sizing choices for the implemented circuit in a condensed way.

Device	**Width**	**Length**
P_{res-}, N_{res+}, N_{c1-4} and N_{res1-4}	350nm	60nm
Inverter and Nor gates	350nm	60nm
P_{cal} and P'_{cal}	350nm	60nm
P_{in} and P'_{in})	5μm	60nm
P_{latch}, P'_{latch}, N_{latch} and N'_{latch}	500nm	60nm
N_{cap-} and N_{cap+}	1μm	1μm
C_{cal} and $C_{cal'}$	50μm	50μm

Table 4.3: Sizing choices.

4.5.2 Characterization

With both the circuit functioning and its sizing defined, it is now possible to test the circuit limits and the results that can be achieved using it. As it is well known, the supply voltage under which the circuit will function is highly application dependent and highly changes the results that can be achieved. With that in mind and knowing this is a circuit intended for low-power, two different supply voltages were used and the results for each will be analyzed, being these 1.2 V and 0.6 V.

4.5.2.1 Supply voltage 1.2 V

In this analysis the supply voltage is defined as 1.2 V and the sizing is defined as in table 4.3. The first analysis to perform is to the maximum operating frequency.

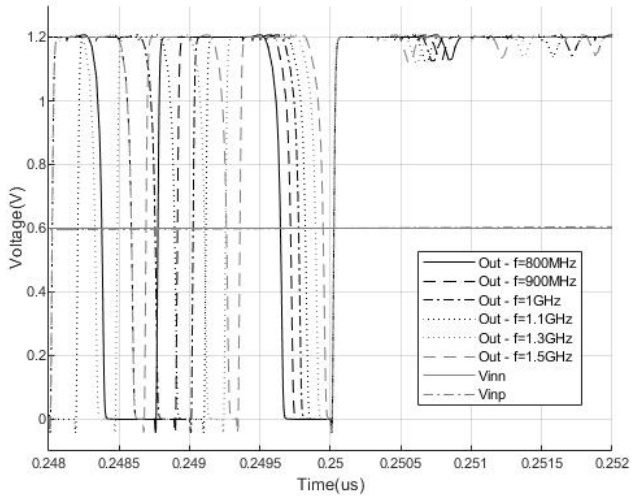

Figure 4.15: Output of the comparator for different frequencies, with $V_{DD} = 1.2$V.

When increasing the frequency the circuit may not have enough time to produce a square wave at the output, especially near the transition point.

As it can be seen in the figure 4.15, which presents the output for different frequencies near the transition point, for 1.5 GHz, the circuit is not producing a square wave and so it can be considered that the circuit is operating at a higher frequency but with lower sensitivity.

Since in this work, the main objective is study the capability of the circuit to reduce the offset to a value as small as possible (always within reasonable values), the chosen decision criteria was that sensitivity had to be approximately 0.1 mV. Meaning that the comparator had to produce a square wave at the output (with the right value depending on the comparison) for a difference of 0.1 mV between its

inputs.

The circuit was then set to perform a comparison for every 0.1 mV difference between entries, and for the frequency 1.3 GHz, even with only a difference of 0.15 mV between entries, the comparator still produces a square wave, although with only 7% of duty cycle (it can only be guaranteed for 0.15 mV and not for 0.1 mV, because the evaluation period may not start at exactly 0.1 mV from the equality point).

It is worth noting that, this conditions and simulations were performed in typical conditions, for real circuits and circuits under radiation effect the sensitivity can change drastically.

With the operating frequency defined, it is now possible to obtain the normal comparator curves. Figure 4.16 shows the response in time of the comparator for one fixed input(V_{inn}) and the other varying from GND to V_{DD} (V_{inp}), for the typical case. Figure 4.17 represents the same response but in order to the difference between inputs ($V_{inp} - V_{inn}$).

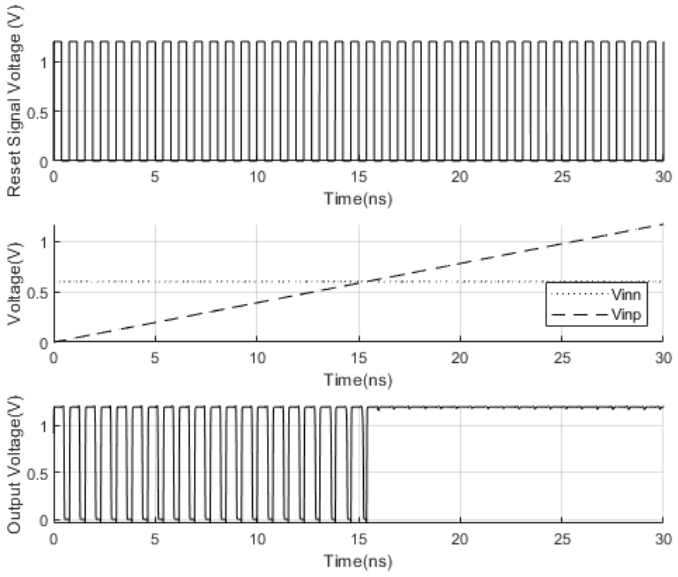

Figure 4.16: Time response of the comparator, with $V_{DD} = 1.2V$.

A important aspect about this result is that, the response has a good behavior from 0 to V_{DD}. If either of the inputs surpasses $V_{DD} - V_t$, the appropriate input transistor would turn off considering the simpler models of MOS functioning. However, what happens is that the circuit still works in sub-threshold region and can react even to a very small difference between entries in deep sub-threshold region.

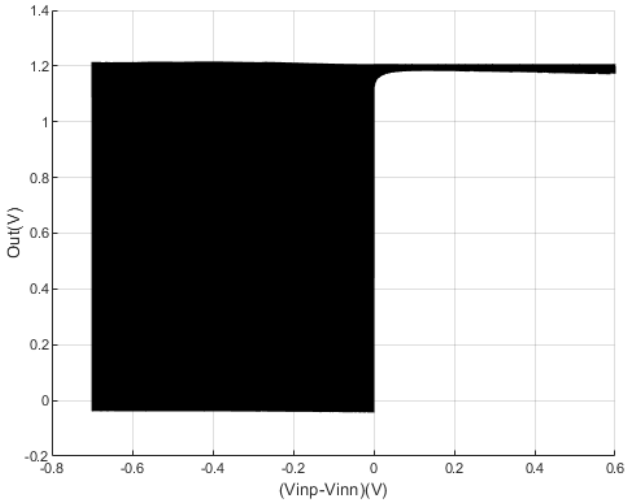

Figure 4.17: Output of the comparator in order to the difference between inputs ($V_{inp} - V_{inn}$), with $V_{DD} = 1.2$V.

Having the reset signal imposing GND in the nodes of the comparator, and consequently, V_{DD} at the output nodes (they are inverted), makes that in every cycle even if the response of the comparator is 0V the circuit still has half of the cycle with V_{DD} at the output. Because of this behavior is harder to compare figure 4.17 with the ideal behavior present in figure 2.2. However, it can still be seen that the output transitions to GND for $V_{inp} - V_{inn}$ less than 0V and stays at V_{DD} for $V_{inp} - V_{inn}$ greater than that, as in the ideal behavior.

In table 4.4 some important characteristics of the comparator response are presented for the typical case.

Typical	StrongArm Latch
Supply voltage	1.2V
Sampling Frequency	1.3GHz
Sensitivity	0.15mV
ICMR	[0, 1.2]V
Power P_d	86.466μW
Propagation delay	0.15275ns
Resolution	12 bits

Table 4.4: Characteristics of the implemented comparator response, for typical run, with $V_{DD} = 1.2$V.

Although the shown curves represent the ideal response of a comparator, they are far from reality since this circuit will present deviations in its parameters not just due to the fabrication process where it is assumed that the deviations can go up to 3σ, covering 99.7% of the fabricated devices, as well as the radiation induced effects. Following the presented table 4.1, it can be assumed that 5σ of total deviation

would account for both this quantities and so a 30-Monte Carlo simulation was performed to obtain the circuit response under this circumstances.

Before analyzing the overall performance of the circuit in the 30 - MC runs, one run was chosen to analyze the calibration process in more detail.

Figure 4.18 shows the comparator output without calibration and table 4.5 represents the devices parameters for that run.

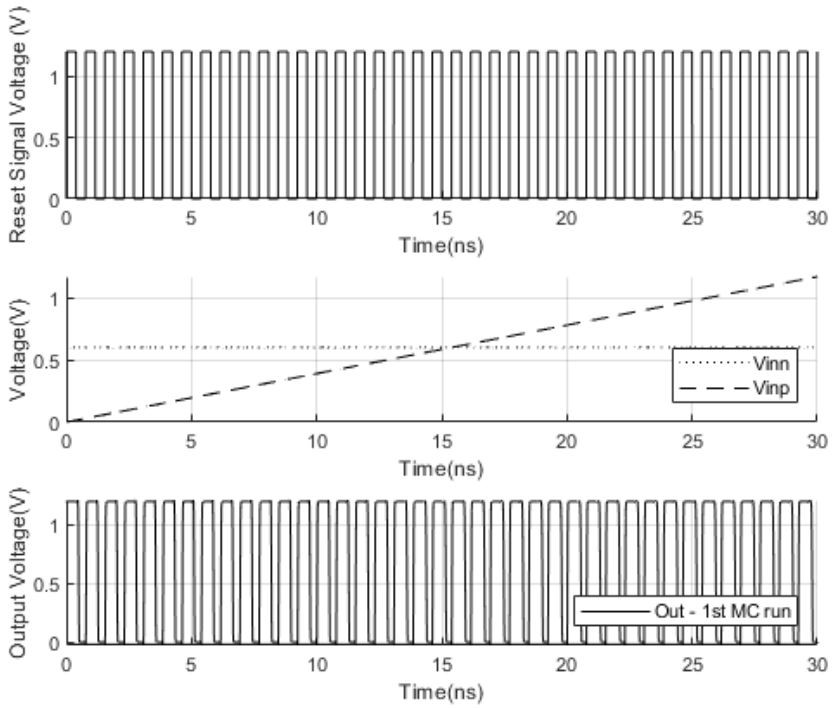

Figure 4.18: Output of the comparator for one MC run, before calibration, with $V_{DD} = 1.2$V.

MC Run	StrongArm Latch
V_{tp}	-694.2mV
V_{tn}	393.6mV

Table 4.5: Threshold voltage for one MC run, with $V_{DD} = 1.2$V.

Starting by comparing the threshold voltage for this run with the ones presented in table 4.1 as the typical ones, it can be seen that there is a significant shift in the threshold voltage for NMOS and PMOS devices. So much significant that by analyzing the figure 4.18, it can be seen that the comparator only outputs a '0' after the evaluation phase, meaning that no comparison is being performed. It can be concluded that the offset for this situation must be greater than 600 mV, since no transition is seen for any $V_{inp} - V_{inn}$.

In order to try to correct this offset, the calibration circuit was activated, obtaining the behavior represented in figure 4.19.

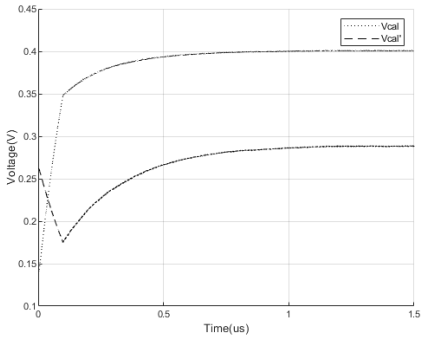

Figure 4.19: Calibration voltages represented in time, during the calibration of one MC run, with $V_{DD} = 1.2V$.

Short-circuiting the inputs of the comparator and using the output to detect the unbalance, the calibration capacitors were charged until the offset was corrected. They rapidly obtain a significant difference that contradicts the offset. After that, knowing that the calibration period is still active, the circuit keeps reducing the offset to the maximum possible with the charge step implemented.

The output after calibration for the same run as in figure 4.18, is represented in figure 4.20.

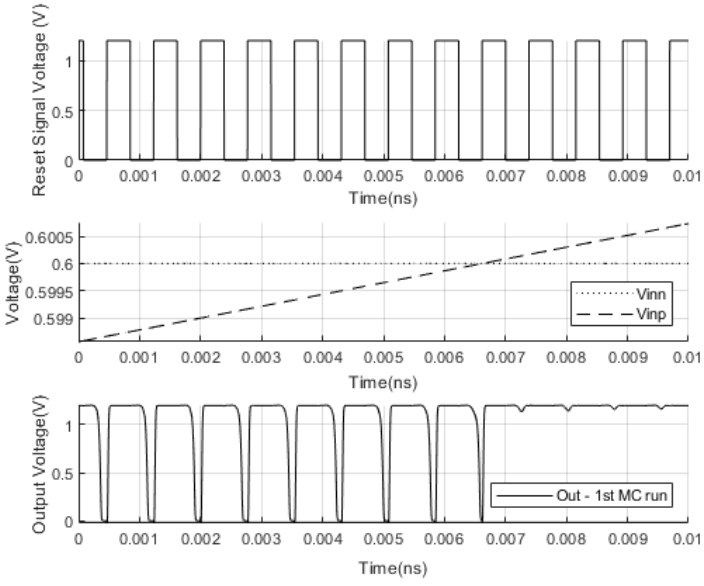

Figure 4.20: Output of the comparator for one MC run, after calibration, with $V_{DD} = 1.2V$.

Through this graphic, it is clear how strong this calibration circuit is. The pre-calibration offset was greater than 600 mV and after calibration it's smaller than 0.1 mV. Moreover, the circuit is still capable of

outputting a square wave, even if with a reduced duty cycle (obviously, this response could be insufficient depending on the specifications of a given application, other choices would have been taken in that case).

Since this only represents one MC run, the distribution of the offset before and after calibration for all runs can be also seen in figures 4.21 and 4.22, respectively. Furthermore, some additional detail on the results is presented in appendix C.

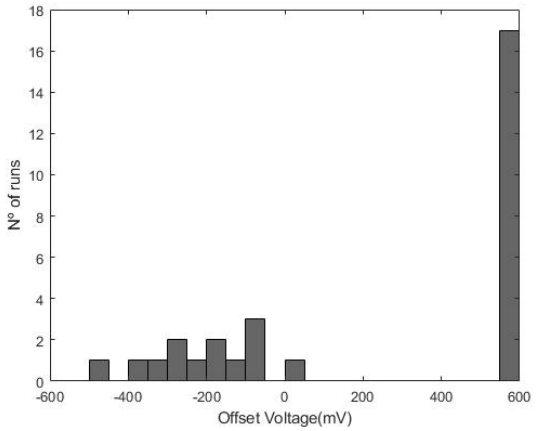

Figure 4.21: Histogram of the offset voltage, before calibration, with $V_{DD} = 1.2$V.

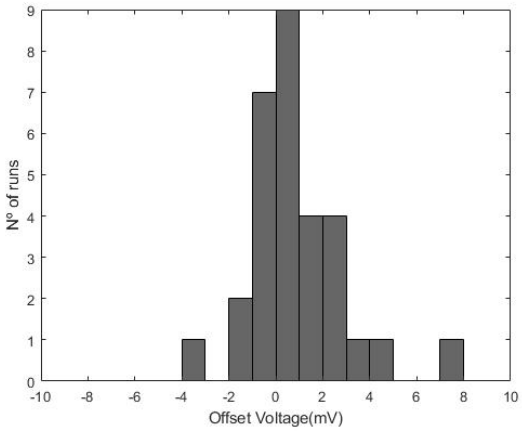

Figure 4.22: Histogram of the offset voltage, before calibration, with $V_{DD} = 1.2$V.

Note: Since $V_{DD} = 1.2$V and one of the inputs is fixed at 0.6 V, if the offset is greater than 0.6 V in either the positive or negative way, no transition from low state to high state happens, and so the offset is represented as if it is 600 mV.

Before calibration, the offset is quite significant, reaching values above and below 600 mV multiple times, as it was the case of the run analyzed before. Even for the offset values closer to 0 V, the minimum offset voltage obtained was 11 mV (can be consulted in appendix C), and this shift completely changes the comparator behavior which can dictate the inoperability of this circuit.

After calibration, in the majority of the cases, the offset is almost totally cancelled. Not only to values under 8 mV, as is the case for all performed tests, but also to values under 1.5 mV, as is the case for 22 of these.

The offset is a very important factor, however, there are also some other very important quantities in a comparator used to measure its performance, which are presented in table 4.6.

30-MC runs	Mean Value	Standard Deviation	Maximum	Minimum
Supply voltage	1.2V	-	-	-
Sampling Frequency	1.3GHz	-	-	-
ICMR	[0, 1.2]V	-	-	-
V_{tp}	-367.82mV	63.25mV	-209.4mV	-581.5mV
V_{tn}	421.9mV	68.89mV	656.6mV	253mV
Offset	0.8mV	1.3mV	7.6mV	-3.2mV
Power P_d	88.0μW	7.9μW	104.9μW	68.3μW
Propagation delay	0.172ns	0.024ns	0.230ns	0.1174ns
Sensitivity	1.9mV	2.1mV	14.7mV	0.1mV

Table 4.6: Comparator response characteristics for 30-MC runs, with $V_{DD} = 1.2$V.

Through the data present in the table, adding the results obtain in the presented histograms, it is clear that this circuit performs a good compensation of the offset, presenting corrections of more than 600 mV in some cases. In fact, the main problem in the comparator response is that the shift in V_t and β sometimes significantly change the speed to which the nodes charge by pushing the devices into deep sub-threshold region and also making their gain smaller. This fact means that the sensitivity of the circuit can be worse in those cases. However, with the offset voltage almost completely corrected is still possible to use the comparator within certain limits.

Naturally, all the presented characteristic have to be analyzed in the context of a specific application. For the chosen speed, the sensitivity obtained for these circumstances was presented, but at the cost of circuit speed, a circuit with a more refined sensibility could be obtained.

With this it is possible to calculate the figure of merit for this comparator configuration, equation 4.3.

$$FOM = \frac{P_d}{2^n f_s} = \frac{88.0\mu W}{2^{9bits} * 1.3GHz} = 0.1322fj/conv \tag{4.3}$$

4.5.2.2 Supply voltage 0.6 V

In a similar way to what was performed previously the supply voltage was fixed to 0.6 V. This voltage is much lower than the previously studied voltage and in most of the cases it means that most transistors will operate in the weak inversion and even in sub-threshold region. This functioning point is very relevant even more than the previously studied because as introduced in the previous chapters low power circuits have been gaining popularity and are being widely used.

The first analysis performed was to the maximum operating frequency of the circuit, from where it was established that in this case the sampling frequency would be 20 MHz.

As before with the operating frequency defined for this case, it is now possible to obtain the normal comparator response. Figure 4.23 shows the response in time of the comparator for one fixed input(V_{inn})

and the other varying from GND to V_{DD} (V_{inp}), for the typical case.

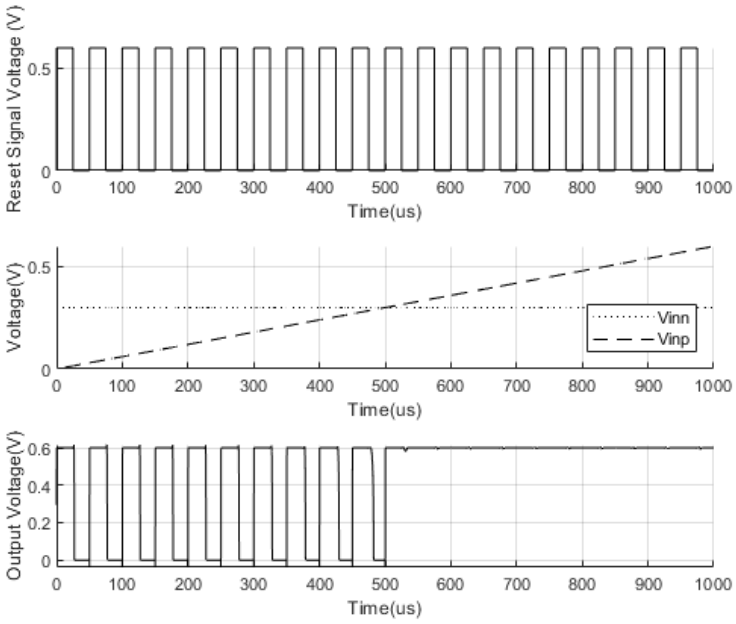

Figure 4.23: Time response of the comparator, with $V_{DD} = 0.6$V.

In table 4.7 some important characteristics of the comparator response are presented, for the typical case.

Typical	StrongArm Latch
Supply voltage	0.6V
Sampling Frequency	20MHz
Sensitivity	0.15mV
ICMR	[0, 0.6]V
Power P_d	2.7545μW
Propagation delay	1.98ns
Resolution	12 bits

Table 4.7: Characteristics of the implemented comparator response, for typical run, with $V_{DD} = 0.6$V.

Not considering the frequency change, the nominal response of the circuit is very similar to what was obtained before, as expected. Even more than the previous case the transistors operate in sub-threshold region and a comparison can still be correctly performed. Furthermore, the power is much lower than the previous case, being possible to see the trade from high speed to low power referred before.

Following the same reasoning as before, with the fabrication process deviations up to 3σ, covering 99.7% of the fabricated devices, as well as the radiation induced effects presented table 4.1, it can be assumed that 5σ of total deviation would account for both this quantities and so a 30-Monte Carlo simulation was performed to obtain the circuit response under this circumstances.

Before analyzing the overall performance of the circuit in the 30-MC runs, one run was chosen to analyse the results of the calibration process in more detail. Table 4.8 represents the devices parameters for this run.

MC Run	StrongArm Latch
V_{tp}	-581.5mV
V_{tn}	393.6mV

Table 4.8: Threshold voltage for the one MC run, with $V_{DD} = 0.6$V.

The offset before calibration in this case is greater than 300 mV, since the comparator doesn't change its output during the sweep of V_{inp} from 0 to 0.6 V, with V_{inn} fixed at 0.3V. Similar to what was done before the calibration circuit was activated and its behavior is also similar as the presented in the last section. Once the calibration voltage stabilized, a new test to the comparator was performed, represented in figure 4.24.

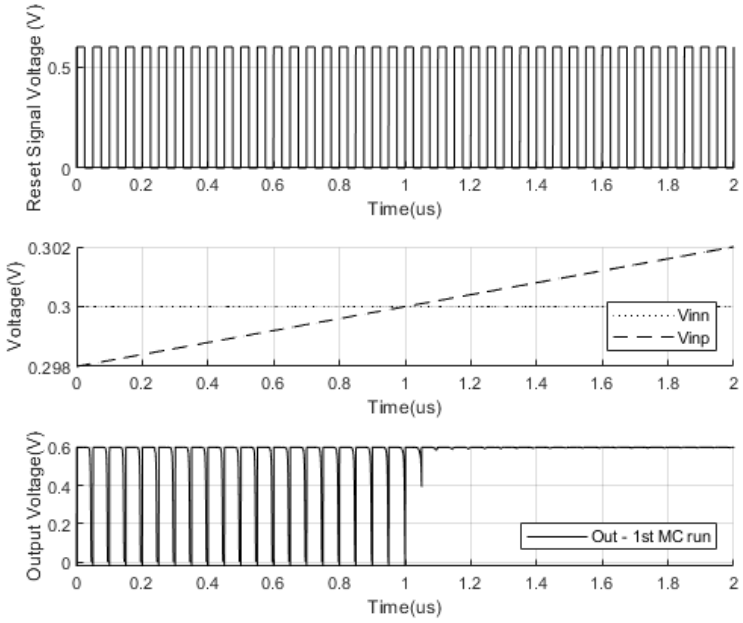

Figure 4.24: Output of the comparator for one MC run, after calibration, with $V_{DD} = 0.6$V.

Again, the circuit started with a very high offset and after the calibration this offset was reduced to a very small value, less than 1 mV. Before calibration this circuit is not able to perform a comparison, but after calibration its response is very similar to the ideal one.

Since this only represents one run, the distribution of offset before calibration and after calibration for all runs can be also seen in figures 4.25 and 4.26, respectively.

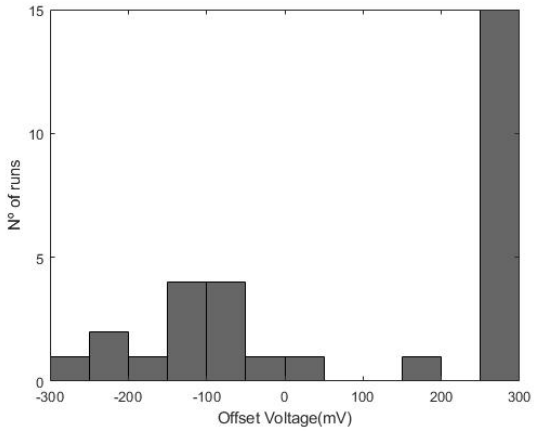

Figure 4.25: Histogram of the offset voltage, before calibration, with $V_{DD} = 0.6$V.

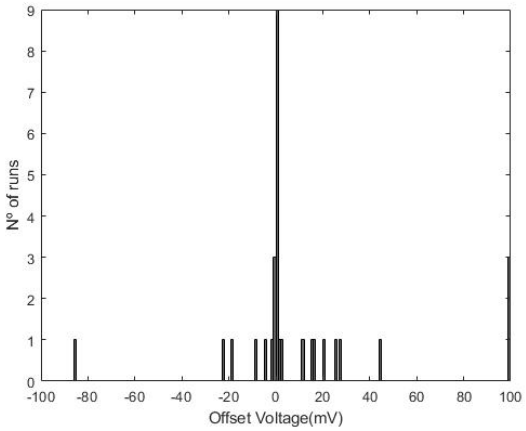

Figure 4.26: Histogram of the offset voltage, before calibration, with $V_{DD} = 0.6$V.

Note: Since $V_{DD} = 0.6$V and one of the inputs is fixed at 0.3 V, if the offset is greater than 0.3 V in either the positive or negative way, no transition from low state to high state happens, and so the offset is represented as if it is 300 mV.

Similar to what happened before the offset is quite significant, reaching values above and below 300 mV multiple times, as it was the case of the run analyzed before.

After calibration, the remaining offset is very small being less than 1 mV in 12 of the 30 cases, showing the capacity of this circuit to correct offset even with a lower supply voltage.

Other very important quantities in a comparator used to measure its performance are presented in table 4.9.

30-MC runs	Mean Value	Standard Deviation	Maximum	Minimum
Supply voltage	0.6V	-	-	-
Sampling Frequency	20MHz	-	-	-
ICMR	[0, 0.6]V	-	-	-
V_{tp}	-367.82mV	63.25mV	-209.4mV	-581.5mV
V_{tn}	421.88mV	68.89mV	656.6mV	253mV
Offset	10.75mV	23.47mV	100	-86
Power P_d	5.357μW	1.3937μW	8.4316μW	2.4176μW
Propagation delay	2.36ns	1.06ns	9.4ns	0.79ns
Sensitivity	13.55mV	18mV	100mV	0.1mV

Table 4.9: Comparator response characteristics for 30-MC runs, with $V_{DD} = 0.6V$.

With this it is possible to calculate the figure of merit for this comparator configuration, equation 4.4.

$$FOM = \frac{P_d}{2^n f_s} = \frac{5,357\mu W}{2^{5bits} * 20MHz} = 8.37fj/conv \tag{4.4}$$

4.5.3 Layout

For the layout, the techniques presented in section 4.3.2 were taken into account. Furthermore, the capacitors were re-design in a L-shape, to guarantee a better area occupation.

The layout for this comparator is presented in figures 4.27 and 4.28, that show the comparator with and without the calibration capacitors, respectively.

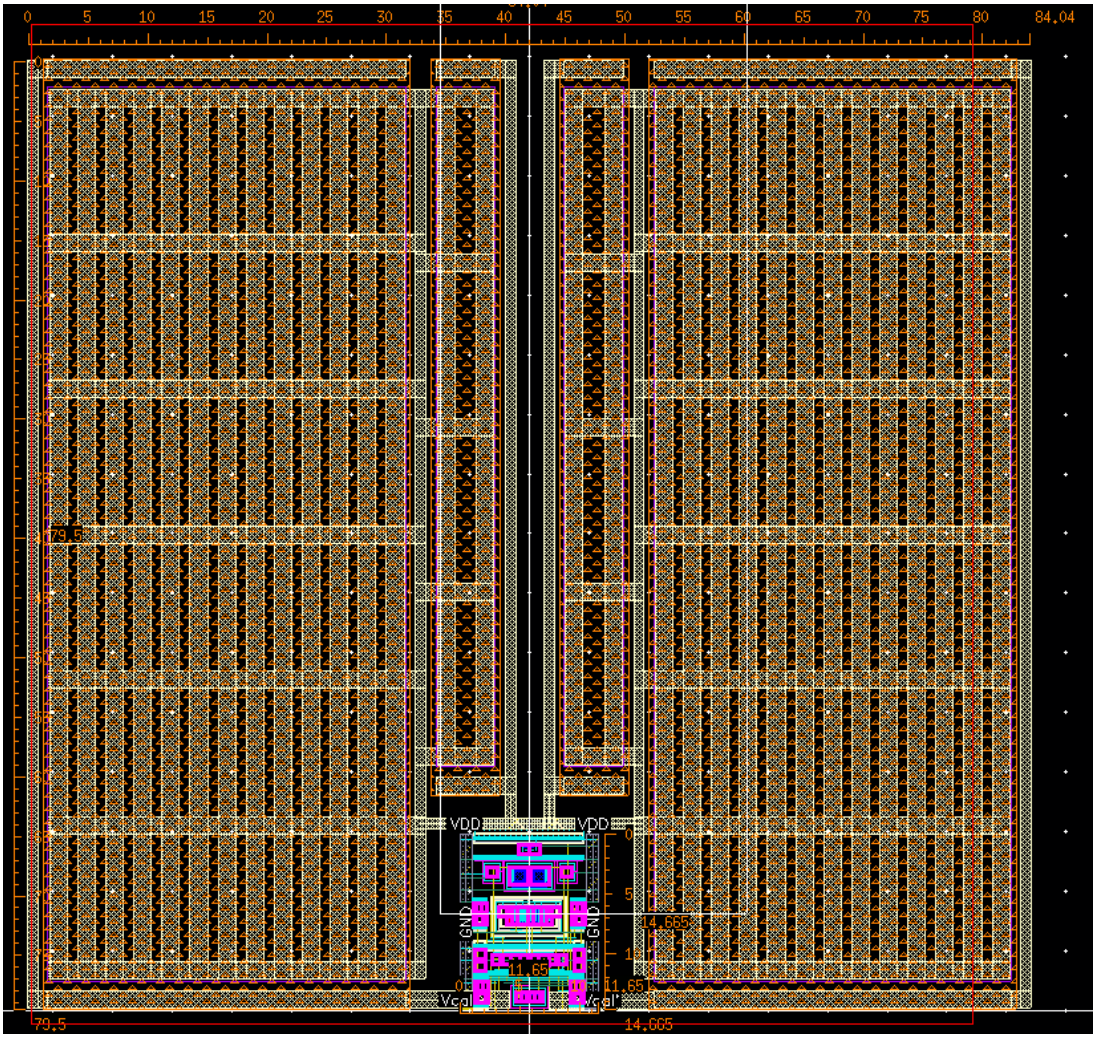

Figure 4.27: Layout of the studied comparator.

Comparing the size of the comparator circuit including the calibration capacitors and excluding these, it can be clearly seen that having a refined offset calibration highly increases the area of the layout. By choosing a smaller dimensions for the calibration capacitors, the area could be significantly decreased but at the cost of definition on the offset cancellation as it can be observed in table 4.2.

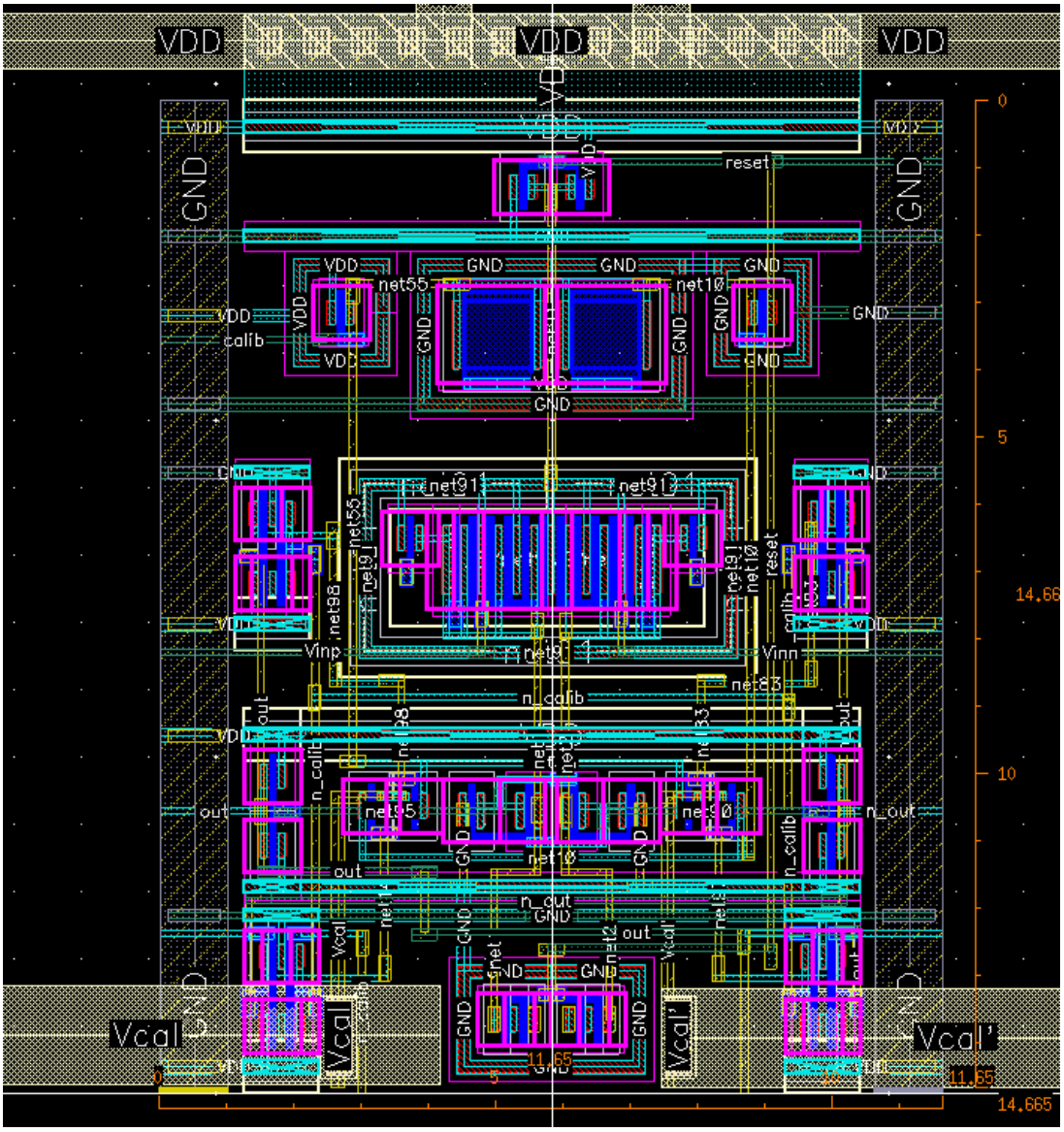

Figure 4.28: Layout of the studied comparator (zoomed in the StrongArm Latch).

Moreover, just the fact of having any calibration circuit is a significant increase in area but that is justified by the results presented in the previous section of this work (depending on the application).

4.6 Comparative study

Although this is a very specific type of comparator that aims to cancel the offset voltage with an external calibration circuit, its overall performance should be analyzed and compared with other implementations and studies.

Table 4.10 shows the most important quantities for different studies, as well as the performed in this

work.

References	[45]	[46]	[47]	[48]	[49]	[12]	This Work	
Technology (μm -CMOS)	0.5	0.35	0.18	0.18	0.6	0.18	0.065	0.065
Supply Voltage (V)	$\pm$1.25	1.2	1.8	1	-	1.8	1.2	0.6
Power P_d (μW)	-	-	225	63.5	750	158.5	88.0	5.357
Sampling Rate (MHz)	-	20	-	20	40	50	1300	20
Resolution (bits)	-	8	8	12	8	8	9	5
Propagation Delay (ns)	932	-	-	26	-	4.2	0.172	2.36
Offset Voltage (mV)	24.2	3	-	0.0476	-	3.44	0.8	10.75
FOM (fj/conv)	-	1.64	15.7	0.77	73.2	0.7	0.1322	8.37
Layout Area (mm^2)	0.086	0.021	0.016	0.008	-	0.008	0.66	0.66

Table 4.10: Comparative study between different articles and this work.

The first thing that has to be referred is that the comparator from this work highly benefits from the smaller technology node when compared to the other studies. It is the smaller node between all of the presented studies, and it could be considered significantly lower. This means that the implemented comparator benefits from lower threshold voltages, which allows a stronger functioning for lower supply voltages, especially important for low power applications. Furthermore, it also reduces the overall devices size which can reduce the layout area (although, it doesn't in this case).

Secondly, taking into account the used supply voltages for the different works as well as the advantage of being implemented in a smaller node, the power obtained is in accordance with the generality of the other studies. By using half of the supply significantly drops but the other quantities are also affected as the frequency, resolution and offset.

Continuing, the frequency in which the comparator is able to correctly perform is also highly affected by the size of the devices and the supply voltage. For a supply voltage of 0.6 V, the speed of this comparator is similar to the other studies, but if a supply voltage of 1.2 V is applied, this circuit is able to perform up to 1.3 GHz.

Regarding the resolution of the comparator of this work when compared with the others, it is worth noting that, it has a very good value. The resolution of this work was obtained from the MC runs, which took into account deviations of 5σ to simulate both factory and radiation induced deviations. For the typical case with 1.2 V, for example, the resolution is 12 bits which is even higher than the presented one. Other quantities like offset, propagation delay, the FOM and, even, the power also account for these deviations.

As for the main objective of this work, it can be seen that the calibration circuit reduces it into very small values. The mean value for 1.2 V of supply voltage is the smallest in the table, even though the deviations were very high. Moreover, the offset voltage is much lower than the presented in a lot of cases

as shown in section 4.5.2. For a supply voltage of 0.6 V, the offset is a bit higher because even with the calibration circuit, there are deviations that can't be correct with it, dooming the offset to be higher in this case.

Through the FOM, it is possible to see that the circuit as a performance within the other studies. For 1.2 V of supply voltage, the best FOM is obtained. However, as said before this circuit benefits from a smaller node which as a huge impact in the overall performance.

Regarding the layout area, it is more than clear the huge difference between the area of this work and other works. This is because the capacitors that compose the calibration circuit need a significant amount of area to have the wanted definition. As said before, this could be reduced but the area of the calibration circuit would always mean a large increase in area.

Lastly, taking the overall performance of this work, it is known that if only the comparator was implemented in this technology node, the presented result could be much better for small deviations. However, this would also mean that for deviations applied in this study the comparator wouldn't work in most cases, and so by sacrificing power, sampling rate, resolution and even FOM, it is possible to obtain a circuit resilient to higher deviations.

Chapter 5

Conclusion

Through this work, in first instance, it was possible to clearly state not only the importance of comparator circuits, but also radiation hardened circuits. Comparators are widely used in ADCs which are the essential unit that turns the real world to a digitized world. Moreover, radiation applications always had a huge interest in the scientific community, and this interest tendency is to increase even more. Adding to all this, with the reduction of technology nodes and the need avoid power hungry circuits, low-power circuits and applications have a huge interest.

In order to implement this comparator, two topologies were considered, being this the StrongArm Latch Comparator and the Double Tail comparator. As the objective was to cancel the offset, some calibration techniques were considered. In the end the combination that provided the best results was a similar implementation as done in [39].

Imposing a deviations that would account for 99.7% of the fabricated devices plus the radiation induced deviations, some simulation to the comparator performance were performed for both 1.2 V and 0.6 V of supply voltage. The results obtained confirm that this calibration circuit is capable of correcting huge amounts of offset. However, there are also deviations that can't be corrected by the calibration circuit.

When comparing this work with other studies, it was possible to frame these results within other comparators. It could be concluded that the calibration circuit means trading a possible faster and better solution for a more resilient one with the capability of correcting the offset voltage to acceptable values and keep a good performance overall.

Lastly, the implemented comparator was analyzed in a generic way and through this analysis it can be concluded that this implementation provides a solid solution for comparator with low offset during all its lifespan, since the calibration also accounts for aging. Naturally, when analyzing a specific application, other design choices could be taken making the comparator faster, more precise or with even less power but this always means sacrificing some quantities to improve others.

Regarding future work on this subject, deeper analysis as post-layout simulations can be performed to the comparator, other radiation models can be deduced and used in order to close even further the

distance between model and reality, and ultimately, the circuit can be printed and studied under real radiation to verify its operation.

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Appendix A

Foreground calibration vs Background calibration

Voltage offset calibration is essential either at comparator level, ADC level or in any other circuit that requires a precise comparison. This calibration can be performed in "foreground" or "background", depending on if the output data stream has to be interrupted or not in order to perform the calibration.

Foreground calibration requires that, for a short period of time, known entries are forced in the converter, forcing a known state, and its output is taken off-line so that the deviations relative to a reference can be detected and corrected. Normally, this kind of corrections is applied by an analog feedback DAC or through a digital post-processing step. Regarding the reference input signal used, this can either be static, i.e., short circuiting the inputs to measure differential offset, or a step of known values that stimulate multiple codes. This kind of calibrations is performed and advantageous in situations where the input signal is not known or may have an unpredictable behavior. On the other hand, this requires a temporary loss of data/non-functioning of the circuit to perform the calibration. In [50], a foreground calibration algorithm that by creating and using a look-up-table(LUT), estimates and corrects memoryless nonlinear impairments in both single channel and time-interleaved analog-to-digital converters (TIADCs) is presented. In a similar way, [51] and [53] describe a foreground calibration technique that finds and stores calibration coefficients used in normal operation.

Background calibration corrects various source of mismatch without the need to stop the output data stream. A simple way to perform this calibration is to rely on statistical properties of the input signal and average, compare and extract errors from the outputs, e.g., for an analog input that represents a beat frequency of the same clock, the output will eventually be the same and that way any deviation from the average can be corrected. Other way to perform this calibration is to add redundancy to the circuit, allowing units to be in calibration while the others assure the output. There are other techniques that perform background offset cancellation either by digital or analog means, some of them are explored in [54], [55], [56] and [13]. The advantages of this type of calibration are not just the non-interrupting output

data stream as it can correct deviations due to time, temperature, or supply variation. The downside is that it can rely on more area usage, have a slower convergence or more power consumption.

The comparator considered in the thesis work allows for background calibration even having to stop its functioning to calibrate, as long as in the cycles used for calibration, a comparison is not needed.

Appendix B

Double-tail Comparator with Offset Calibration

As an alternative to the studied comparator, a Double-Tail Comparator topology with the self-calibration circuit from [39] was implemented. The implemented scheme is presented in figure B.1.

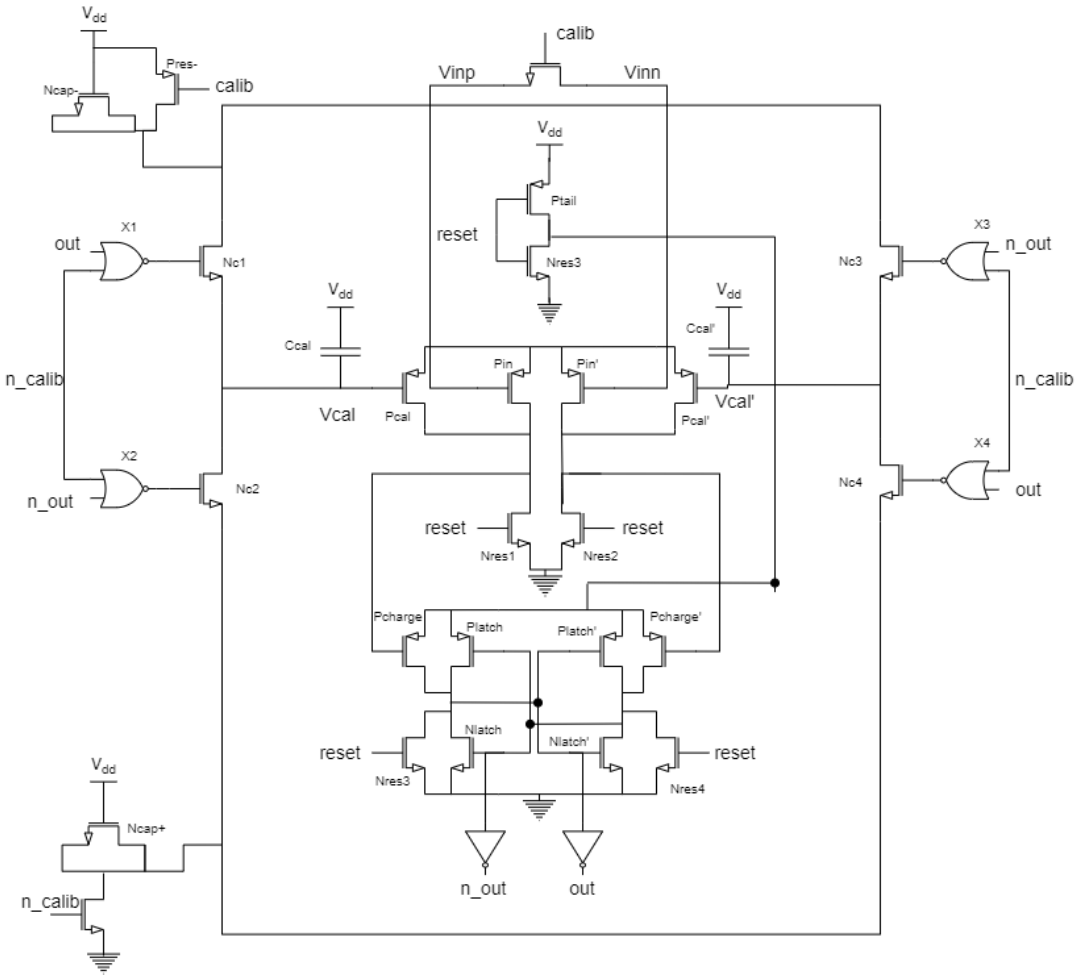

Figure B.1: Double tail latch comparator with offset calibration.

Having the pre-amplifier stage separated from the latch stage, has the benefit of having the possibility to apply a high tail current in the latch and a small one in the pre-amplifier stage, hence reducing the offset. Since this circuit is supposed to have really high offset voltages and being able to compensate them with an external calibration circuit, this advantage is less significant.

This topology also as a higher voltage headroom which could mean higher speed.

B.1 Sizing.

As it was done for the StrongARM Latch topology, the sizing of the devices that compose this circuit was also performed with speed as the main objective.

The behavior of most transistors is exactly the same as the competitor topology, so it comes with no surprise that the sizing that provides the best speed is exactly the same.

The implemented sizing is presented in table B.1.

Device	**Width**	**Length**
P_{res-}, N_{res+}, N_{c1-4} and N_{res1-4}	350nm	60nm
Inverter and Nor gates	350nm	60nm
P_{cal} and P'_{cal}	350nm	60nm
P_{in} and P'_{in})	5μm	60nm
P_{latch}, P'_{latch}, N_{latch} and N'_{latch}	500nm	60nm
N_{cap-} and N_{cap+}	1μm	1μm
C_{cal} and $C_{cal'}$	50μm	50μm

Table B.1: Sizing choices.

B.2 Characterization.

The behavior of this topology was checked both with 1.2V and 0.6V of supply voltage, as it was the case for the StrongARM topology. The first check to perform was to the frequency to which this comparator could functioning maintaining the wanted behavior. Figures B.2 and B.3 represent the response of this circuit near the transition points.

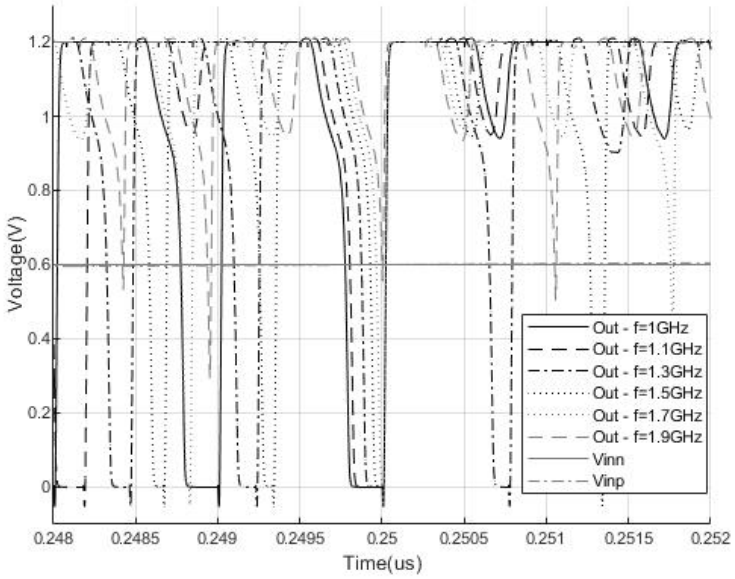

Figure B.2: Output of the comparator for different frequencies, with $V_{DD} = 1.2$V.

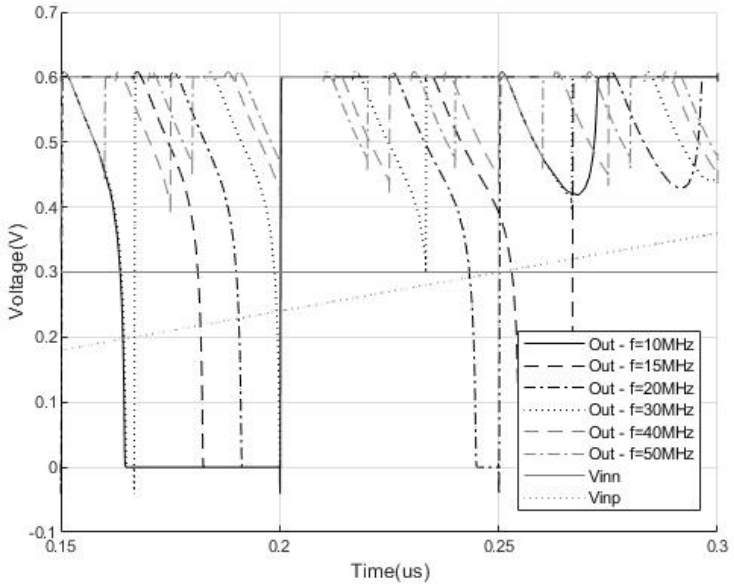

Figure B.3: Output of the comparator for different frequencies, with $V_{DD} = 0.6$V.

Through this images, and when comparing with 4.15 for the other case, it is possible to see that this response can't work at a higher sampling rate, and even has a lot more of uncertainty in the transition zone.

Although it is not represented, for the complete voltage difference sweep, these errors in certain zones,

especially in the transition zone and to input voltages higher than $V_{DD} - V_t$, were really significant.

The main difference from the StrongARM Latch comparator is that, in this case, the calibration current that comes from the calibration PMOS charges the gate of the latch transistor instead of its source. Hence, any small deviations in the calibration have a much higher impact in the circuit, especially if the differential pair enters in sub-threshold region, and so this implementation is not as consistent.

Further testing was only performed to the StrongARM Latch Comparator, since in this case is a more suitable design.

Appendix C

Details of the MC Simulations

This section presents more details on the MC simulations.

C.1 Supply voltage 1.2 V

Run	V_{tp}	V_{tn}	Offset Before Calibration	Offset After Calibration	Power	Sensitivity	Propagation Delay
1	-581,5	393,6	600	0,2	91,164	0,1	0,1867
2	-315,3	318,3	600	0,5	89,437	0,3	0,1808
3	-410,9	451,2	-230	1	84,887	2,5	0,1424
4	-340,5	422,4	600	2,2	102,47	0,2	0,1422
5	-444,5	656,6	-278	-3,2	91,163	5,4	0,2104
6	-385,7	483,2	600	-0,3	104,88	0,1	0,1255
7	-281,6	359,3	-51	0,3	81,379	1,3	0,2129
8	-352	436,6	600	2,2	101,3	6,8	0,1439
9	-471,6	283,3	600	4,2	81,56	1,7	0,1929
10	-397,7	502,4	600	0,8	88,44	0,1	0,134
11	-300,2	378,2	-294	-1,2	84,687	0,1	0,1963
12	-232,8	408,2	-400	-0,3	88,447	4,3	0,2069
13	-328,5	342,2	600	0,4	68,752	0,1	0,2188
14	-425,9	466,5	-139	-0,1	90,933	1,5	0,1857
15	-346,3	474,6	-196	3,2	98,367	2,7	0,1611
16	-456,4	352,2	600	-0,5	81,774	0,1	0,1527
17	-391,6	415,3	600	1	92,011	0,5	0,1737
18	-291,5	589,3	-184	2	89,648	3,5	0,1655
19	-368,7	386,1	-340	-0,4	99,582	2	0,1426
20	-209,4	513,4	600	-0,5	83,668	0,5	0,198
21	-322,1	303,1	-68	1,5	98,647	0,1	0,1435
22	-418,1	443,8	600	-0,1	73,391	0,1	0,1784
23	-379,9	370,1	600	0,4	87,357	0,1	0,1635
24	-248,2	492,4	-475	-1,1	78,997	6	0,2299
25	-334,6	253	-81	1,5	88,389	0,1	0,1443
26	-434,6	429,5	600	0,7	76,597	0,2	0,1576
27	-357,5	458,7	600	2	99,667	0,5	0,154
28	-494,8	331	11	0,2	68,306	0,1	0,1812
29	-404,1	401	600	0,1	100,38	0,1	0,1412
30	-308,1	541	600	7,6	74,612	14,7	0,1943

Table C.1: Results of the 30-MC runs, with $V_{DD} = 1.2$V

C.2 Supply voltage 0.6 V

Run	V_{tp}	V_{tn}	Offset Before Calibration	Offset After Calibration	Power	Sensitivity	Propagation Delay
1	-581,5	393,6	300	-0,1	5,5828	0,1	1,26
2	-315,3	318,3	300	25	5,551	0,1	2,41
3	-410,9	451,2	-142	-2	4,3145	16	1,25
4	-340,5	422,4	300	100	6,2588	100	1,03
5	-444,5	656,6	152	-19	5,8774	9	3,83
6	-385,7	483,2	300	2	7,5897	1	0,79
7	-281,6	359,3	-125	-0,4	3,4191	21	2,395
8	-352	436,6	300	100	6,8763	100	1,62
9	-471,6	283,3	300	20	3,5654	1	2,34
10	-397,7	502,4	-60	-23	8,4316	13	2,54
11	-300,2	378,2	-203	-4,5	4,6229	1	2,74
12	-232,8	408,2	300	0,2	4,6106	0,1	1,98
13	-328,5	342,2	-80,5	0,5	2,6273	1,5	2,66
14	-425,9	466,5	-139	-8,2	7,2252	10	1,21
15	-346,3	474,6	300	-0,1	4,7452	0,1	2,25
16	-456,4	352,2	300	0,1	6,5903	0,1	1,86
17	-391,6	415,3	-200	11,5	6,5302	2	2,66
18	-291,5	589,3	-216	-86	3,6571	5	1,51
19	-368,7	386,1	300	16	4,4613	1	2,46
20	-209,4	513,4	-134	15,1	6,6257	0,5	2,08
21	-322,1	303,1	300	27,4	3,7923	2	2,25
22	-418,1	443,8	300	0,4	4,8054	0,1	3,75
23	-379,9	370,1	-300	44,5	4,2102	15	7
24	-248,2	492,4	-66,5	0,5	6,2588	0,1	1,07
25	-334,6	253	300	0,6	6,1225	4	1,86
26	-434,6	429,5	300	1,3	7,1171	1	0,91
27	-357,5	458,7	-26	0,1	2,8409	0,1	1,71
28	-494,8	331	47,5	0,1	5,8976	0,1	1,22
29	-404,1	401	300	100	2,4176	100	9,4
30	-308,1	541	-86	0,4	8,078	1,5	0,88

Table C.2: Results of the 30-MC runs, with $V_{DD} = 0.6$V.