Radiation Hardened Comparator

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***Abstract*—Comparators are an essential unit in many circuits, one of them being ADCs which are the electronic bridge between the real world and the digitized world. Adding to this fact, both low-power circuits and radiation hardened circuits are scientific areas with high and increasing interest. Knowing the importance that a radiation hardened comparator has, especially prepared for low-power, in this work the objective is to implement a comparator with an offset cancellation technique capable of reducing its natural offset aggravated by radiation, during all its life cycle. To do the proposed, some alternatives of comparator and calibration circuits were analyzed. The chosen comparator topology was the StrongARM Latch to which a calibration scheme that works through charge transfer was added. Recurring to a Monte-Carlo Simulation with 5σ that accounts for fabrication (3σ) and radiation deviations (2σ), the circuit response was tested for both a comparator with 1.2 V of supply voltage working at 1.3 GHz and for a comparator working with 0.6 V of supply voltage at a speed of 20 MHz. The offset was significantly reduced in both cases, in most tests being able to turn an unusable comparator into a comparator with less than 0.1 mV of offset. The offset calibration significantly reduces the offset that is natural and imposed to the circuit, providing a very good solution for circuits subject to radiation.**

***Index Terms*—Comparator, Low-power, StrongARM Latch, Radiation-Hardened, Offset Cancellation, CMOS**

I. Introduction

A. Context and Motivation

Comparators are widely used especially in circuits that measure and digitize analog signals, namely analog-to-digital converters (ADCs), relaxation oscillators, memory sense amplifiers (SAs) and data receivers. This type of devices is the bridge between the real world and the digitized world. Hence, they have a huge importance.

Other topic that has a great interest and has been gaining even more is low-power applications. With the growth in demand for portable devices, wireless communication, consumer electronics, medical equipment, and topics such as edge-IoT, low-power circuits are becoming even more a research focus. ADCs with reduced transistor sizes, low-power dissipation and decreased propagation delay are essential for this kind of application with the comparator has a key element to satisfy these conditions.

Since comparators are decision-making circuits, their accuracy, which is commonly determined by its input-referred offset voltage, determines the resolution of high-performance ADCs. Furthermore, a faster and accurate comparator involves high gain and high bandwidth, therefore, dynamic latch comparators are used instead of static comparators, provide high-speed, low-power consumption, high-input impedance, and full-swing output, benefiting from the positive feedback.

Moreover, radiation is also a huge field of interest in scientific research. Radiation affects not only living beings, but also circuits normal operation. When subject to radiation, circuits deteriorate, changing permanently their characteristic. This degradation usually occurs due to the interaction between an impinging particle (proton, photon, heavy ion, electron, pion etc.) and the materials building the device. The type of damage is directly related to the energy of the particle and their relative ionizing proprieties. It is possible to describe this circuit degradation as a variation of the normal parameters of a MOS device, the threshold voltage(V_t) and the current factor(β).

Joining all these factors, it is clear the interest in designing a radiation hardened comparator cannot be overstated.

The main aim of the work presented in this paper is to design and test a radiation hardened comparator based on the StrongARM Latch topology and the calibration circuit employed in [1].

B. Natural and Radiation Mismatches

Starting by the natural deviations that the fabrication process imposes, these are usually described by their simplified models present in equations 1 and 2.

$$var(\Delta V_t) = \sigma_{Vt}^2 = \frac{A_{Vt}^2}{WL} \tag{1}$$

$$var(\frac{\Delta\beta}{\beta}) = \sigma_{\beta}^2 = \frac{A_{\beta}^2}{WL} \tag{2}$$

Regarding radiation, there are two main types of effects on circuits, them being cumulative effects and single-event effects. Cumulative effects can be divided into displacement damage dose (DDD), generated by big particles, and total ionizing dose (TID) caused either by photons, or by charged particles. TID is the type of effect of interest in this work since it leads to variations in transistors parameters.

The radiation induced deviations are based on the worst deviation presented in [4], expressed in their absolute value and in how many standard deviations they represent.

The total deviation considers 3σ for the fabrication process which includes 99.7% of total fabricated devices and adds the deviation imposed by radiation.

Although, radiation can produce a change in the current factor around 3%, both the ON current and the offset voltage

TABLE I
STANDARD AND RADIATION DEVIATIONS ON PARAMETERS THAT SUFFER FROM MISMATCHES.

Parameter	W/L ($\mu m/\mu m$)	Typical	A_{vt}	σ	Radiation Deviation	Total Deviation
Vt_{NMOS}	0.35/0.06	422.7mV	3,5mV/μm	24.15mV	9mV = 0.37σ	$3.37sigma$
β_{NMOS}	0.35/0.06	-	-	-	1.44%	-
Vt_{PMOS}	0.35/0.06	-363.2mV	2,0mV/μm	13.80mV	21mV = 1.52σ	4.52σ
β_{PMOS}	0.35/0.06	-	-	-	3.0625%	-

are strongly affected by the V_t variation, and so the deviations applied to the circuit when tested will be 5σ considering both type of deviations.

II. RADIATION HARDENED COMPARATOR

A. Taimur Rabuske et al., 2015

In [1], a very low-power background calibration technique to nullify the comparator offset caused by process, voltage, and temperature (PVT) is presented.

The comparator circuit is composed by a Strong-Arm latch dynamic comparator [3] combined with differential offset calibration circuits (presented in figure 1).

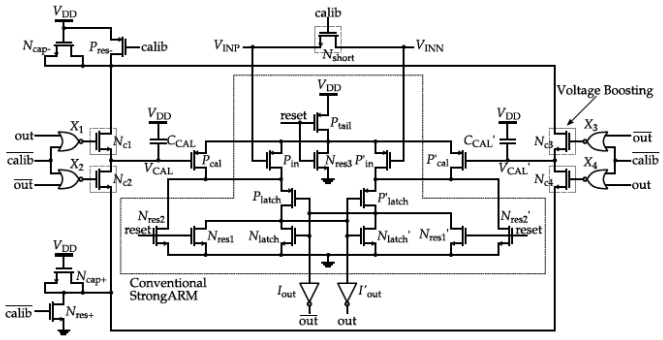

Fig. 1. StrongARM latch with offset cancellation from [1].

In this circuit, the difference between inputs drives a differential current which activates the latches, leading to positive feedback that brings one output to 0 and the other to VDD.

The calibration process in this circuit increases or reduces VCAL by a small step $\Delta VCAL$ until the offset is cancelled or the calibration process ends. This technique works in the following way (as described in [1]):

1) With C_{CAL} and $C_{CAL'}$ initially discharged, V_{CAL} and $V_{CAL'}$ are at VDD, and since P_{CAL} and $P_{CAL'}$ are cut-off, they have a reduced effect on the calibration threshold. Also since "calib" is '0', P_{res-} and N_{res+} are ON and that way N_{cap-} is discharged to ground and N_{cap+} is charged to VDD.
2) When "calib" turns to "1" (indicating a calibration sequence), N_{short} shorts the inputs V_{INP} and V_{INN}, making the differential voltage from the comparator equal to 0. When the inputs have stabilized, a comparison is requested by pulling down the "reset" signal and the obtained results (a digital "0" and "1") are used, jointly with the fact that "not calib" is "0" to identify which is the lower and the higher side (one MOS switch among N_{c1} and N_{c2} and one MOS switch among N_{c3} and N_{c4} are closed).
3) In the last part of the calibration process, part of the charge stored in N_{cap+} is redistributed to C_{CAL} or $C_{CAL'}$ and part of the charge stored in C_{CAL} or $C_{CAL'}$ is lost to N_{cap+}. This reduces the voltage of the slower branch, V_{CAL} or $V_{CAL'}$, increasing the current in P_{CAL} or $P_{CAL'}$. Since this circuit works with negative feedback, the comparator offset is reduced and with enough cycles cancelled. The process can be stopped when the output starts oscillating between "0" and "1", which means that the minimum step was reached. However, if continuously performed it corrects PVT errors on-the-fly.

B. Supply voltage 1.2 V

Following the presented table I, it can be assumed that 5σ of total deviation would account for both deviations and so a 30-Monte Carlo simulation was performed to obtain the circuit response under this circumstances. With an operating frequency established as 1.3 GHz.

Before analysing the overall performance of the circuit in the 30 - MC runs, one run was chosen to analyse the calibration process in more detail.

Figure 2 shows the comparator output without calibration.

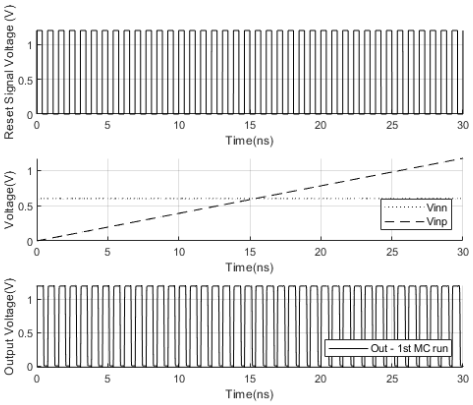

Fig. 2. Output of the comparator for one MC run, before calibration, with $VDD = 1.2$V.

Tthere is a significant increase in the offset voltage. So much significant that by analysing the figure 2, it can be seen that the comparator only outputs a '0', meaning that no comparison is being performed. It can be concluded that the offset for this situation is greater than 600 mV since no transition is seen for any $V_{inp} - V_{inn}$.

To try to correct this offset, the calibration circuit was activated. Short-circuiting the inputs of the comparator and using the output to detect the unbalance, the calibration capacitors were charged until the offset was corrected. They rapidly obtain a significant difference that contradicts the offset. After

that, knowing that the calibration period is still active, the circuit keeps reducing the offset to the maximum possible, previously defined.

The output after calibration for the same run as in figure 2, is represented in figure 3.

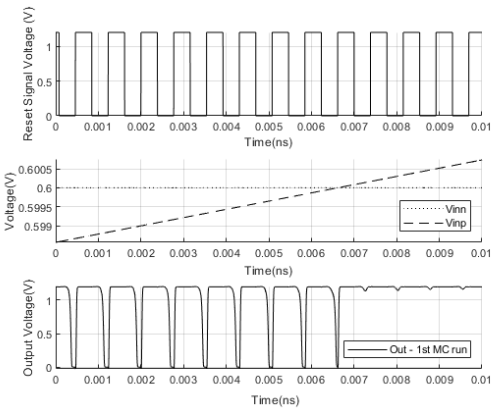

Fig. 3. Output of the comparator for one MC run, after calibration, with $VDD = 1.2$V.

Through this graphic, it is clear how strong this calibration circuit is. The pre-calibration offset was greater than 600 mV and after calibration it's smaller than 0.1 mV.

Since this only represents one MC run, the distribution of the offset before and after calibration for all runs can be also seen in figures 4 and 5, respectively.

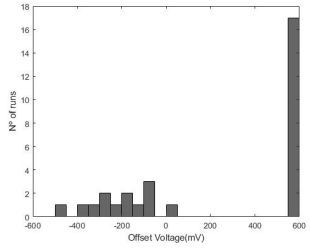

Fig. 4. Histogram of the offset voltage, before calibration, with $VDD = 1.2$V.

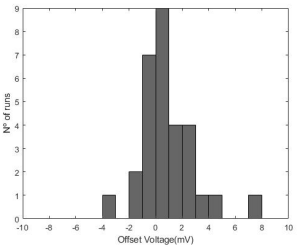

Fig. 5. Histogram of the offset voltage, before calibration, with $VDD = 1.2$V.

Before calibration, the offset is quite significant, reaching values above or below 600 mV multiple times, as it was the case of the run analyzed before. Even for the offset values closer to 0 V, the minimum offset voltage obtained was 11 mV, and so it is clear that this shift completely changes the comparator behavior which can dictate the inoperability of this circuit.

After calibration, in most of the cases, the offset is almost totally cancelled. Not only to values under 8 mV, as is the case for all performed tests, but also to values under 1.5 mV, as is the case for 22 of these.

The offset is a very important factor, however, there are also some other very important quantities in a comparator used to measure its performance, which are presented in table II.

TABLE II
COMPARATOR RESPONSE CHARACTERISTICS FOR 30-MC RUNS, WITH $VDD = 1.2$V.

30-MC runs	Mean Value	Standard Deviation	Maximum	Minimum
Supply voltage	1.2V	-	-	-
Sampling Frequency	1.3GHz	-	-	-
ICMR	[0, 1.2]V	-	-	-
V_{tp}	-367.82mV	63.25mV	-209.4mV	-581.5mV
V_{tn}	421.9mV	68.89mV	656.6mV	253mV
Offset	0.8mV	1.3mV	7.6mV	-3.2mV
Power P_d	88.0μW	7.9μW	104.9μW	68.3μW
Propagation delay	0.172ns	0.024ns	0.230ns	0.1174ns
Sensitivity	1.9mV	2.1mV	14.7mV	0.1mV

C. Supply voltage 0.6 V

The operating frequency of the circuit, in this case, was established as 20 MHz. The distribution of offset before calibration and after calibration for 30-MC runs can be seen in figures 6 and 7, respectively.

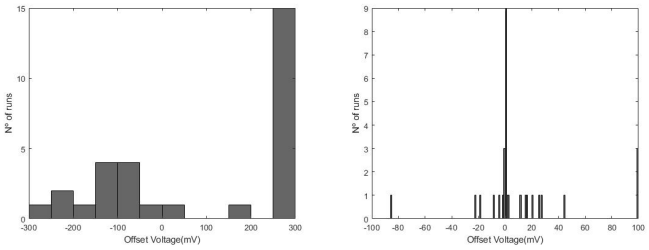

Fig. 6. Histogram of the offset voltage,before calibration, with $VDD = 0.6$V.

Fig. 7. Histogram of the offset voltage, before calibration, with $VDD = 0.6$V.

Similar to what happened before the offset is quite significant, reaching values above or below 300 mV multiple times.

After calibration, the remaining offset is very small, being less than 1 mV in 12 of the 30 cases, showing the capacity of this circuit to correct offset even with a lower supply voltage.

Other very important quantities in a comparator used to measure its performance are presented in table III.

TABLE III
COMPARATOR RESPONSE CHARACTERISTICS FOR 30-MC RUNS, WITH $VDD = 0.6V$.

30-MC runs	Mean Value	Standard Deviation	Maximum	Minimum
Supply voltage	0.6V	-	-	-
Sampling Frequency	20MHz	-	-	-
ICMR	[0, 0.6]V	-	-	-
V_{tp}	-367.82mV	63.25mV	-209.4mV	-581.5mV
V_{tn}	421.88mV	68.89mV	656.6mV	253mV
Offset	10.75mV	23.47mV	100	-86
Power P_d	5.357μW	1.3937μW	8.4316μW	2.4176μW
Propagation delay	2.36ns	1.06ns	9.4ns	0.79ns
Sensitivity	13.55mV	18mV	100mV	0.1mV

D. Layout

The layout for this comparator is presented in figure 8.

It can be clearly seen that having a refined offset calibration highly increases the area of the layout. By choosing a smaller dimensions for the calibration capacitors, the area could be significantly decreased but at the cost of definition on the offset cancellation.

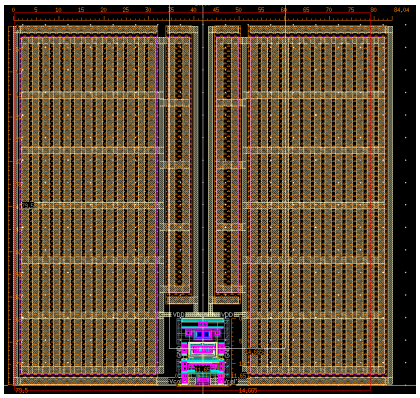

Fig. 8. Layout of the studied comparator.

E. Comparative study

Although this is a very specific type of comparator that aims to cancel the offset voltage with an external calibration circuit, its overall performance should be analyzed and compared with other implementations and studies.

Table IV shows the most important quantities for different studies, as well as the performed in this work.

TABLE IV
COMPARATIVE STUDY BETWEEN DIFFERENT ARTICLES AND THIS WORK.

References	[5]	[6]	[7]	[8]	[9]	[2]	This Work	
Technology (μm -CMOS)	0.5	0.35	0.18	0.18	0.6	0.18	0.065	0.065
Supply Voltage (V)	$\pm$1.25	1.2	1.8	1	-	1.8	1.2	0.6
Power P_d (μW)	-	-	225	63.5	750	158.5	88.0	5.357
Sampling Rate (MHz)	-	20	-	20	40	50	1300	20
Resolution (bits)	-	8	8	12	8	8	9	5
Propagation Delay (ns)	932	-	-	26	-	4.2	0.172	2.36
Offset Voltage (mV)	24.2	3	-	0.0476	-	3.44	0.8	10.75
FOM (fj/conv)	-	1.64	15.7	0.77	73.2	0.7	0.1322	8.37
Layout Area (mm^2)	0.086	0.021	0.016	0.008	-	0.008	0.66	0.66

The first thing that must be referred is that the comparator from this work highly benefits from the smaller technology node when compared to the other studies. It is the smaller node between all of the presented studies, and it could be considered significantly lower. This means that the implemented comparator benefits from lower threshold voltages, which allows a stronger functioning for lower supply voltages, especially important for low power applications.

On a second notice, by using half of the supply, the power significantly drops but the resolution and speed of the circuit are also affected. It should be noticed that even with 5σ, the correct operation of the comparator is guaranteed, and both the speed and the resolution have good values.

Lastly, taking the overall performance of this work, it is known that if only the comparator was implemented in this technology node, the presented result could be much better for small deviations. However, this would also mean that for deviations applied in this study the comparator wouldn't work in most cases, and so by sacrificing power, sampling rate, resolution and FOM, it is possible to obtain a circuit resilient to higher deviations.

III. CONCLUSION

Through this work, in first instance, it was possible to clearly state not only the importance of comparator circuits, but also radiation hardened circuits.

Furthermore, imposing deviations that would account for 99.7% of the fabricated devices plus the radiation induced deviations, some simulation to the comparator performance were performed for both 1.2 V and 0.6 V of supply voltage. The results obtained confirm that this calibration circuit is capable of correcting huge amounts of offset.

Moreover, when comparing this work with other studies, it was possible to frame these results within other comparators. It could be concluded that the calibration circuit means trading a possible faster and better solution for a more resilient one with the capability of correcting the offset voltage to acceptable values and keep a good performance overall.

Lastly, the implemented comparator was analyzed in a generic way and through this analysis it can be concluded that this implementation provides a solid solution for comparator with low offset during all its lifespan, since the calibration also accounts for aging. Naturally, when analyzing a specific application, other design choices could be taken making the comparator faster, more precise or with even less power but this always means sacrificing some quantities to improve others.

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