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Sub-1V Bandgap Voltage Reference Circuit and Voltage to Current Converter

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

Acknowledgement

There are many people that I would like to acknowledge. To my supervisors through this work Prof. Jorge Manuel dos Santos Ribeiro Fernandes and Dr. Taimur Gibran Rabuske Kuntz for the guidance and support. Their knowledge, experience and patience was an important factor to complete this work. My gratitude to INESC-ID for the provided tools, and more specifically to the group i have had the pleasure to meet and to work with for the availability to help whenever necessary.

Finally, to my family and friends for the continuous support throughout the whole process to obtain this degree.

Abstract

This thesis explores the design steps of a Bandgap Voltage Reference (BGR) circuit and a voltage to current converter, implemented in one system. Both circuits are crucial blocks for high performance and reliable circuits, with a wide range of applications in many fields from analog to digital circuits. This work contemplates the design of the various sub-circuits which integrates both the BGR circuit and the voltage to current converter, including trimming sections, to improve the performance in all conditions that the system might be exposed to.

The system was designed in a 180 nm conventional CMOS process technology. In the case of the BGR circuit, simulated results have shown temperature coefficients as low as 20.8 ppm/°C over a temperature range of 165 °C (-40 °C to 125 °C). Additionally, the circuit displays a PSRR of -45.7 dB at low frequencies and -39 dB at 1 MHz. The converter circuit presents a process corners current variation of 3.2 %, for the same temperature interval. The system current consumption is 137.1 μA.

Keywords

CMOS, Reference Voltage, Reference Current, Matching, Resistor Trimming.

Resumo

Esta tese de mestrado explora o projecto de um "Bandgap Voltage Reference" (BGR) e de um conversor de tensão para corrente, implementados no mesmo sistema. Ambos os circuitos são blocos cruciais para circuitos alto desempenho e fiáveis, com aplicações em diferentes áreas, desde circuitos análogos até digitais. Este trabalho contempla a criação dos variados blocos que integram o circuito BGR e o conversor de tensão para corrente, incluindo secções de ajuste, de maneira a melhorar o desempenho para todas as condições de funcionamento a que o sistema poderá estar exposto.

O sistema foi projetado numa tecnologia convencional CMOS de 180 nm. No caso do circuito BGR, os resultados por simulação demonstram um coeficiente de temperatura tão baixo quanto 20.8 ppm/°C para um intervalo de temperatura de 165 °C (-40 °C a 125 °C). Adicionalmente, o circuito apresenta um PSRR de -45.7 dB para baixas frequências e -39 dB a 1 MHz. O circuito conversor apresenta uma variação de corrente em "corners" de 3.2 %, para o mesmo intervalo de temperatura. O consumo de corrente do sistema é 137.1 μA.

Palavras-chave

CMOS, Tensão de Referência, Corrente de Referência, Emparelhamento, Ajuste Resistivo.

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Acronyms

BGR	Bandgap Voltage Reference
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Contrary To Absolute Temperature
DECAP	Decoupling Capacitor
DRC	Design Rule Checking
GND	Ground
IC	Integrated Circuit
I_{REF}	Current Reference
LR	Line Regulation
LVS	Layout Vs Schematic
MIM	Metal Insulator Metal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
PEX	Parasitic Extraction Tool
PMOS	P-type Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PTAT	Proportional To Absolute Temperature
PVT	Process variation, Voltage and Temperature
TC	Temperature Coefficient
VDD	Circuit Supply Voltage
V_{REF}	Voltage Reference

Contents

1. Introduction

In the field of electronics, the circuits always consist of different blocks, each one with a specific function that performs a desired task when working together. A very important block, and one of the most used, is the reference block. This reference block is responsible for generating accurate DC voltages and current, independent of variations in the process manufacturing, supply voltage and temperature (PVT).

The evolution seen in the field of electronics is immense, especially during the 20th century. Reference blocks performance and reliability developed consequently, with the creation of new topologies, techniques or just by adding different devices. Nowadays, the reference block is essential in almost every electronic equipment, them being control systems, supply sources and others.

1.1 Work Objectives

The system to be implemented takes part in a bigger project, developed by a group from INESC-ID. It was asked to develop two reference circuits, one is a voltage reference circuit and the other a current reference.

The system is supplied by a voltage of 1.8 V. The reference voltage desired value is 900 mV, and presenting a total variation in the process corners below 5 % in the temperature range of 165 °C (-40 °C to 125 °C). The reference current desired value is 1 μA, with a similar variation in the same temperature interval. These are the main goals to be achieved, the rest of the performance measures are expected to deliver acceptable results.

The technology selected is the complementary metal oxide semiconductor, or CMOS, in 180 nm. CMOS is a type of metal oxide semiconductor field effect transistor (MOSFET) fabrication process that uses complementary and symmetrical pairs of transistors to perform logic functions, and also used for constructing integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips, and other digital logic circuits. CMOS devices work over a temperature range of –55 °C to 125 °C. The helping tools used are the Cadence software for the design and implementation, and after that, the Calibre software for the layout design and extraction. The following goals are set for this project:

- Analyse the state of the art related to each circuit that forms the system, choosing an architecture for each block.
- Design schematics for those blocks using the technology related to the design kit provided, with Cadence software.
- Define the important measures of each block and create the respective simulation benches.
- Validate the schematic using the various simulation benches.
- Design the layout of the validated schematic.
- Validate the layout with Calibre software, such as DRC and LVS.
- Extract and simulate the layout created, and corroborate the results.

1.2 Document Organization

This document is composed by eight chapters, with the introduction being the first one. The chapter 2 presents the background of bandgap voltage reference circuits, as well as a glimpse of the current reference topologies studied.

The chapters 3 and 4 explain the blocks used and designed in the BGR circuit and the voltage to current converter circuit, respectively.

In the chapter 5, the analyses and simulations performed are talked about, followed by the schematic results of the system. The chapter 6 describes the steps taken in the layout design, and presents the system layout.

The chapter 7 displays the post-layout results of the designed system, as well as a comparison with other similar works. The eighth and last chapter shows the final conclusion of this project and discusses future work.

2. Background and Motivation

2.1 Voltage Reference Circuit

The voltage reference circuit is a system that generates a constant output voltage, which in theory, does not depend on the operating voltage, load current, temperature, or time.

This circuit is categorically different from the voltage regulator but with similar objectives, as both circuits generate regulated output voltages that are immune to the changes listed before, however, the accuracy is what distinguishes them. The voltage regulator presents a higher output current, resulting in a less precise output signal, higher output noise and unspecified long term stability.

Voltage reference circuits are used in all circuits that require a precise voltage, such as high resolution A/D and D/A converters, battery management systems, digital meters, smart sensors and many others.

2.2 Performance Measures

The characterization of a circuit is usually associated with its performance. The following measures allow to specify the voltage reference circuit implemented, as well as make comparisons with similar systems [1]. A precise reference voltage is not only a temperature compensated voltage source but also a stable circuit in time, therefore the reference voltage circuits should have high static and dynamic performances.

The static performance influences the absolute accuracy of the output voltage, and is affected by factors as:

- Line regulation.
- Load regulation.
- Variations on the components characteristics and values.
- Components mismatches.
- Channel length modulation effect (λ).
- Quiescent current.

The dynamic performance is regarded as the output voltage variations over the full range of operating conditions, consequently, it is generally influenced by factors as:

- Line Regulation (LR).
- Temperature Coefficient (TC).
- Power Supply Rejection Ratio (PSRR).
- Output Noise.

The following sections will provide formal definitions for each one of these factors.

2.2.1 Line Regulation

The line regulation (S_{LR}) specifies the variation of the output of the system with respect to the input voltage variation at a given temperature, which is usually considered the nominal temperature. The measurement is represented in Equation 2.1, and it is normally specified as μV/V or % [1].

$$S_{LR} = \frac{\Delta V_{REF,T_{(nom)}}(\Delta V_{IN})}{\Delta V_{IN}}, \tag{2.1}$$

where $\Delta V_{REF,T_{(nom)}}(\Delta V_{IN})$ is the variation of the reference voltage measured within the input voltage variation in the range of $\Delta V_{IN} = V_{IN(max)} - V_{IN(min)}$. The parameter $V_{IN(min)}$ indicates the minimum operating voltage of the voltage reference circuit, whereas $V_{IN(max)}$ represents the maximum operating voltage.

2.2.2 Temperature Coefficient

The physical characteristics of the various components will be impacted by the operating temperature, thus making the output voltage (V_{REF}) a temperature dependent signal. This temperature sensitivity of the circuit is known as temperature coefficient (TC) and it specifies the reference voltage variation over a range of temperature. This measurement is represented in Equation 2.2 and it is specified as parts-per-million per degree Celsius (ppm/°C) [1].

$$\begin{aligned} TC &= \frac{(V_{REF(max),V_{IN(nom)}} - V_{REF(min),V_{IN(nom)}})}{(T_{max} - T_{min}) * V_{REF(nom)}} * 10^6 \\ &= \frac{\Delta V_{REF,V_{IN(nom)}}(\Delta T)}{\Delta T * V_{REF(nom)}} * 10^6, \end{aligned} \tag{2.2}$$

where $\Delta V_{REF,V_{IN(nom)}}(\Delta T)$ is the variation of the reference voltage measured within the temperature range $\Delta T = T_{max} - T_{min}$.

2.2.3 Power Supply Rejection Ratio

In real world implementation, the power rail on the silicon is corrupted by the high frequency noise due to signal coupling, feedback, power surge, among others. The PSRR is defined as the ability of the output voltage to reject the noise and other signals at specific frequencies on the power supply. This measurement is represented in Equation 2.3 and it is specified in decibels (dB) [1].

$$PSRR = 20\log\frac{V_{REF,AC}(f)}{V_{IN,AC}(f)}, \tag{2.3}$$

where $V_{IN,AC}(f)$ is the power supply affected by noise at a certain frequency, directly related to $V_{IN} = V_{IN,AC} + V_{IN(nom)}$. The output voltage $V_{REF}(f) = V_{REF,AC}(f) + V_{REF(nom)}$, is an AC coupled reference voltage measured at the output of the voltage reference circuit.

2.2.4 Output Noise

Another frequency dependent performance parameter of the voltage reference circuit is the output noise. The noise is a random disturbance of a useful information signal and is created by several effects. Different types of noise are generated by different devices and different processes, the ones studied on this work are the thermal, shot and flicker noise.

The thermal noise, also known as "white noise", is generated by the random thermal motion of charge carriers, usually electrons. The shot noise is created by the junction of two materials where an electric field exists. Lastly, the flicker noise, occurs in almost all electronic devices because is originated by the imperfections of the used materials.

The output noise is specified in spectral densities, noise voltage per root hertz ($V/\sqrt{Hz}$), with a peak-to-peak voltage in a certain bandwidth [1].

2.2.5 Quiescent Current

The quiescent current, or supply current, is the current drawn from the power supply to operate the system designed at steady-state with no resistive load. In nominal conditions, with V_{IN} (nom) and the quiescent current I_q (nom), the power consumption of the system is given by V_{IN} x I_q [1].

Taking that into consideration, a low quiescent current is desirable. First, it implies the circuit has good power efficiency, resulting in long hours of work for applications with limited supply power. Additionally, a low quiescent current reference circuit has small power dissipation and consequently a small-heating effect which helps to maintain the accuracy and stability of the output signals.

The quiescent current is specified in amperes (A), and even though it is not a main concern in the system design, it will be measured and the result will be discussed.

2.3 Bandgap Voltage Reference Circuit

Bandgap Voltage Reference, or BGR, is the most commonly applied voltage reference circuit for bipolar and CMOS technology. One of the first, and most popular, bandgap circuits is known as Widlar bandgap voltage reference circuit, presented by Robert Widlar at the National Semiconductor in 1971 [2], and was first implemented in a commercial integrated circuit, named LM113. The idea behind the topology of this circuit is the compensation of a PTAT voltage and a CTAT voltage to reach a reference voltage with zero TC. For this, a weighted sum between these two voltages, such that

$$V_{REF}(T) = m_1 V_{PTAT}(T) + m_2 V_{CTAT}(T) \tag{2.4}$$

in order to get

$$\frac{\partial V_{REF}(T)}{\partial T} = m_1 \frac{\partial V_{PTAT}(T)}{\partial T} + m_2 \frac{\partial V_{CTAT}(T)}{\partial T} = 0 \tag{2.5}$$

For certain values of m_1 and m_2, and noting that $\frac{\partial V_{PTAT}(T)}{\partial T} > 0$ and $\frac{\partial V_{CTAT}(T)}{\partial T} < 0$, a near zero TC reference voltage can be obtained, as shown in Figure 1.

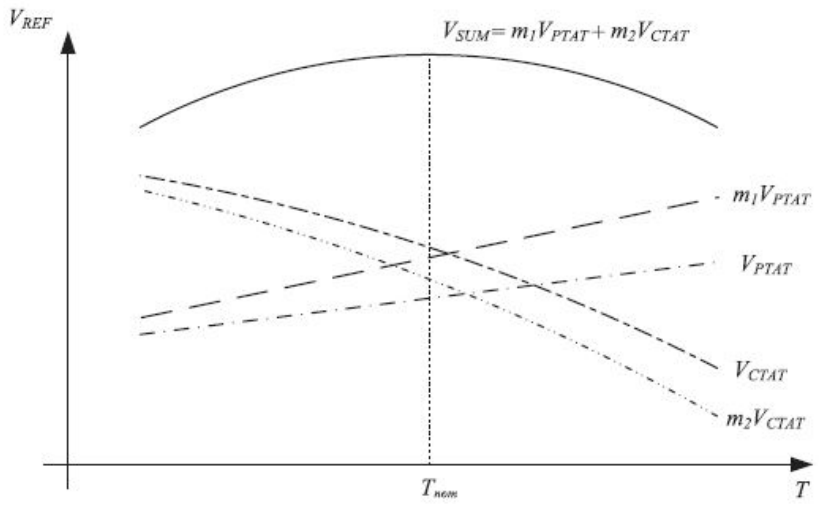

Figure 1: Temperature variation of reference voltage as a sum, from [1].

The compensated voltage obtained $V_{SUM}(T)$ is said to be a near zero TC voltage if $\frac{\partial V_{SUM}(T)}{\partial T} = 0$, at temperature T = T_{nom}. The CTAT voltage, in the Widlar bandgap voltage reference circuit, is formed by the V_{BE} of a BJT, while the PTAT voltage is formed by V_T extracted from ΔVBE of two BJTs biased with the different current densities.

According to Equation 2.4, a near zero TC reference voltage can be obtained by the weighted sum of V_{BE} and V_T as shown in Figure 2, where

$$V_{REF}(T) = V_{BE}(T) + MV_T(T) \tag{2.6}$$

Differentiating the equation in temperature

$$\begin{aligned} \frac{\partial V_{REF}(T)}{\partial T} &= \frac{\partial (V_{BE}(T) + MV_T(T))}{\partial T} \\ &= \frac{\partial V_{BE}(T)}{\partial T} + M\frac{\partial V_T(T)}{\partial T} \end{aligned} \tag{2.7}$$

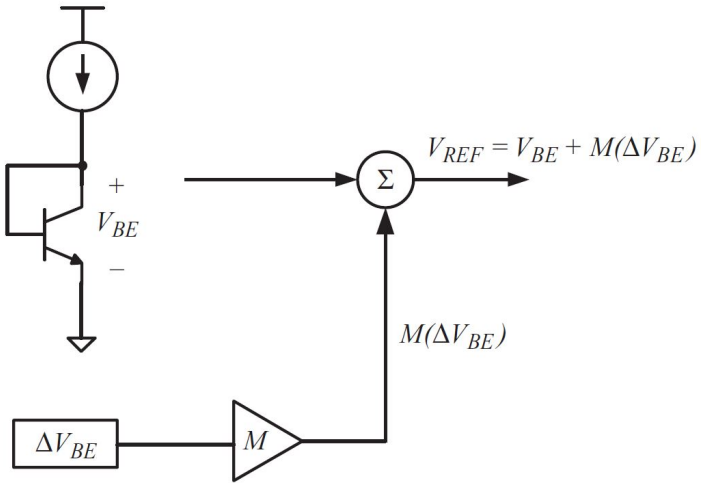

Figure 2: Block diagram of Widlar bandgap voltage reference circuit, from [1].

A BGR circuit, where the output is given by Equation 2.6, is known as a first order compensation circuit. In summary, the Widlar bandgap voltage reference circuit shows that if a CTAT voltage is summed with a PTAT voltage that has been scaled appropriately, such that both the CTAT voltage and the scaled PTAT voltage have the same temperature characteristic in magnitude, then a voltage that is almost independent of the operating temperature is obtained. Most of the BGR topologies are based on this principle, and the group which the circuit implemented belongs to will be discussed in the next section.

2.3.1 Sub-1V Bandgap Voltage Reference Circuit

The trend in integrated circuit fabrication is to move towards the minimum geometry size possible, to increase the circuit speed, capacity and decrease the power consumption. With this reduction in size, the functionality needed in a given area of substrate increases. Due to increased electric field and reduced breakdown voltage, caused by the higher doping of a smaller device, the operating voltage has to be scaled down. However, the voltage reference circuit becomes more difficult to design with low supply voltage.

The lower operating voltage has its limitations, and imposes some design constraints onto the circuit. The first constraint is the output of the voltage reference circuit, since it has to be lower than the supply voltage. The voltage reference circuit capable of generating a lower output voltage is referred as sub-1V voltage reference circuit, which means, as the name suggests, it outputs a reference voltage lower than 1 V. Another constraint is the fact that the circuit is required to be able to work with a low supply voltage. When the voltage reference circuit can operate at a supply voltage lower than 1 V, it is known as sub-1V supply voltage reference circuit. Clearly, a sub-1V supply voltage reference circuit can only generate reference voltage that is lower than the supply voltage, and as a result, it is also a sub-1V voltage reference circuit.

Conventional BGR circuits are neither suitable for low voltage applications, nor for generating low reference voltages. The restriction on designing a sub-1 V reference voltage is the bandgap voltage itself. As previously discussed, a near zero TC voltage is generated by properly scaling the PTAT thermal voltage V_T with the weighting factor M, and summing it up with the CTAT voltage V_{BE} of the bipolar transistor. The value of the factor M is related to the thermal coefficient of V_T (e.g., $\frac{\partial V_T(T)}{\partial T}$) and the thermal coefficient of V_{BE} (e.g., $\frac{\partial V_{BE}(T)}{\partial T}$). The weighting factor M has to be greater than $\frac{\partial V_{BE}(T)}{\partial T} \Big/ \frac{\partial V_T(T)}{\partial T}$. Taking that into account, a sub-1V reference voltage can be achieved by lowering the factor M, either through reducing difference between the thermal coefficients of the CTAT term and the PTAT term, or by using different thermal devices to lower the induced thermal voltages.

There are various methods in the literature that have the purpose of reducing the magnitude of the CTAT and PTAT terms to obtain the desired low reference voltage, such as the resistive division. There are also a lot of methods in the literature to reduce the thermal coefficients of the CTAT and PTAT terms, such as threshold voltage based compensation [3] and using depletion transistors [4]. The resistive division method is widely used, it has been employed in many BGR circuits, however, these circuits use multiple resistors which will inevitably increase the chip area. The threshold voltage compensation method is another approach, which makes use of the thermal properties of the threshold voltages $V_{th,n}$ and $V_{th,p}$ of MOSFETs with transistors biased in the saturation region.

This technique allows a more compact voltage reference circuit, and is also robust to process variation. However, because of the supply voltage variation and channel length modulation effect, these circuits usually suffer from a degraded PSRR performance. In summary, in order to produce a sub-1 V reference voltage, one of these methods must be applied. The topology adopted will be thoroughly explained in the circuit design section.

2.4 Current Reference Circuit

The other main objective of this work is to generate a reference current, e.g., a PVT independent current. Current reference is also essential to provide internal bias current for other analog circuits with low TC, and low sensitivity to supply voltage variation.

This part of the project began with the study of an isolated circuit that could deliver the desired result. The first studied circuit is the well known beta-multiplier current reference [5], represented in Figure 3. This circuit is an example of positive feedback use, since, with the addition of the resistor, the closed loop gain is lowered (a positive feedback system can be stable if its closed loop gain is less than one). However, if the size of the resistor is decreased, the loop gain increase will push the feedback system closer to instability. The transistors NM2, NM3 and PM3 form the startup circuit.

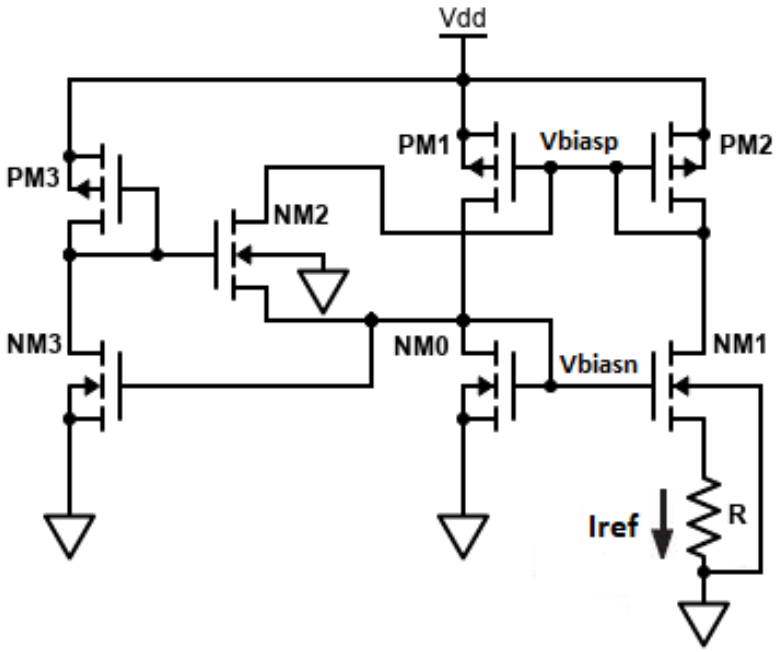

Figure 3: Beta-multiplier current reference circuit.

It was decided to design and simulate this circuit, with the addition of a differential amplifier to the circuit to compare the drain voltage of NM0 (V_{biasn}) with the drain voltage of NM1 (V_{reg}) and regulate them to be equal. Resulting in the circuit in Figure 4.

After testing, it was concluded that this topology was not appropriate for this application. The behaviour of the reference current in temperature and process corners was simulated, and the results were unsatisfactory. According to the simulations done, the circuit main objective is to generate a current stable with power supply voltage variation, which is not suitable to the proposed objectives. Taking that into account, and after analysing others isolated circuits solutions with similar results, it was concluded that another approach had to be taken.

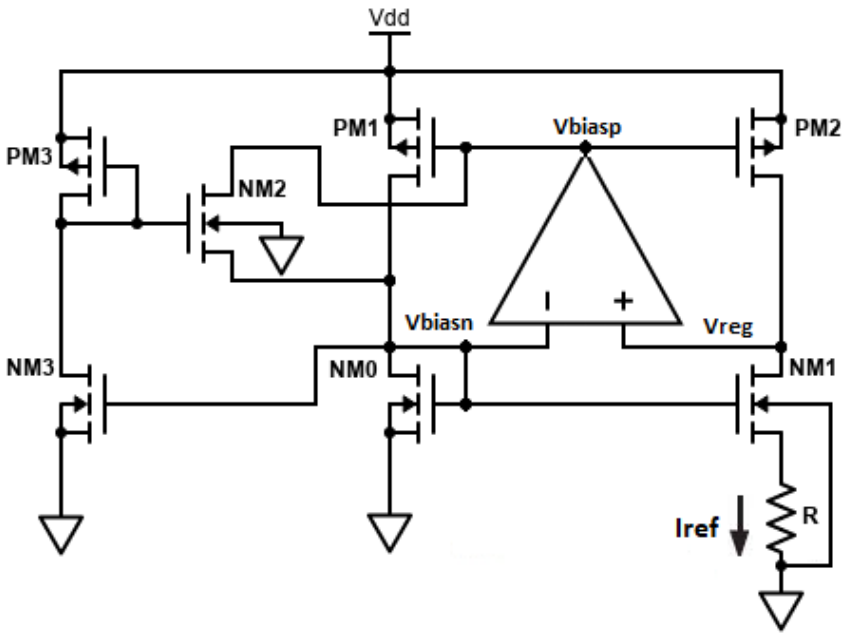

Figure 4: Improved current reference circuit.

The solution adopted was to make use of the BGR circuit already designed at that point, and its superior PVT sensitivity. The topology implemented is thoroughly explained in the circuit design section.

3. Circuit design - Sub-1V Bandgap Voltage Reference

3.1 Topology Implemented and Analysis

The Bandgap Voltage Reference topology implemented is a modified conventional opamp based on the β-multiplier BGR circuit in order to achieve the sub-1 V output voltage desired. This topology is based on the principle of the one proposed in [6], which in itself is an adaption of [7]. As previously said, the target value for the reference voltage is 900 mV, for temperatures between -40 °C and 125 °C, with a VDD voltage of 1.8 V.

As discussed in section 2.3.1, there are multiple methods to lower the reference voltage of a BGR circuit, Figure 5 shows a particular one. Taking the disadvantages into consideration, it was decided to apply the resistive division method, resulting in the represented circuit. Instead of stacking two thermal complementary voltages, this bandgap voltage reference circuit is a current sum circuit that generates a near-zero TC voltage by converting a temperature independent current into a reference voltage through a resistor.

The operation of this circuit is similar to that of the conventional opamp based β-multiplier bandgap voltage reference circuit, where the operational amplifier forms an inverted feedback loop to ensure its two input nodes have the same voltage.

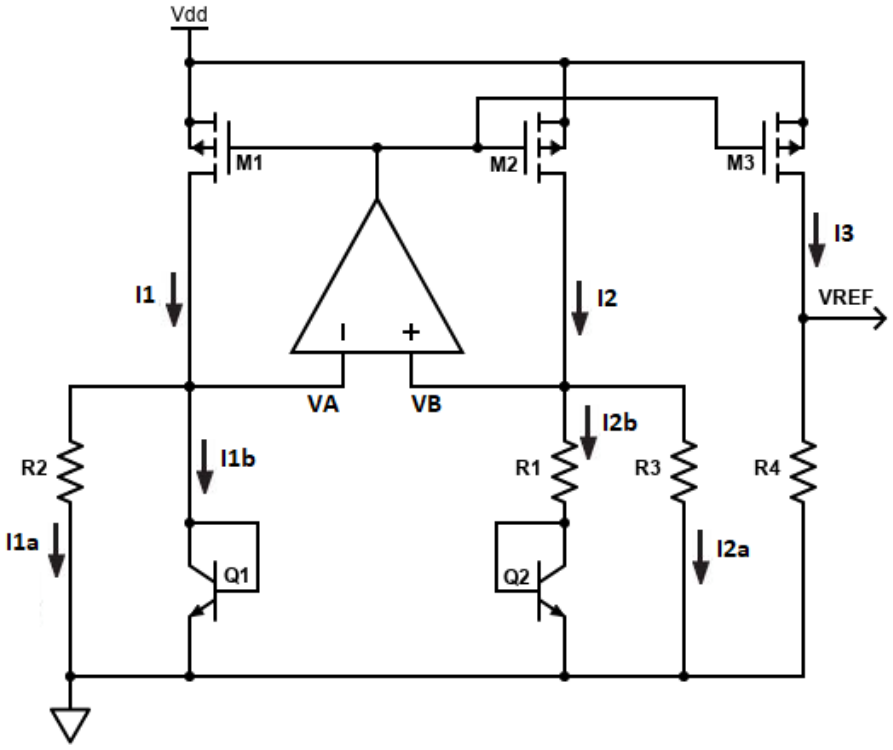

Figure 5: Bandgap voltage reference - topology.

Consider $R_2 = R_3$ such that $I_1 = I_2$, $I_{1a} = I_{2a}$ and $I_{1b} = I_{2b}$.

$$I_{2a} = \frac{V_A}{R_3} = \frac{V_B}{R_3} = \frac{V_{BE1}}{R_3}, \tag{3.8}$$

$$I_{2b} = \frac{V_B - V_{BE2}}{R_1} = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{\Delta V_{BE1,2}}{R_1} \tag{3.9}$$

The current I_2= I_{2a} + I_{2b}, and $\Delta V_{BE1,2}$ is the difference in the base-emitter voltages of the two TBJs Q_1 and Q_2. This difference has the following expression.

$$\Delta V_{BE1,2} = V_{BE1} - V_{BE2} = V_T ln(N) \tag{3.10}$$

With N being the emitter area ratio between Q_1 and Q_2. The output voltage of the bandgap voltage reference circuit is given by

$$\begin{aligned} V_{REF} &= I_3 R_4 \\ &= I_2 R_4 \\ &= (I_{2a} + I_{2b}) R_4 \\ &= \left(\frac{V_{BE1}}{R_3} + \frac{\Delta V_{BE1,2}}{R_1} \right) R_4 \\ &= \frac{R_4}{R_3} \left(V_{BE1} + \frac{R_3}{R_1} V_T ln(N) \right) \end{aligned} \tag{3.11}$$

Comparing Equations 3.11 and 2.6, it is possible to conclude that this circuit is a first-order compensated bandgap voltage reference circuit, where the weighting factor

$$M = \frac{R_3}{R_1} ln(N). \tag{3.12}$$

3.2 Sub-circuits

3.2.1 BGR Core Circuit

The design of the Bandgap voltage reference begins with the implementation of the core of the circuit, represented in Figure 6. The design process will be done in steps, starting with the BJTs current mirror and ending with the operational amplifier, presented in the next section.

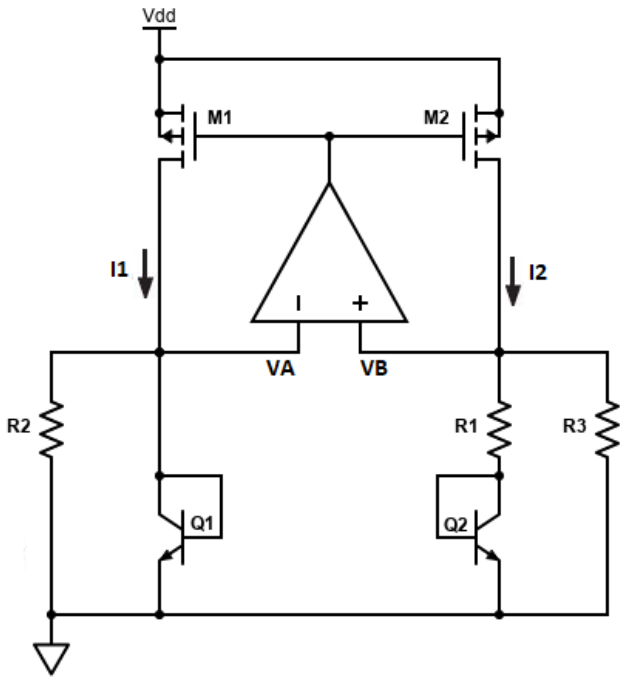

Figure 6: Bandgap voltage reference core - topology.

Firstly, the sizing of the transistors forming the current mirror is performed, using a multiplicity, between the BJTs, of N = 8. This will help mitigate the effect of process variation and device mismatch of the BJT pair when designing the layout. Using a layout technique known as common-centroid, where, in this case, the transistor Q_1 will be in the center, and the fingers of the transistor Q_2 will be around it, as represented in Figure 7.

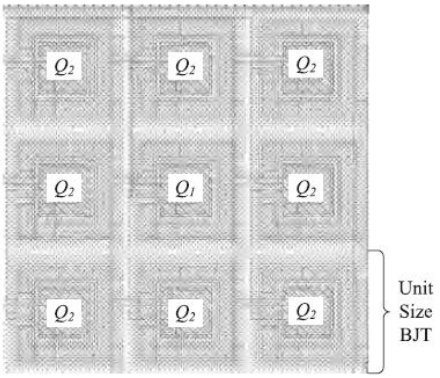

Figure 7: Centroid based layout, from [1].

The bipolar transistors have to be properly biased to operate correctly, therefore, it is considered an initial current $I_1 = I_2 = 6\ \mu$A, that will enable the start of the bandgap core design, by implementing the circuit in Figure 8.

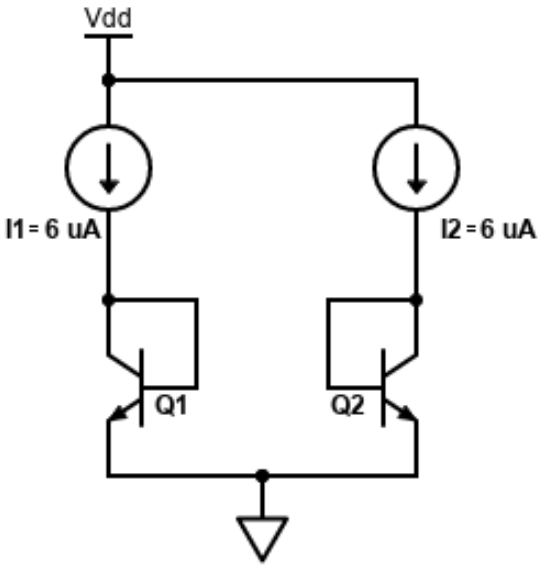

Figure 8: V_{BE1} and V_{BE2} voltages for equal emitter currents.

In order to extract ΔV_{BE}, a resistor R_1 is inserted in series with Q_2. If $V_A = V_B$, the voltage across the resistor will be equal to $\Delta V_{BE1,2}$. With that, the current flowing through the resistor is a PTAT current that can be extracted with a current mirror and converted back to a PTAT voltage using another resistor. The PTAT voltage will be combined with a CTAT voltage (V_{BE1}) to generate the reference voltage with low TC.

Furthermore, and according to Equation 3.9, in order to reach the initial resistance values

for R_1, R_2 and R_3, the derivative of V_{BE1} and $\Delta V_{BE1,2}$ must be calculated. The results, through simulation, are presented in Figures 9 and 10, respectively.

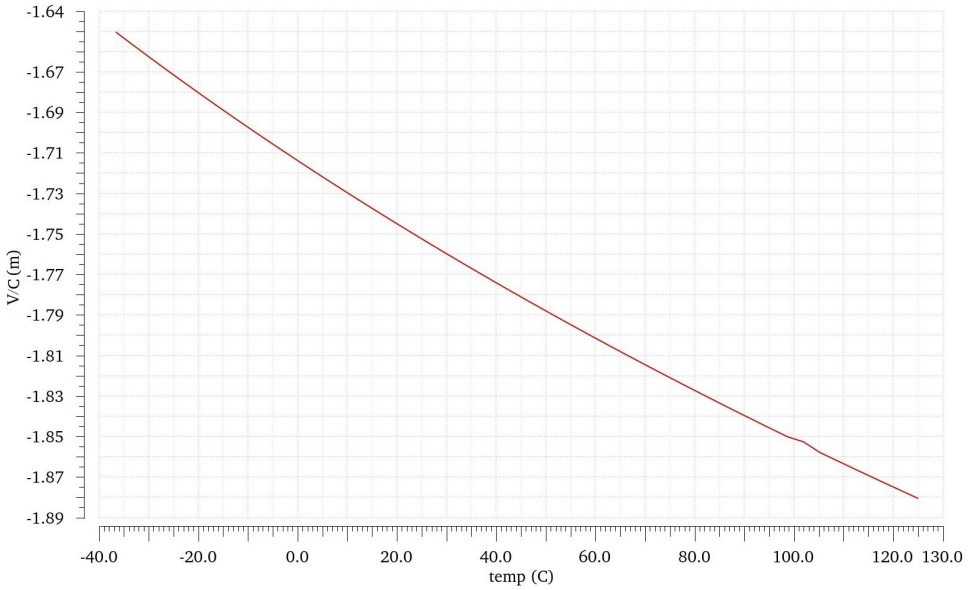

Figure 9: Derivative of V_{BE1}.

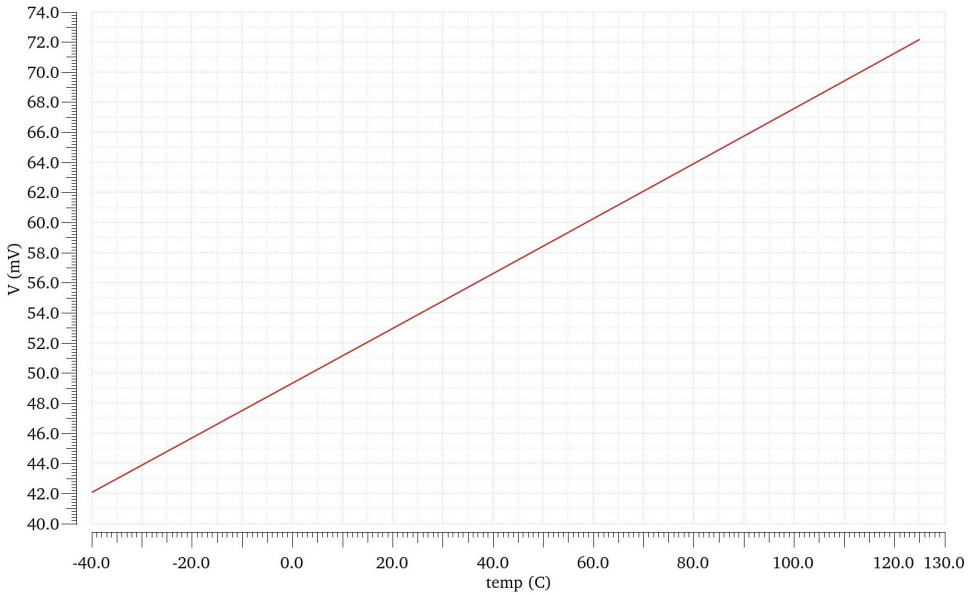

Figure 10: $\Delta V_{BE1,2}$.

At the nominal temperature, the value of $\frac{\partial V_{BE1}}{\partial T} \approx$ -1.75 mV/C and $\frac{\partial V_T}{\partial T} \approx$ 0.09 mV/C. Remembering that M = -$\frac{\partial V_{BE1}}{\partial T}/\frac{\partial V_T}{\partial T}$, for $T = T_{nominal}$, the result is M = 19.44.

Evidently, from Figure 10, the value of $\Delta V_{BE1,2}$ = 54.7 mV at the nominal temperature, and according to Equation 3.9, the value of R_1 = 54.7/0.006 = 9116 Ω. According to Equation 3.12, the value of $R_2 = R_3 = R_1$ x 19.44/ln(8) = R_1 x 9.35 = 85.241 kΩ.

To conclude the design of the bandgap core, only the the current mirror at the top remains to be designed. The PMOS transistors dimensions are calculated to achieve a V_{GS} = 1.16 V, in

order to replicate the voltage drop in each ideal current source seen in Figure 8. The results are listed in Table 1, the components names make reference to Figure 6.

Component	W	L	Unit
M1	2	1.53	μm
M2	2	1.53	μm

Table 1: MOSFETs dimensions.

3.2.2 Operational Amplifier

The opamp used is a single stage with a tail current source, as shown in Figure 11. The objective of this operation amplifier in the BGR circuit is to ensure the voltages V_A and V_B are equal at all times, and in all possible conditions.

The value of V_{GS} of the transistors M1 and M2, calculated in the previous section, indicate that the voltage at the each input is V_A (In-) = V_B (In+) = VDD - V_{GS} = 1.8 - 1.16 = 640 mV. In order for this opamp to be integrated in the bandgap core, in its quiescent point, the output voltage has to be equal to the voltage at its inputs.

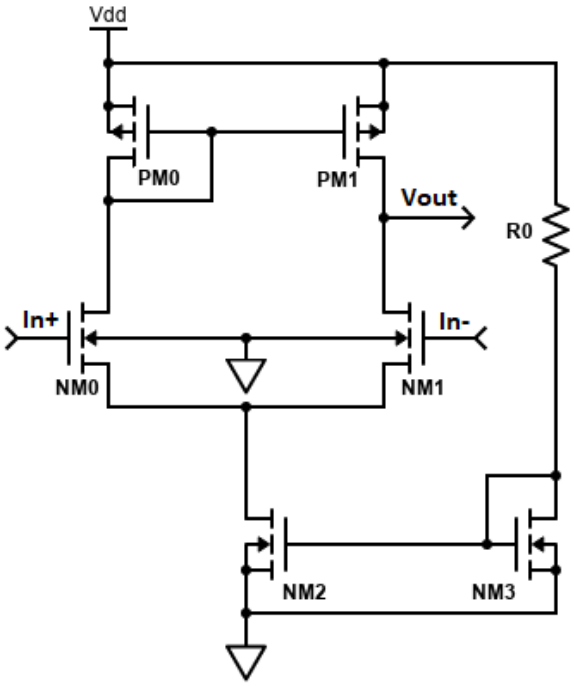

Figure 11: Opamp - topology.

The first step in the design of this opamp is done by deciding the value for the current flowing in each branch, thus, 10 μA is chosen as an initial value, prioritizing a lower consumption. After that, it is possible to calibrate the sizes of the components forming the current source: the transistors NM2 and NM3 and the resistor R_0, in order to feed 20 μA into the differential pair. The resistance value of the resistor chosen is 140 kΩ and the sizes of the transistors are listed in Table 11.

The remaining components were calibrated in order to reach the correct quiescent point, and to increase the opamp gain to a value high enough to ensure the two input nodes of the amplifier have the same voltage. The open loop gain, also known as DC gain, is defined as

$$A_v(dB) = 20\log\left(\frac{V_{OUT}}{V_B - V_A}\right) \tag{3.13}$$

The remaining transistors dimensions calculated are listed in Table 2.

Component	W	L	Unit
NM0	15	0.5	μm
NM1	15	0.5	μm
NM2	25	1	μm
NM3	15	1	μm
PM0	1.5	1.945	μm
PM1	1.5	1.945	μm

Table 2: MOSFETs dimensions.

An alternative to the resistor is possible through the use of a technique known as the bootstrap technique, where the resistor is replaced with a PMOS transistor with its gate connected to V_{OUT}. This method was implemented and tested, but the obtained results for the extreme values of temperature were not satisfactory, for example, the quiescent point of the BGR circuit, for T = -40 °C, presented an output voltage value of 1.3 V instead of 900 mV. Upon multiple tests, it was concluded that the resistor achieved more stable results, reaching the objectives proposed.

Following this, the schematic of the opamp implemented is represented in Figure 12 and the respective symbol in Figure 13.

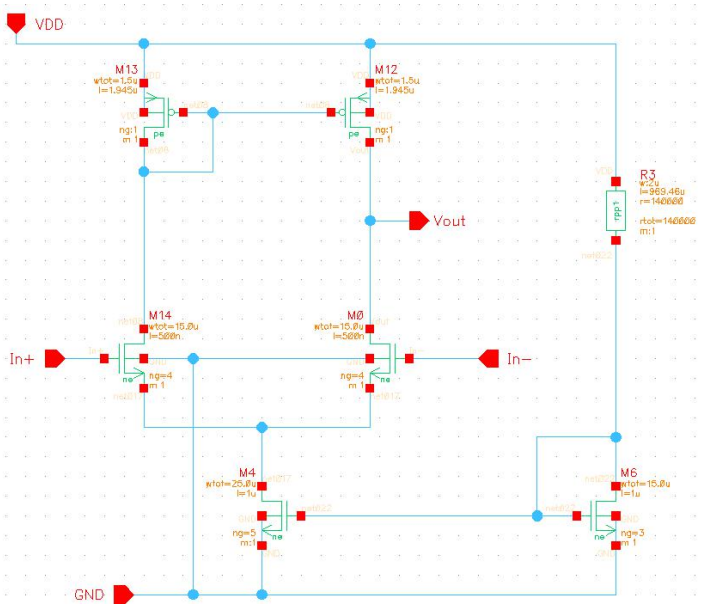

Figure 12: Opamp - schematic.

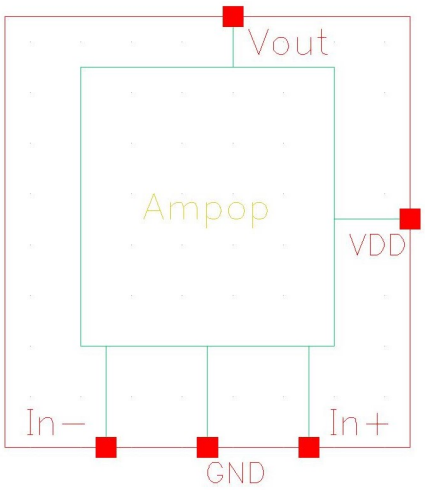

Figure 13: Opamp - symbol.

3.2.3 Startup Circuit

The bandgap voltage reference requires a startup circuit because it is a system that can become stable in both equilibrium state and quasi-equilibrium state. When the circuit starts, it is at a state with zero current in the BGR circuit, that is $I_1 = I_2 = 0$ and consequently $V_A + = V_B = 0$. As a result, the system is said to be in quasi-equilibrium state, and maintains the whole circuit in the startup condition.

Therefore, a startup circuit is needed in order to provide excitation to this state and bring the system to the equilibrium state that produces a stable reference voltage. Upon reaching the equilibrium state, the startup circuit has a negligible effect on the reference voltage of the BGR.

The startup circuit topology implemented is represented in Figure 14. Since this startup will bias the current mirror in the bandgap core, the pin V_{AMP} is connected to the gate of the transistors M1 and M2, from Figure 5.

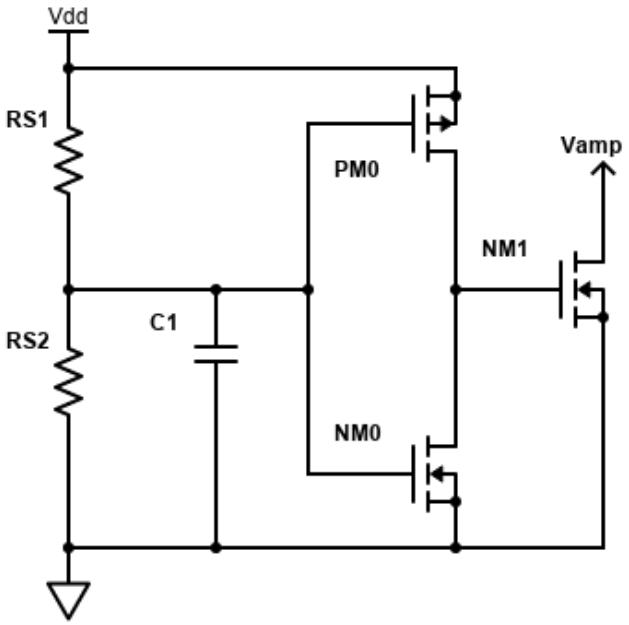

Figure 14: Startup circuit - topology.

When the bandgap voltage reference circuit first connects to VDD, the capacitor C_1 will be charged up by R_{S1}. As a result, the input voltage of the NOT gate formed by NM0 and PM0 will be close to GND and will generate a low input, hence outputs a high signal which turns on NM1. The current drain NM1 will lower the gate voltage of M1, M2 and M3, from Figure 5, to GND, meaning, the currents I_1, I_2 and I_3 will start to flow. At this point the circuit is started up.

Then, as time passes by, the capacitor will reach a voltage higher than the triggering voltage of the NOT gate, resulting in a low signal at the output of the NOT gate, which will bias NM1 to shut off. From this point on, the startup circuit will no longer affect the working of the bandgap voltage reference circuit, and consequently, of the voltage to current converter as well. If system is detached from VDD, the capacitor C_1 is going to be discharged through R_{S2}, therefore, in order to prevent a large amount of current being wasted by the resistor when connected to VDD through R_{S1}, R_{S2} has to have a very large resistance.

The parameters used in the design of the startup circuit are listed in Tables 3 and 4, the

components names make reference to Figure 14.

Component	Value	Unit
R_{S1}	75	kΩ
R_{S2}	105	kΩ
C_1	150	pF

Table 3: Resistors and capacitor values.

Component	W	L	Unit
NM0	1	1	μm
NM1	0.3	5	μm
PM0	15	1	μm

Table 4: MOSFETs dimensions.

The startup period, which is determined by the charging time of C_1 through R_{S1}, implies that the startup delay is controlled by the RC time delay of these components. Therefore, the startup delay for the circuit is τ = C_1 x R_{S1} = 150 x 10^{-12} x 75000 = 11.25 μs. This startup delay should be longer than the VDD settling time, to avoid the propagation of the unstable VDD to the reference voltage.

In conclusion, the schematic of the startup circuit implemented is represented in Figure 15 and its respective symbol in Figure 13.

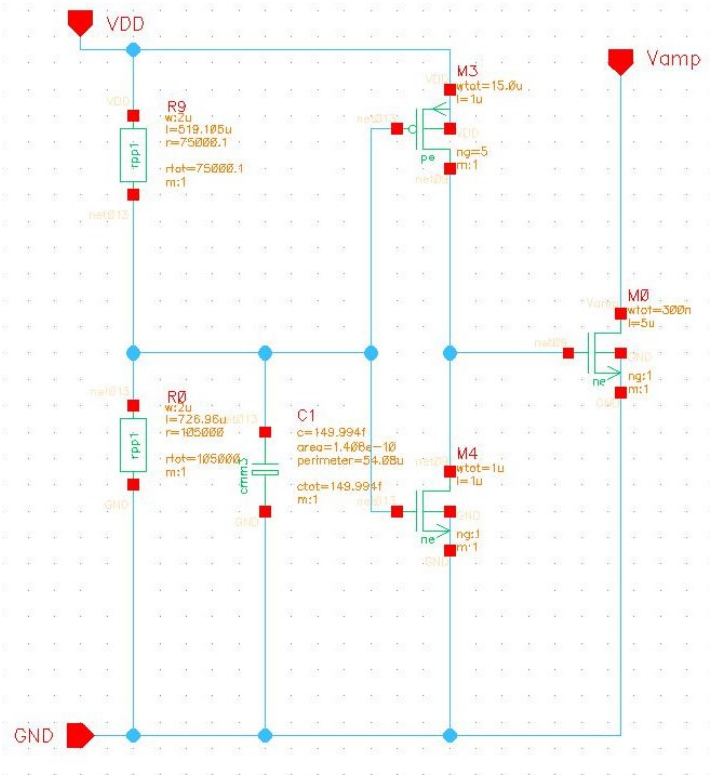

Figure 15: Startup circuit - schematic.

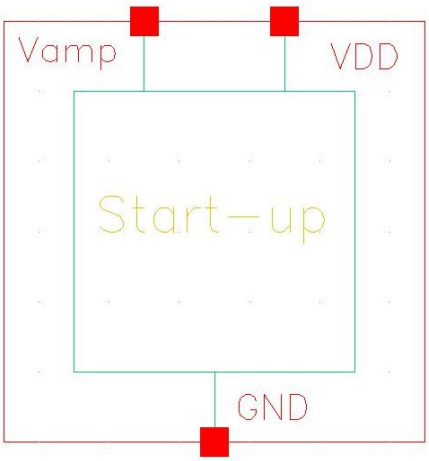

Figure 16: Startup circuit - symbol.

4. Circuit Design - Voltage to Current Converter

4.1 Topology Implemented and Analysis

As discussed in the section 2.4, after the examination of the results obtained for the isolated current reference circuits, it was decided to generate the current by utilizing the BGR circuit designed. The general approach to build a micro-ampere current reference is based on two different structures, shown in Figures 17 and 18 [8] [9].

The first one is a circuit where the reference current is the combination of a PTAT current, coming from the BGR core, and a CTAT current created by V_{BE}, however, since these two compensated currents come from different sources, the result would suffer from process variation.

The other topology makes use of the BGR reference voltage established, using an amplifier as a buffer of V_{REF} and an additional resistor to convert that voltage into a current, as shown in Figure 18 [10]. Feedback is used to generate the PMOS gate voltage that tries to produce a voltage drop of precisely V_{REF} across the resistor. In order to generate a stable reference current, a resistor with zero TC is preferable. However, since a zero TC resistor in CMOS process is not easily fabricated, as the doping concentration is hard to control, an off-chip resistor is usually the adopted solution.

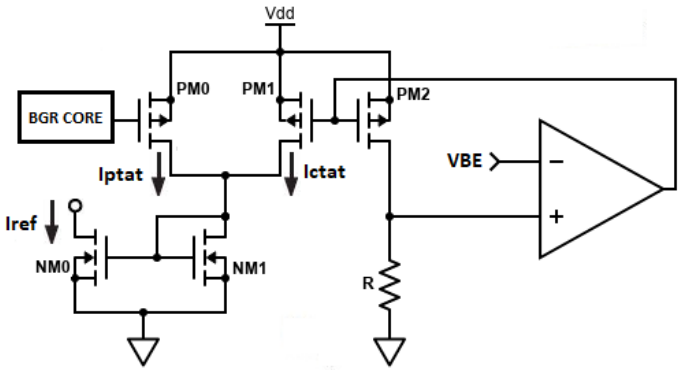

Figure 17: Combination of CTAT and PTAT current.

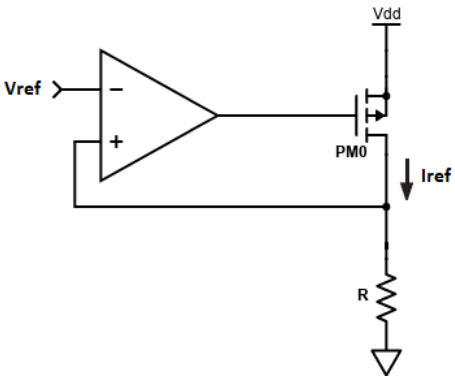

Figure 18: Voltage to current converter circuit.

In this work, the approach chosen is the latter, represented in Figure 18. As previously mentioned, an off-chip resistor is usually the solution, however, in the technology used there are multiple resistors with low temperature coefficients. It was decided to use the resistor type already used in the BGR circuit, since it is the one with the lowest TC.

In order to check the affect of the temperature on the on-chip resistor, the voltage across R is measured, while an ideal current of 1 mA is flowing through it. The simulation result is represented in Figure 19. The total voltage variation obtained is V_{MAX} - V_{MIN} = 1.541 - 1.508 = 0.033 V, which is 2.17% of the voltage at the nominal temperature (1.52 V). According to Equation 2.2, the temperature coefficient is TC = 131.57 ppm/°C.

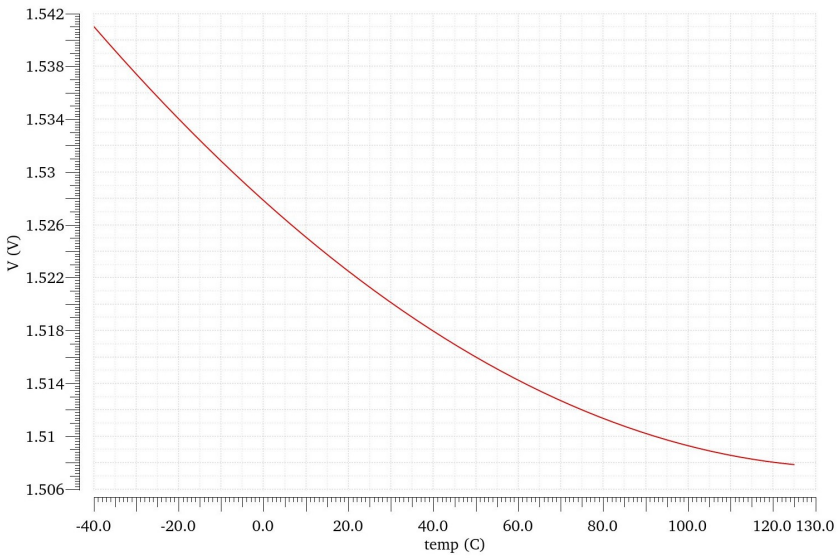

Figure 19: Voltage variation in temperature.

Considering this, the proposed circuit will provide both options to choose from, one where an off-chip resistor is used to calculate the current and another where it is calculated using the on-chip resistor [11]. As shown in Figure 20, a path is created, starting in a point where the voltage is V_{REF} and ending in a pin (Trim_up), where a pad will be externally connected. Connecting to that pad will be the external resistor, if that is the option taken by the user.

Additionally, a transistor NMOS will act as a switch, controlled by the voltage at its gate, placed after the resistor, to avoid higher parasitic elements. When the voltage at the gate (ExtR) is 0, the transistor will cut and act as an open circuit, meaning the off-chip resistor will be used to generate the current. On the other hand, when the gate voltage has a high enough value, the transistor will act as a diode, connecting the on-chip resistor to GND and generating the desired current I_{REF}.

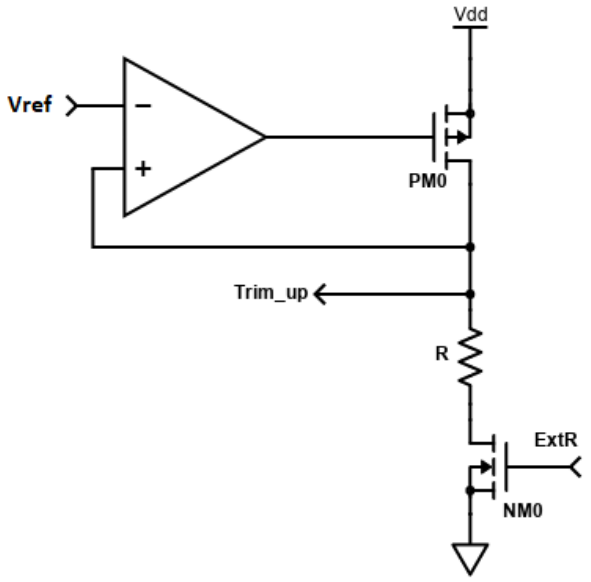

Figure 20: Voltage to current converter - topology.

4.2 Sub-circuits

4.2.1 Amplifier

As previously mentioned, the objective of this amplifier is to act as a buffer to the voltage at the inverting input (V_{REF}). The amplifier implemented is similar to the opamp used in the BGR circuit, but without the current tail source. The topology is presented in Figure 21.

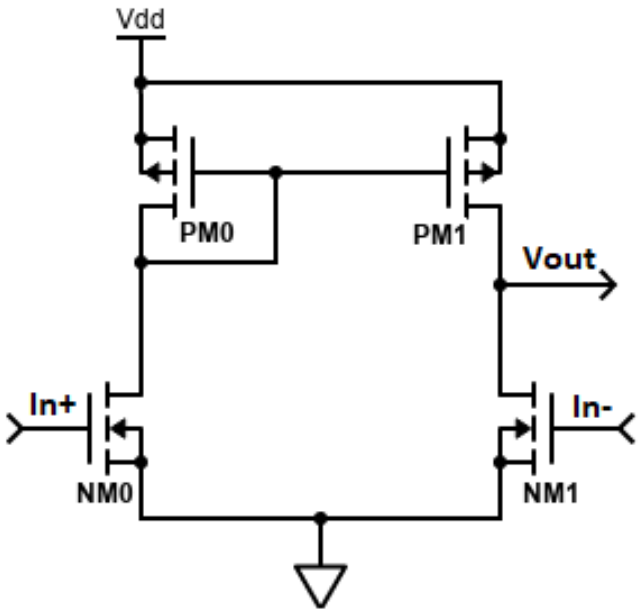

Figure 21: Amplifier - topology.

The transistors in this amplifier were sized in order to reach the correct quiescent point, which is presenting an output voltage equal to the voltage at the input (900 mV). The dimensions obtained are listed in Table 5.

Component	W	L	Unit
NM0	4	1	μm
NM1	4	1	μm
PM0	15.5	0.5	μm
PM1	15.5	0.5	μm

Table 5: MOSFETs dimensions.

Following this, the schematic in Figure 22 was implemented, and its respective symbol in Figure 23.

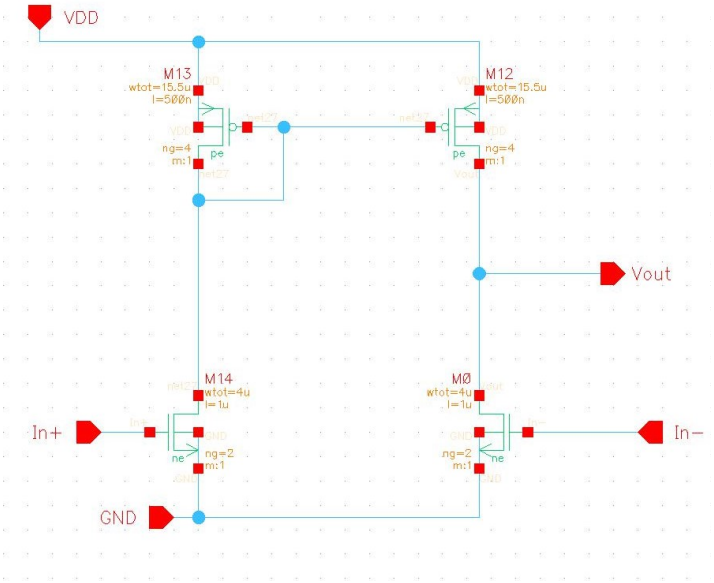

Figure 22: Amplifier schematic.

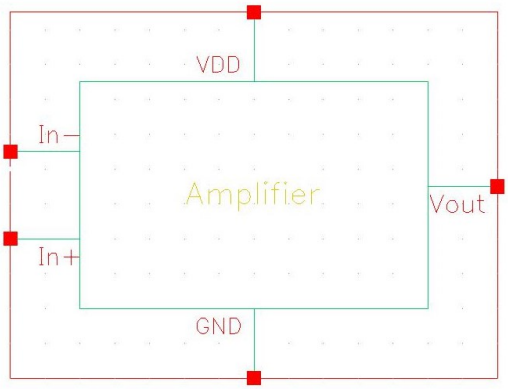

Figure 23: Amplifier symbol.

4.2.2 Resistor Trimming

The on-chip resistor has a resistance value of 900 kΩ, since the voltage across it is 900 mV and the target current is 1 μA. According to Figure 19, and as previously calculated, the TC of the on-chip resistor used is low. However, after analysing the process corners simulation for the current, it is clear that the total variation obtained is not suitable for this application. The result is represented in Figure 24, where the typical corner is represented in the colour red.

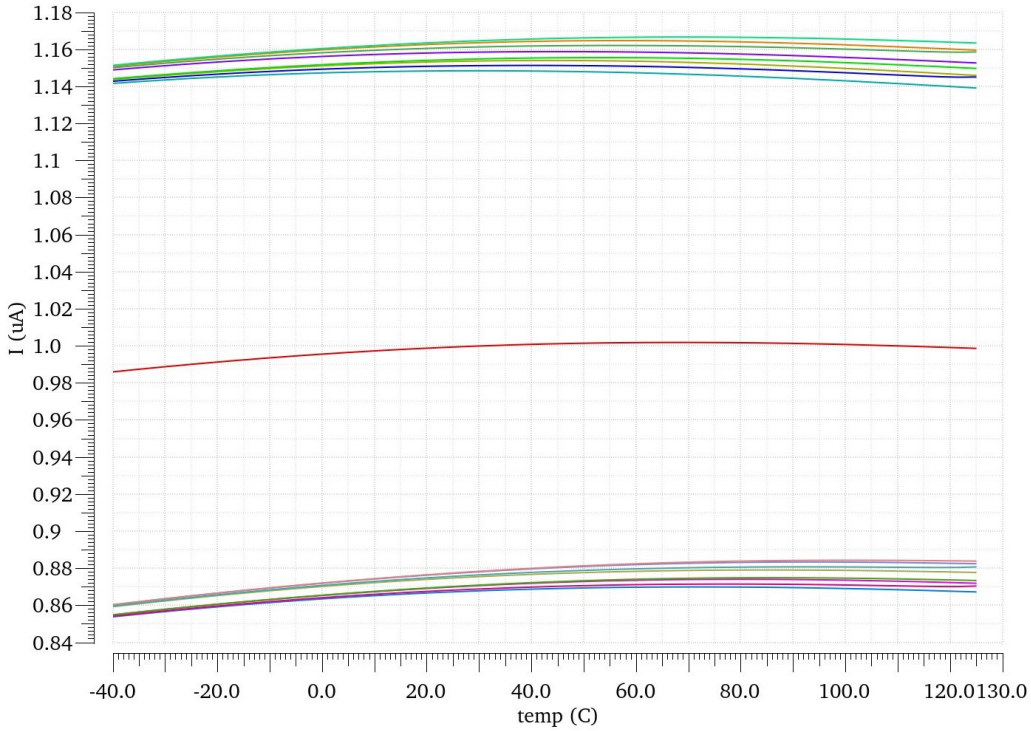

Figure 24: Process corners simulation.

Therefore, in order to reach a better variation of the current in the corners simulation, the trimming the resistor is performed, which permits a precise adjustment of the resistance value to reach the desired value of current, in each process corner [10]. This technique consists in separating the original resistor into two parts, one part has a fixed resistance value and the other has a value that will vary accordingly.

According to Figure 24, the maximum value of the current reached is approximately 1.17 uA, thus the minimum resistance value is 769 kΩ. On the other hand, the minimum value of the current reached is approximately 0.85 uA, thus the maximum resistance value is 1058 kΩ, which represents a variation of 1058 - 769 = 289 kΩ. Usually, in the trimming process, a safety margin is implemented, therefore it is decided to amplify the variation obtained to 465 kΩ. This augmentation will result in a new minimum resistance value of 675 kΩ, that represents the fixed value of the resistor, and a new maximum resistance value of 675 + 465 = 1140 kΩ.

In summary, the on-chip resistor will be formed by a fixed resistance value, 675 kΩ, and the remaining part will be adjusted, 465 kΩ. The adjustment is done by dividing the resistance value 465 kΩ into five independently controlled resistors, represented as R_0 through R_4 in Figure 25. Each one of these resistors will be controlled through a switch, implemented with a NMOS transistor, where they will be ON (triode region) or OFF (cut off region), depending on the transistor gate voltage. The trimming result is a digital word of 5 bits, for each process corner, noting that the resistance values chosen for each resistor allow the digital word for the nominal corner to be 10000. The circuit implemented, now with the resistor R trimmed, is represented in Figure 25.

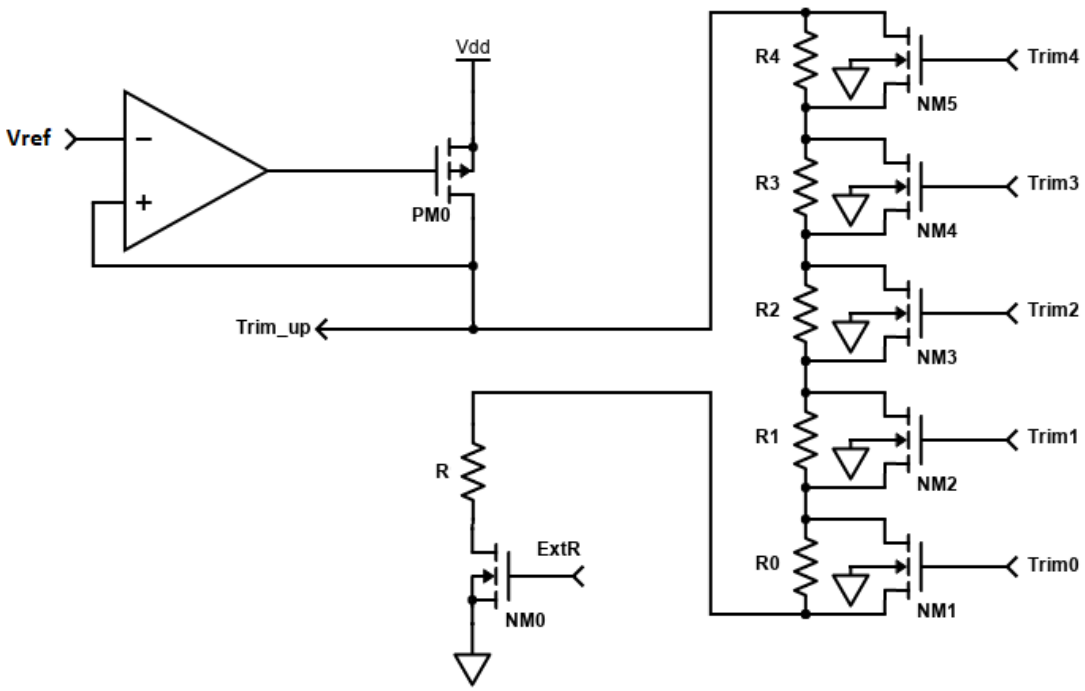

Figure 25: Voltage to current converter circuit with trimmed resistor.

Everyone of the NMOS transistors, acting as a switch, have to have a large width because the current flowing through the resistor should be negligible when compared with the one flowing through it. In order to replicate a short circuit as best as possible in the ON mode, the ratio W/L has to be extremely high.

The dimensions of the transistors used are listed in Table 6, the resistances values are listed in Table 7.

Component	W	L	Unit
NM0	10	0.18	μm
NM1, NM2, NM3, NM4, NM5	50	0.18	μm
PM0	8	8.9	μm

Table 6: MOSFETs dimensions.

Component	Value	Unit
R_0	15	kΩ
R_1	30	kΩ
R_2	60	kΩ
R_3	120	kΩ
R_4	240	kΩ

Table 7: Resistors values.

4.2.3 Current Mirrors

Reference circuits present an output current that is, usually, flowing in the conventional direction, e.g., the currents flows from the positive terminal to the negative. However, depending on the application, it is convenient to have that same current flowing in the opposite direction. To cover this possible problem, the circuit represented in Figure 26 was implemented. The transistor PM1 will form a current mirror with PM0, with a ratio of 1:1, and output the current flowing in the conventional direction through Iref. The transistor PM2 will also mirror the current, however, the mirror formed by transistors NM6 and NM7 will reverse the flowing direction of the current, and output it through Iref2.

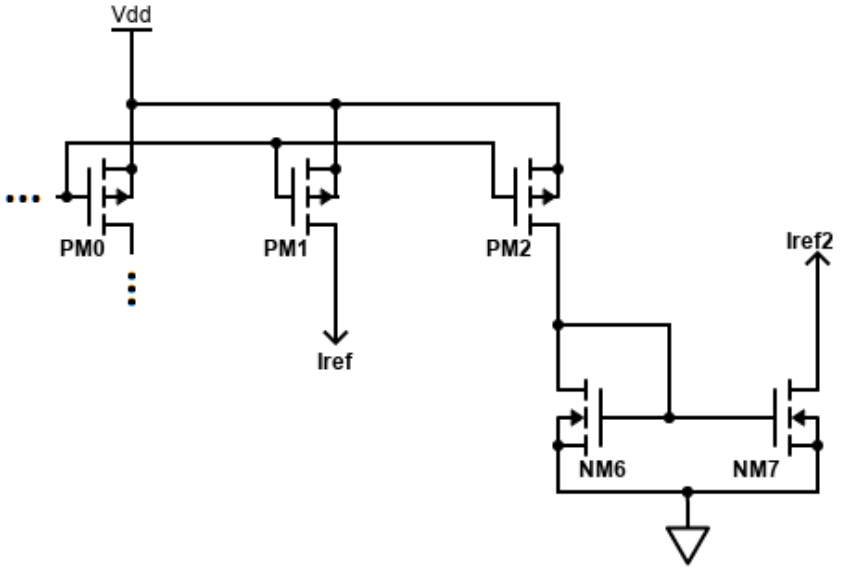

Figure 26: Current mirrors.

The dimensions of the transistors used in the design of these current mirrors are listed in Table 8.

Component	W	L	Unit
NM6, NM7	1	10.5	μm
PM1, PM2	8	8.9	μm

Table 8: MOSFETs dimensions.

4.3 System Schematic

The schematic of the system, which includes the BGR circuit and the voltage to current converter, is represented in Figure 27. The schematic is represented in a separate page, due to the size of the circuit and better visibility, enabling the possibility to discern all the details.

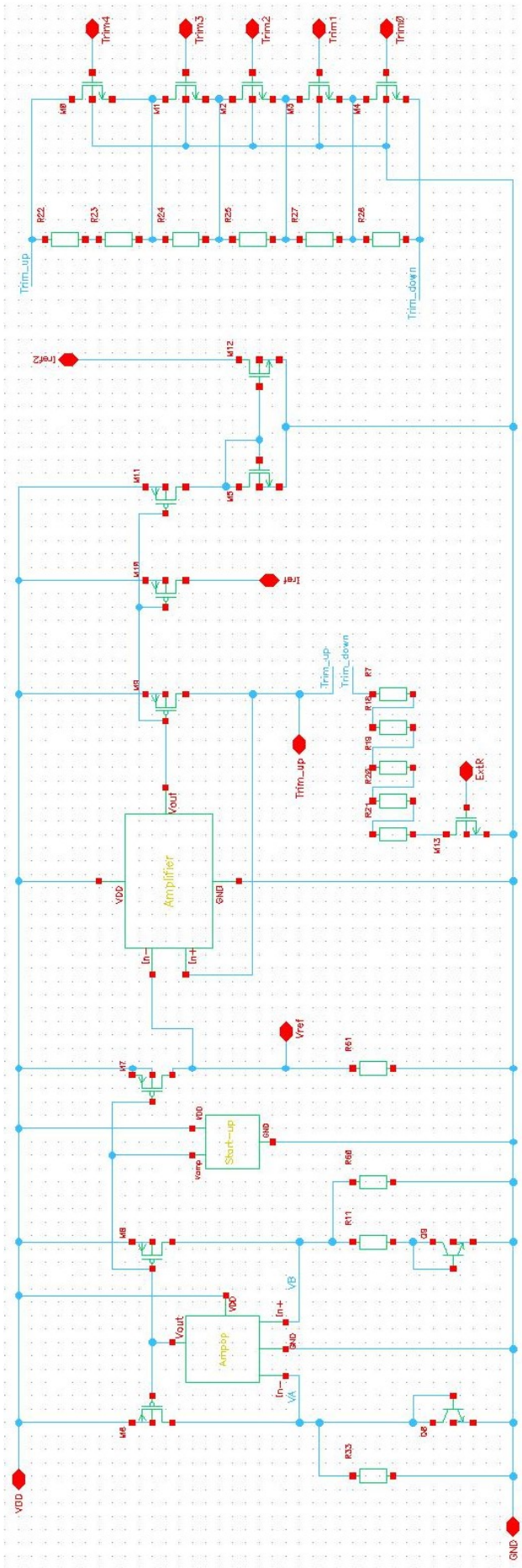

Figure 27: System - schematic.

5. Pre-layout Results

5.1 Testbench and Analyses

The environment, also known as testbench, used to verify the performance of the system designed is represented in Figure 28.

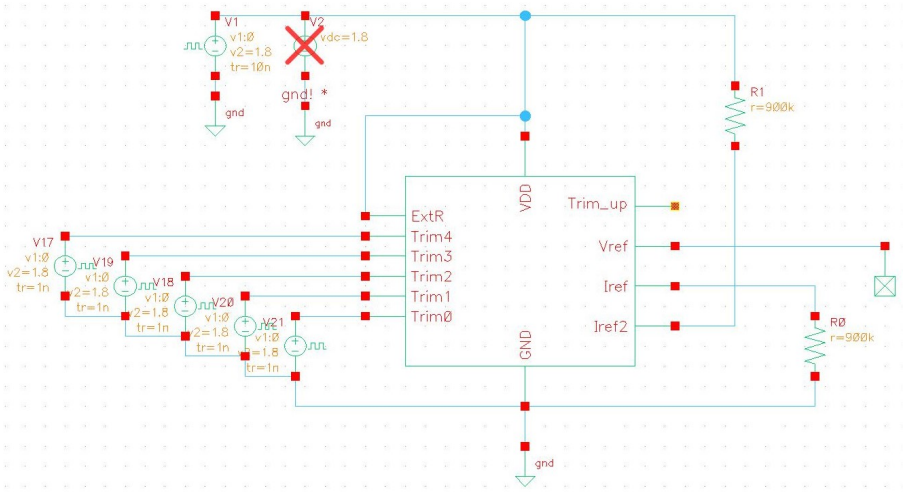

Figure 28: System testbench.

The power supply VDD is generated by either a vdc source with 1.8 V, for DC and AC analyses, or a vpulse source with a rising time of 10 ns, for transient analyses. The pin ExtR is either connected to VDD, to utilize the on-chip resistor, or connected to GND to use the off-chip resistor. The pin Trim_up will be connected to the external resistor, if that is the option taken by the user, otherwise it is not connected at all.

The trimming is performed with vpulse sources, where all the combinations of 5 bits are generated and the delay time is set to 10 μs so the reference voltage from the BGR circuit has enough time to stabilize, as represented in Figure 29.

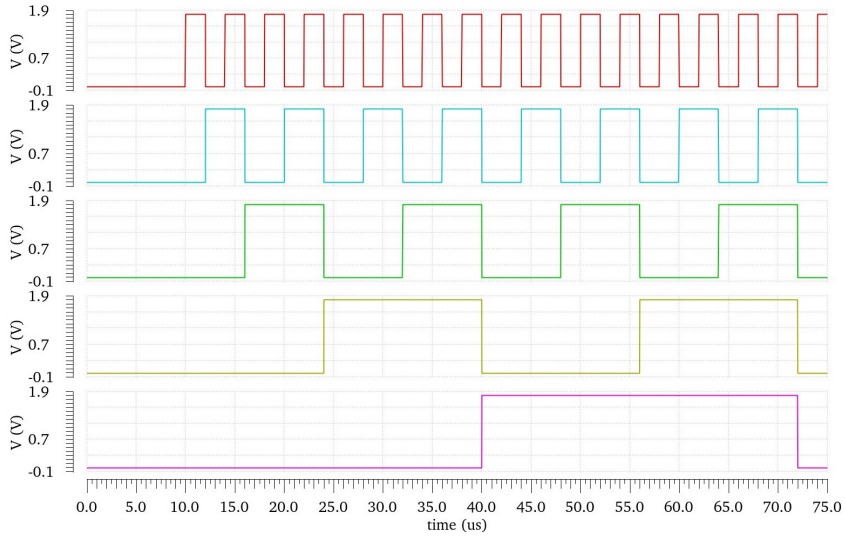

Figure 29: Trim0 (red), Trim1 (blue), Trim2 (green), Trim3 (yellow) and Trim4 (purple).

The pin V_{REF} will output the BGR circuit voltage. The pins I_{REF} and I_{REF2} will output the current converted from the reference voltage, and the resistances R_0 and R_1 are used to measure the value of that same current. The pin I_{REF} outputs the reference current flowing in the conventional direction; whereas the pin I_{REF2} will output the current flowing in the opposite direction, also known as electron direction.

All the analyses performed to evaluate the circuit can be classified in three different groups: DC, AC and Transient analyses. All the analyses performed are be replicated in the post-layout simulations.

5.1.1 DC Analysis

A DC analysis was performed for the quiescent point for every single block designed in this system, as previously discussed. Furthermore, some of the performance measures reviewed in section 2 are calculated through DC analysis. The temperature coefficient measure is achieved by performing a DC analysis with a sweep of temperature from -40 °C to 125 °C. On the other hand, the DC analysis for the linear regulation measurement requires a sweep of power supply voltage value.

5.1.2 AC Analysis

The AC analysis is needed to evaluate the power supply rejection ratio (PSRR), defined in chapter 2. This analysis is performed considering an AC voltage source in the main supply voltage and measuring the output of the circuit at the frequencies of 1 Hz and 10 MHz. In the case of the opamp used in the bandgap, all its specifications are calculated through AC analyses, as future sections will show.

5.1.3 Transient Analysis

The transient analysis in this work is performed to evaluate the performance of the startup circuit for different temperatures, in the interval specified.

5.2 Simulation Conditions

The simulation conditions are highly influenced by specifications such as temperature range, devices models, supply voltage; which are important considering the potential impact on the results. Process corners are the result of the variation from the typical conditions of these parameters, where all the possible combinations are accounted for. For the circuit designed, there are 32 corners and 1 typical condition, also known as nominal corner. The 32 corners will consider all possible combinations of parameters previously mentioned and will take part in the simulations.

As mentioned above, the combinations for the process variations are called process corners, because they represent the limits of the process as the word suggests. In this project, the corners used to simulate all the stages of the circuit during its design are shown in Figure 30. The corners nomenclatures represent:

- **TM** - typical mean
- **WP** - worst power: the V_T of all MOS is lowered, they become faster
- **WS** - worst speed: the V_T of all MOS is raised, they become slower

- **WO** - worst one: the V_T of NMOS is lowered, they become faster; the V_T of PMOS is raised, they become slower
- **WZ** - worst zero: the V_T of NMOS is raised, they become slower; the V_T of PMOS is lowered, they become faster

Noting that, in the case of the DC and AC analyses, there are only 16 corners and 1 typical condition since only one capacitor is used in the system, and it is part of the startup circuit, which has a negligible impact on these simulations. Considering that, a second group of corners is created (C1), enabling the simulation time to be halved for these simulations.

Corners	Nominal	C0	C1
Temperature			
Design Variables			
Click to add			
Parameters			
Click to add			
Model Files			
mos.scs		wo wp ws wz	wo wp ws wz
param.scs		3s	3s
dio.scs		tm	tm
res.scs		wp ws	wp ws
cap.scs		wp ws	tm
bip.scs		wp ws	wp ws
Click to add			
Model Group(s)		<modelgroup>	<modelgroup>
Click to add			
Tests			
...ck_Testbench:1			
Number of Corners	1	32	16

Figure 30: ADE XL corners setup.

5.3 Sub-1V Bandgap Voltage Reference Circuit Simulations

In this section, the performance measures of the BGR circuit are calculated through various simulations. The measures presented in this section make reference to the factors specified in section 2.2, as such, these results allow to characterize and compare this voltage reference circuit with other similar circuits. The following sections will present the process corners simulation for each one of the measures, including the typical corner simulation. The testbench used in this circuit is represented in Figure 28.

5.3.1 Line Regulation

The line regulation is the variation of the reference voltage in respect to the variation of the power supply voltage. This measure value can be obtained by performing a DC analysis, with a sweep in the dc value parameter of the supply source. A first simulation between 1.5 and 3 V would allow to specify the interval for this measurement. Upon examination, it was decided

to use an interval between 1.7 and 2.4 V to reach better results. The new simulation result is represented in Figure 31, including the 16 corners and the typical corner (red).

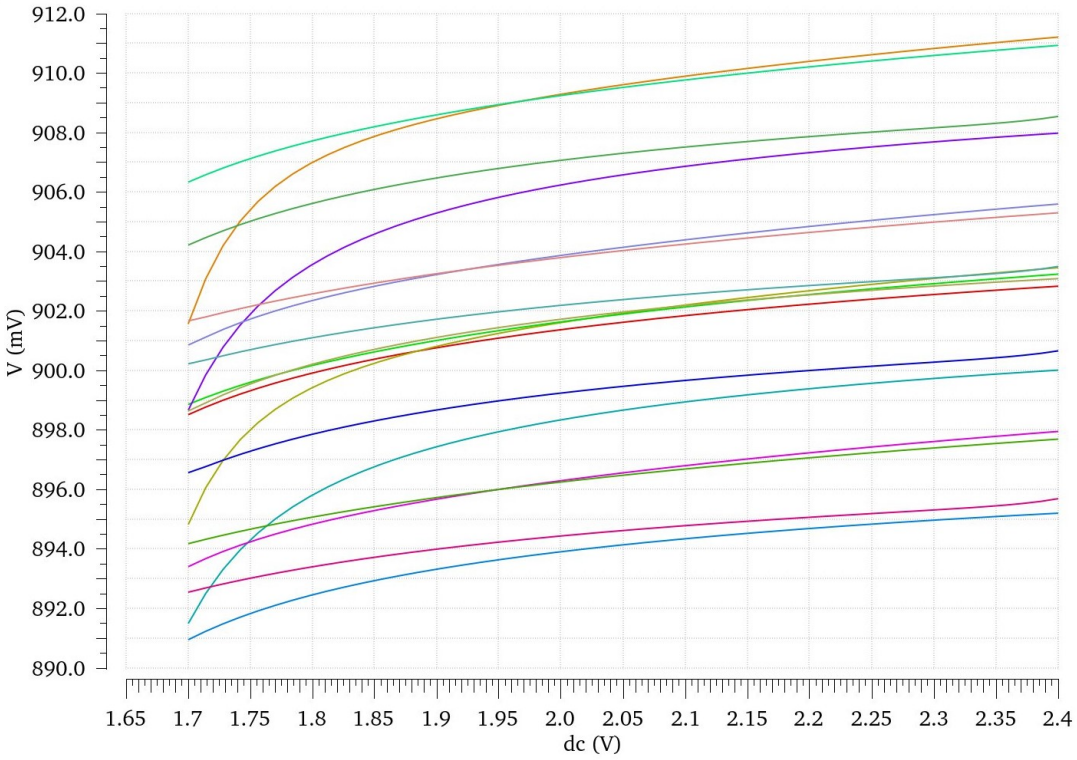

Figure 31: LR - process corners.

According to Equation 2.1, and inspecting the corners simulation result in Figure 31, the line regulation values obtained are listed in Table 9.

Specification	Min.	Typ.	Max.	Unit
LR	0.42	0.57	1.43	%

Table 9: Corners simulation results.

5.3.2 Temperature Coefficient

The next performance measure to be calculated is the temperature sensitivity of the circuit, also known as TC. This measure value can be obtained by performing a DC analysis as well, however, with a sweep in temperature between -40 °C and 125 °C.

The simulation result for the typical corner is represented in Figure 32, and it is obtained the expected result for a reference voltage in a BGR, e.g., the value of V_{REF} is equal to 900 mV at T = 27 °C (nominal temperature). Additionally, as discussed in section 2.3, the voltage obtained is near zero TC, since $\frac{\partial V_{REF}(T)}{\partial T} = 0$ at temperature T = T_{nom}.

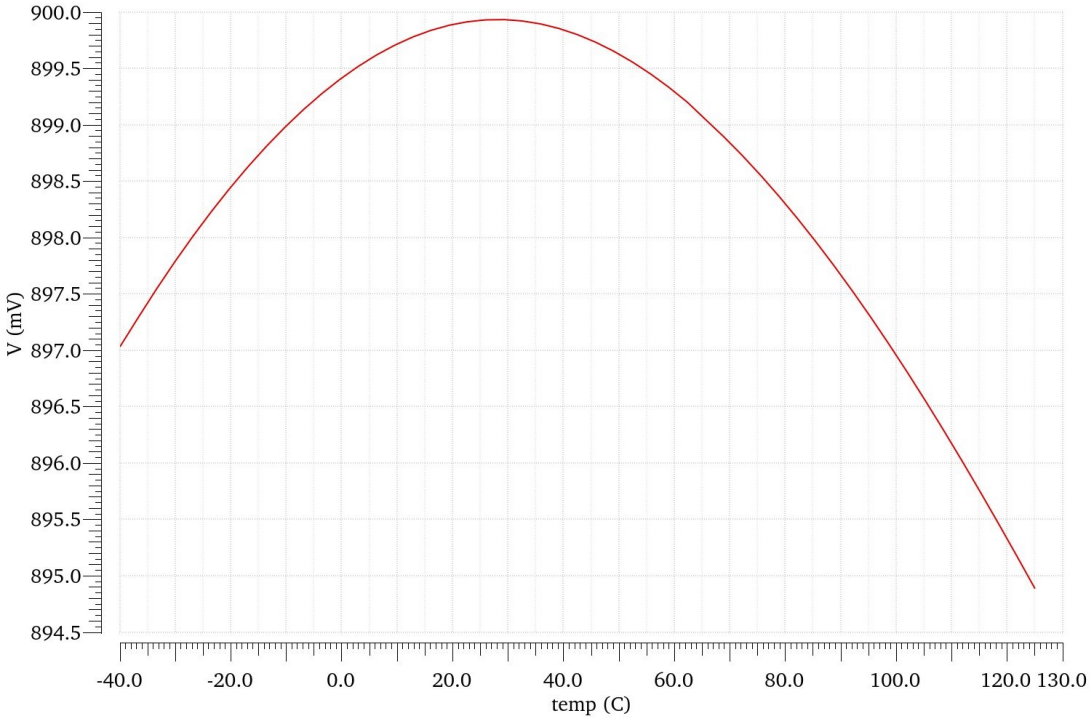

Figure 32: TC - typical corner.

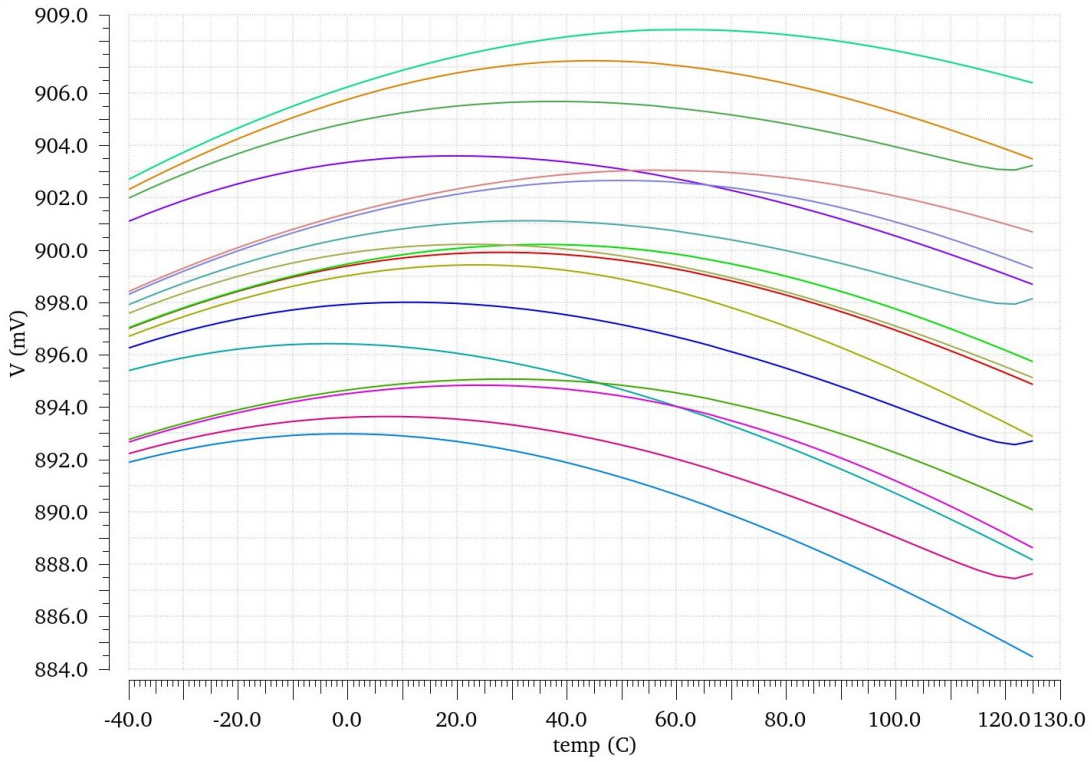

Figure 33: TC - process corners.

Inspecting the result, it is possible to conclude that all the corners display, more or less, the same curvature. Furthermore, the largest voltage variation takes place in the higher

temperatures.

According to Equation 2.2, and inspecting the corners simulation result in Figure 33, the temperature coefficients obtained are listed in Table 10.

Specification	Min.	Typ.	Max.	Unit
TC	21.5	33.6	57.2	ppm/°C
V_{REF}	884.5	900	908.5	mV

Table 10: Corners simulation results.

5.3.3 Power Supply Rejection Ratio

The PSRR is defined as the ability of the output voltage to reject the noise and other signals at specific frequencies on the power supply. This measure value can be obtained through an AC analysis. Where, after inducing a disturbance in the power supply source, the output of the circuit (V_{REF}) is examined in frequency. The result, for a 1 V disturbance in the power supply source, is represented in Figure 34, including the 16 corners and the typical corner (red).

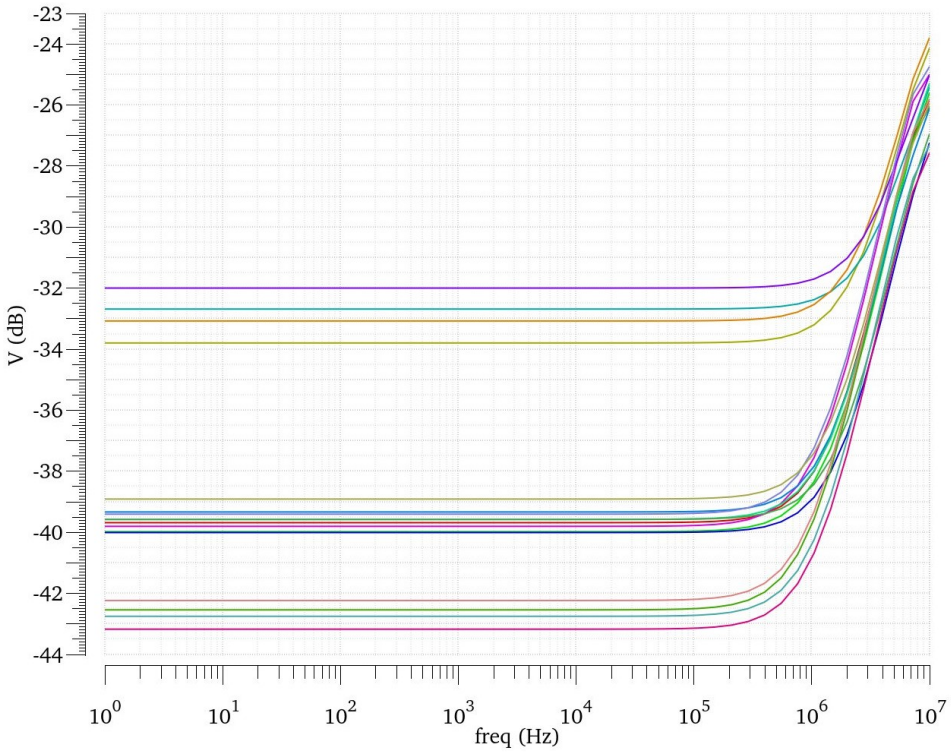

Figure 34: PSRR - process corners.

Inspecting the corners simulation result in Figure 34, the PSRR values obtained are listed in Table 11.

Specification	Min.	Typ.	Max.	Unit
PSRR @10Hz	-32	-39.7	-43.2	dB
PSRR @1MHz	-31.7	-38.2	-40.8	dB

Table 11: Corners simulation results.

5.3.4 Startup Time

The function of the startup circuit is, as the name suggests, to start the circuit and bring it to its normal operating point. In order to check if the startup is fulfilling its purpose, transient analyses are performed for various temperature values. It was decided to perform a transient analysis for the minimum, nominal and maximum temperatures of the range worked on. The results are represented in Figures 35, 36 and 37, respectively, including the 32 corners and the typical corner (red).

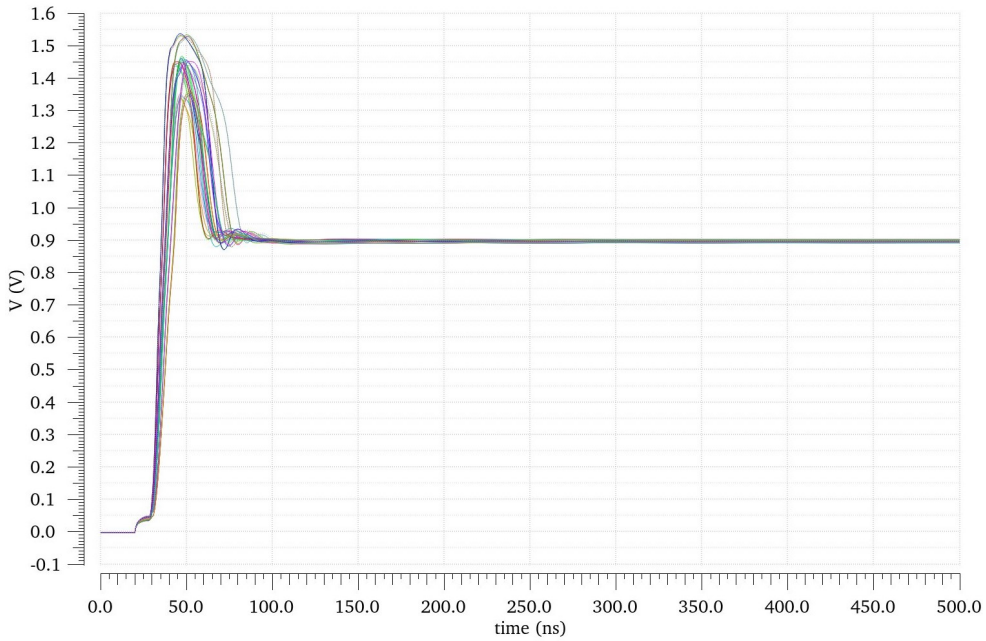

Figure 35: T = -40 °C - process corners.

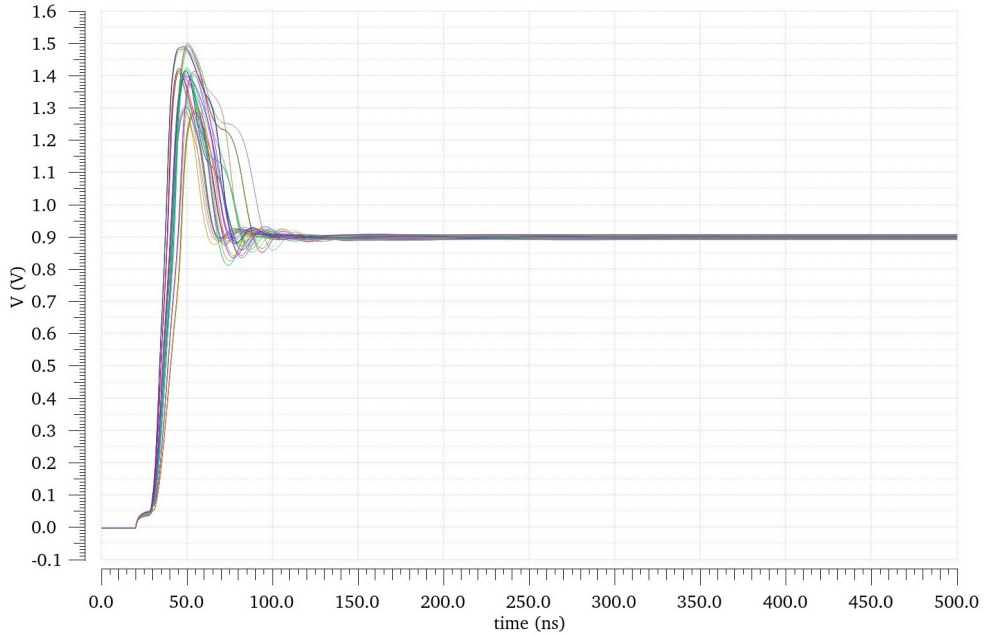

Figure 36: T = 27 °C - process corners.

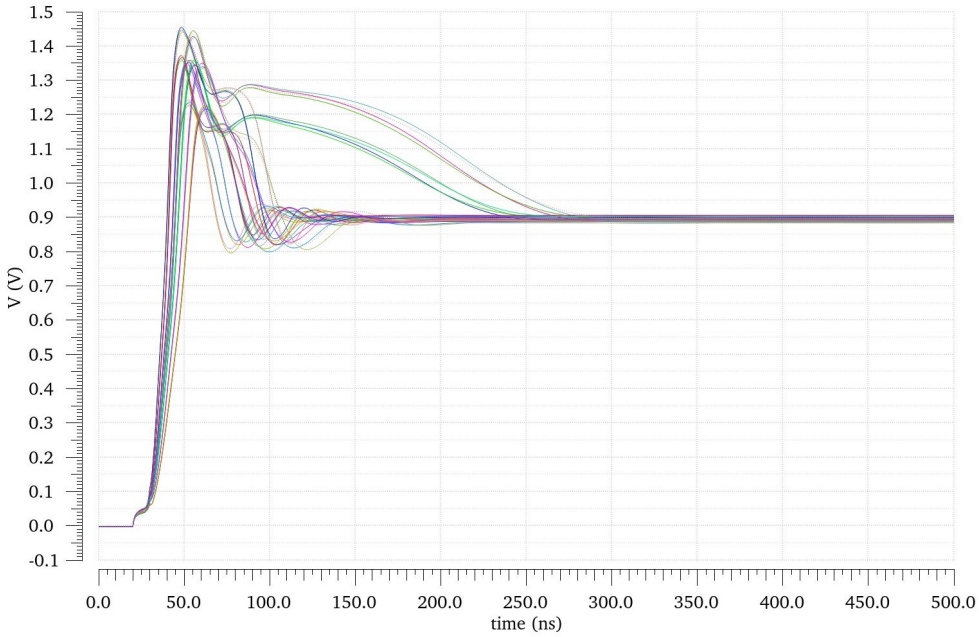

Figure 37: T = 125 °C - process corners.

Inspecting the corners simulation results, for the three different temperatures, it is possible to conclude that the startup circuit is performing its objective successfully in all cases. Additionally, the overall startup time obtained is around 325 ns, meaning the trimming vpulse sources delay time can not be lower than that.

5.4 Operational Amplifier Simulations

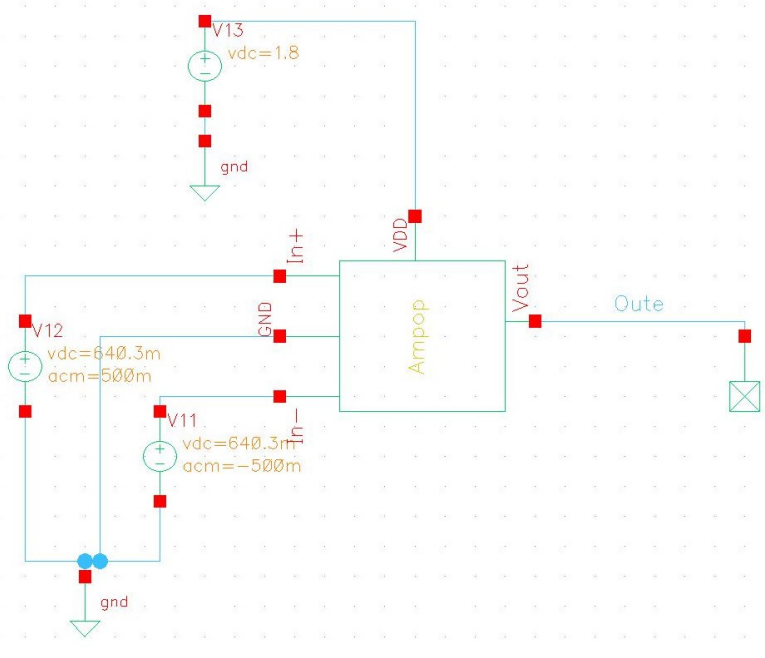

Figure 38: Opamp testbench.

In this section, the specifications of the opamp, used in the BGR circuit, are calculated through various simulations. The results obtained allow to characterize and compare the opamp implemented with other similar circuits.

The testbench used for this circuit is represented in Figure 38. As it is possible to see, the voltage source placed at the input, has a DC value of 640 mV, an AC value of 500 mV for the positive entrance and -500 mV for the negative one.

The DC value is 640 mV because it replicates the voltage in the branch of the original circuit, where the opamp will be placed. The values used for the AC parameters are 500 and -500 mV, to achieve a magnitude of the differential input signal of 1 V, which allows to extract the value of the gain straight from the output.

5.4.1 DC Gain and Bandwith

Through an AC analysis, by sweeping the frequency between 1 Hz and 100 MHz, it is possible to obtain the DC gain of the opamp and its bandwith, represented in Figure 39. Inspecting the graph, the DC gain of the operational amplifier is 53.4 dB and the bandwith is approximately 1.2 MHz, since it is the frequency range over which the voltage gain of the amplifier is above - 3 dB of it is maximum value.

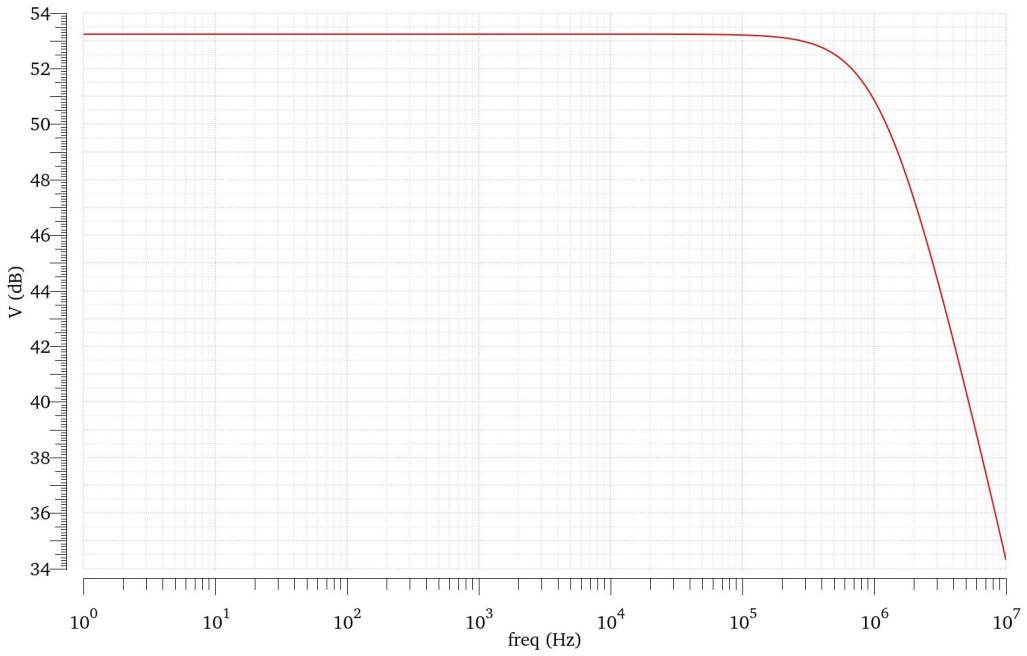

Figure 39: Frequency response.

Usually, a gain of around 60 dB is used in a bandgap, but it was concluded through multiple tests, that the value obtained is high enough to perform the opamp objective in the voltage reference circuit. A high gain is also desirable to maintain the stability of the close-loop, therefore additional simulations were needed in order to confirm it.

5.4.2 Stability and Phase Margin

The phase margin (PM) is the difference between the phase lag and -180°, and the system is stable when the phase margin is positive. According to the result in Figure 40, the value of the

phase when the gain is 0 dB, also known as phase lag, is -103°. The phase margin is PM = -103° - (-180°) = 77°, confirming the stability of the opamp.

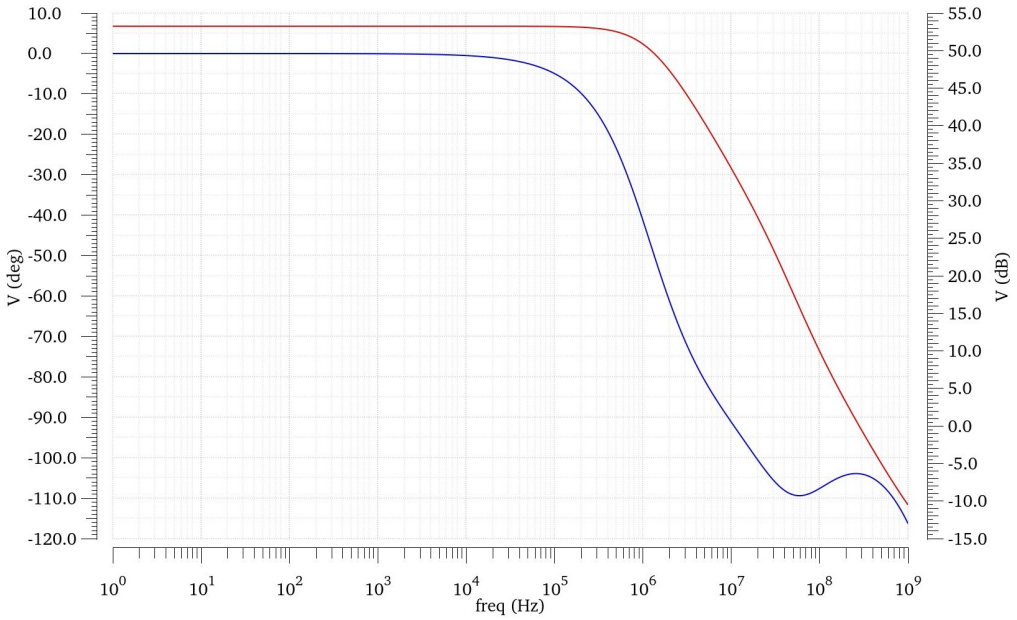

Figure 40: Gain (dB/red) and phase (°/blue).

5.4.3 Power Supply Rejection Ratio

In order to calculate the PSRR of the operational amplifier, the testbench in Figure 38 had to suffer some changes. The AC value of the input sources needs to be zero now, and the AC value of the power supply source equal to 1 V. With these modifications, the opamp will output the voltage variation for an AC disturbance in the power supply. The result in represented in Figure 41, in decibels (dB).

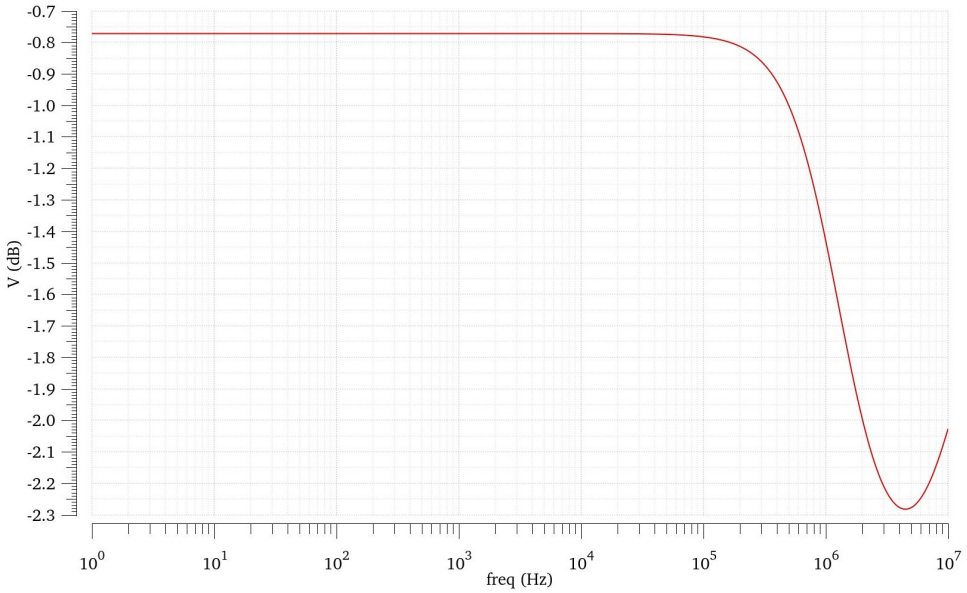

Figure 41: Output voltage variation.

Considering that the PSRR for an opamp is calculated through Equation 5.14.

$$PSRR = 20\log\frac{Gain(f) * V_{IN,AC}(f)}{V_{OUT,AC}(f)}, \tag{5.14}$$

which is equivalent to

$$\begin{aligned} PSRR &= 20\log(Gain(f)) + 20\log\frac{V_{IN,AC}(f)}{V_{OUT,AC}(f)} \\ &= 20\log(Gain(f)) - 20\log\frac{V_{OUT,AC}(f)}{V_{IN,AC}(f)}, \end{aligned} \tag{5.15}$$

where $\frac{V_{OUT,AC}(f)}{V_{IN,AC}(f)}$ is represented in Figure 41, in dB. The gain is also represented in dB in Figure 39. The PSRR value is given by difference between the gain and the output the voltage variation, and the result is represented in Figure 42.

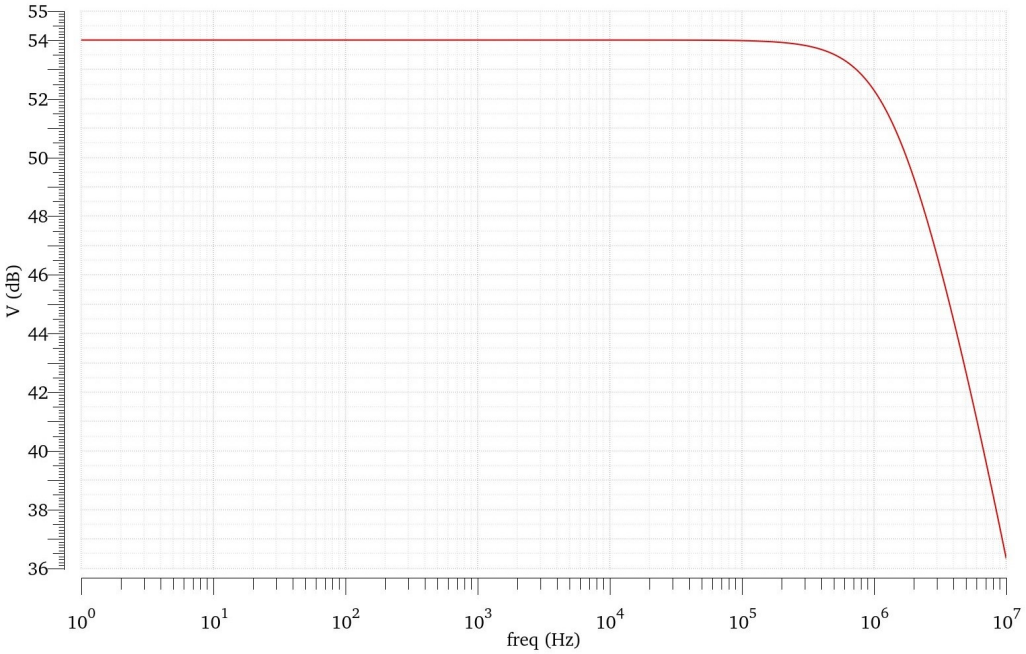

Figure 42: PSRR of the opamp.

The result obtained for the PSRR of the opamp is acceptable, however, its impact on the PSRR of the BGR circuit is not noticeable since it was obtained a solid result, and that is the more important measure of the two.

In summary, all the results obtained in this section are listed in Table 12. These are the specifications of the opamp implemented in the BGR circuit.

Specification	Value	Unit
DC Gain	53.4	dB
Bandwidth	1.2	MHz
Phase Margin	77	°
PSRR @10Hz	54	dB
PSRR @1MHz	52.3	dB

Table 12: Opamp specifications.

5.5 Voltage to Current Converter Circuit Simulations

5.5.1 With Off-chip Resistor

This section presents the results for the circuit using one of the options provided, the off-chip resistor. In order to perform the simulations, an analogLib's ideal resistor was used to reproduce the same effect as the external resistor. Remembering the testbench in Figure 28, the pin ExtR will now connect to GND and the ideal resistor, with a value of 900 kΩ, will be connected to the pin Trim_up.

The result of the DC analysis with a sweep in temperature between -40 °C and 125 °C, including the 16 corners and the typical corner, is represented in Figure 43.

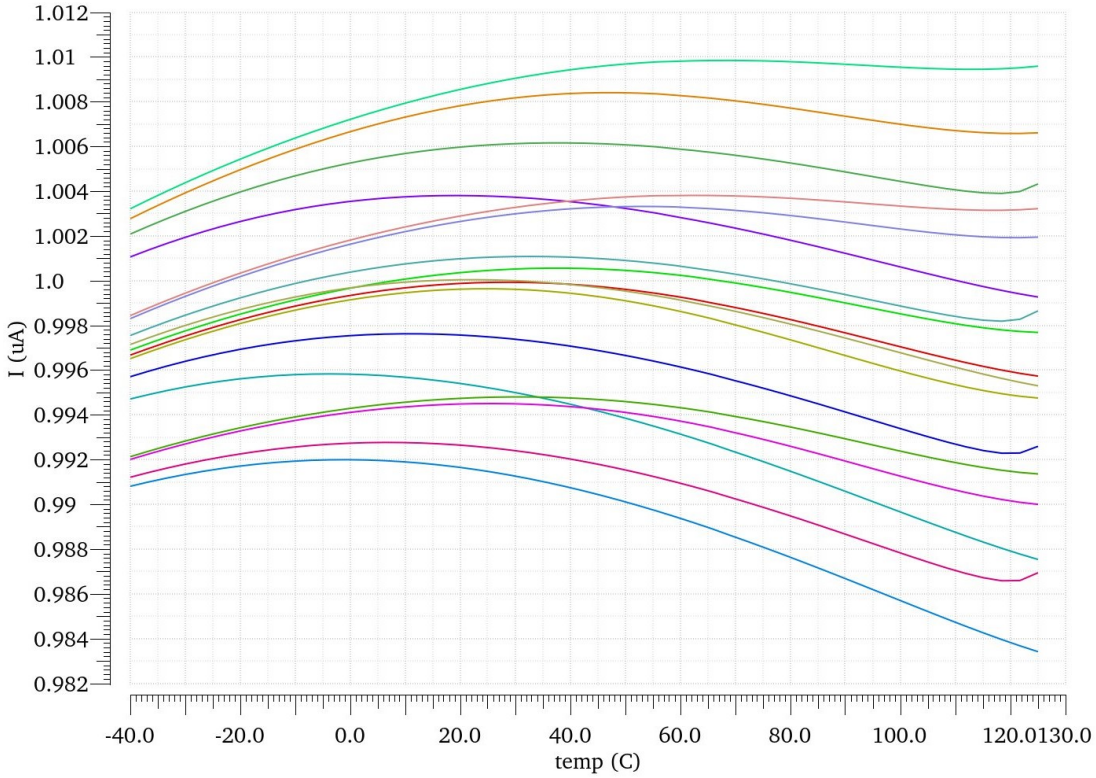

Figure 43: Current variation in temperature - process corners.

The obtained results display a total current variation of ΔI = 1.009 - 0.983 = 0.026 μA, which is equivalent to 2.6 %. Given the fact that the resistor used is ideal, it is safe to assume that most of the current variation obtained is due to the discrepancy in the reference voltage coming from the BGR circuit designed.

5.5.2 With Trimmed On-chip Resistor

In this section, it is presented the result of various simulations of the voltage to current converter circuit, using the alternative, an on-chip resistor. These results show the least possible variation in temperature suffered when using the on-chip resistor. For that, it is performed a transient analysis, where the current in the output I_{REF} is tested for all the 32 possible combinations from the five bits of the trimming circuit. In Figure 44, is represented the typical corner simulation result at nominal temperature, where the current reaches 1 μA at t = 40 μs, which corresponds to the digital word 10000. This analysis is repeated for the remaining 16 corners, and then replicated for the two other temperatures. The current peaks registered in the graph take place when the resistors are being turned ON or OFF. The greatest peak occurs at t = 40 μs, when the largest resistor (240 kΩ) is being short circuited by the switch, represented in Figure 44. All the results obtained are listed in Table 13.

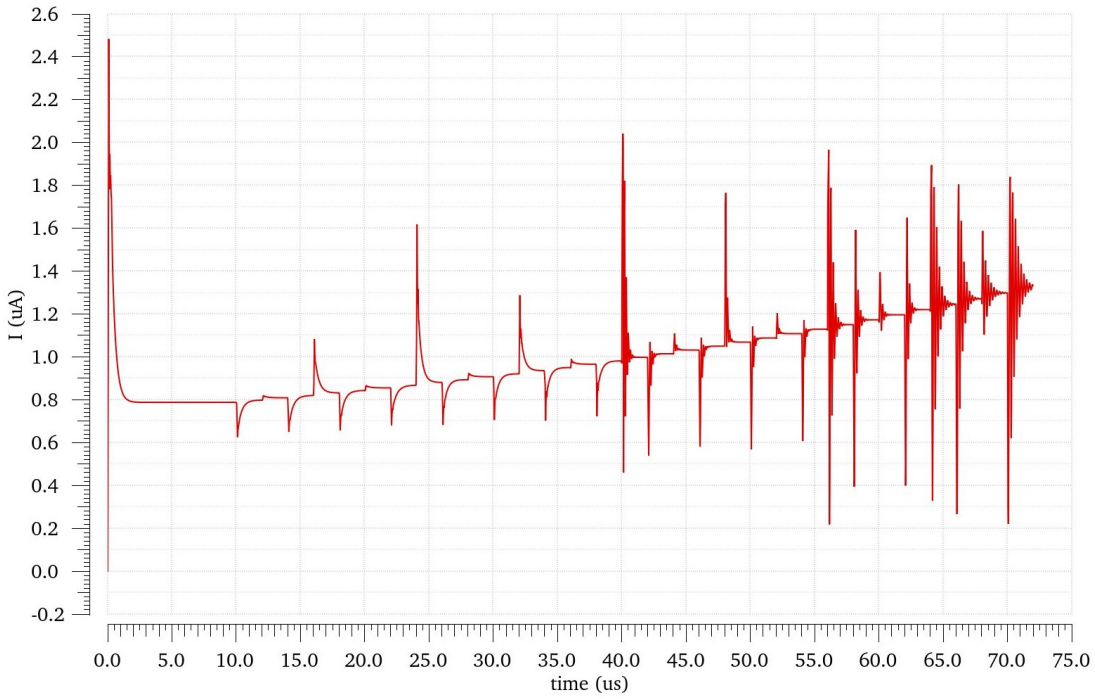

Figure 44: Transient analysis - typical corner.

According to Figure 44, there is oscillation in the latest iterations of the simulation, that occurs due to a smaller phase margin when the resistor has a lower resistance value. However, this is not an issue because the obtained results were not acquired from oscillating iterations, for any of the 17 corners. Even so, in order to confirm it, simulations were conducted to analyse the phase margin for different resistance values.

The phase margin (PM) value is calculated for the highest resistance value, which applies for the trimming word = 00000, through the graph represented in Figure 45. The phase is 26° when the gain reaches 0 dB, indicating a phase margin of PM = 26° - 0° = 26°, which represents a stable system.

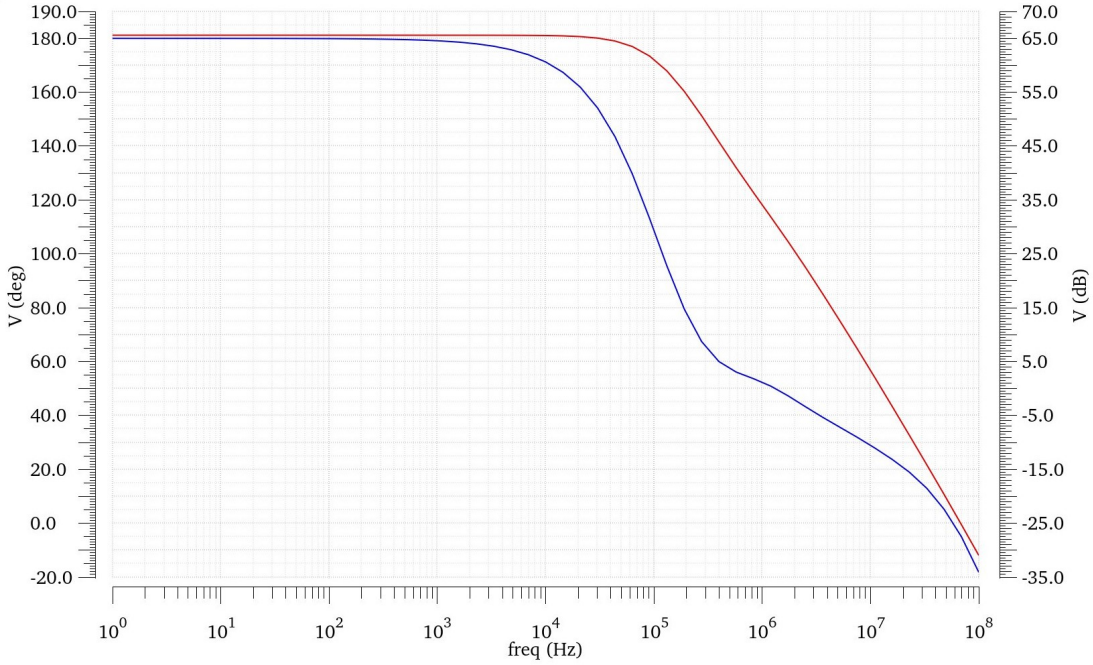

Figure 45: Gain (red) and phase (blue) for R = 1140 kΩ.

As previously stated, the phase margin value decreases for lower resistance values, producing the oscillation in the transient analysis. In order to confirm it, the simulation is repeated for the lowest resistance value possible, which applies for the trimming word = 11111.

According the Figure 46, the phase margin is PM = 8° - 0° = 8°. This value is lower, as predicted, which will result in a dumped oscillation. However, the value is still positive, meaning, the system is also stable for the lower resistance values.

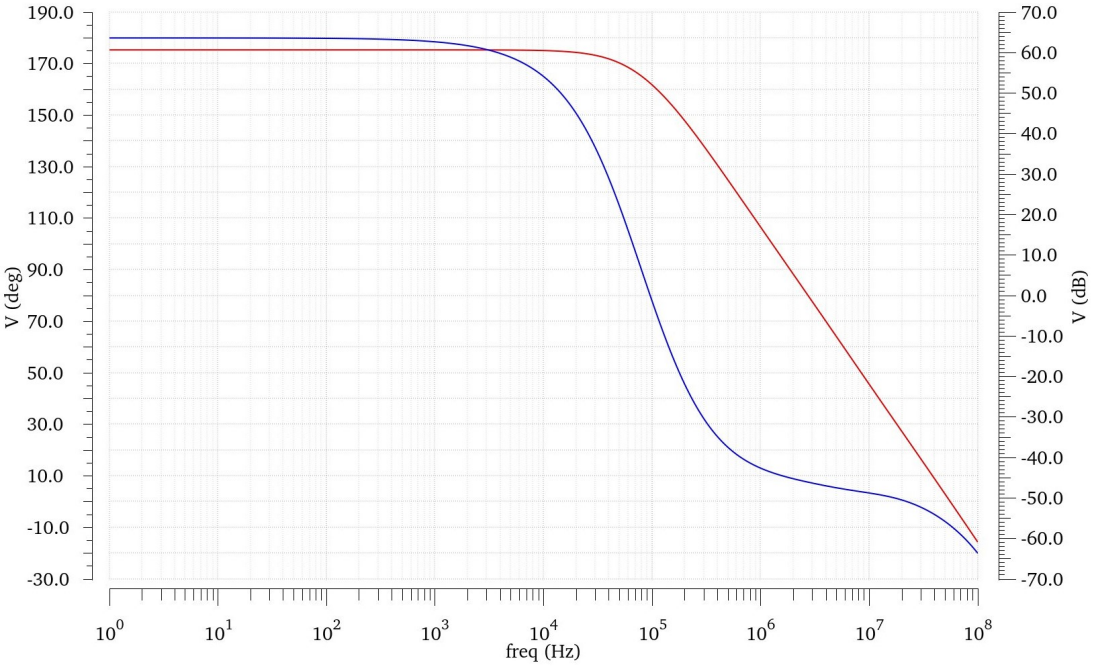

Figure 46: Gain (red) and phase (blue) for R = 675 kΩ.

Corner	Word	T = -40 °C	T = 27 °C	T = 125 °C	Unit
typical	10000	0.987	1.000	0.998	μA
corner0	00111	0.991	0.998	0.991	μA
corner1	00111	0.991	1.000	0.995	μA
corner2	00111	0.989	0.994	0.985	μA
corner3	00111	0.990	0.997	0.990	μA
corner4	11000	0.986	1.001	1.009	μA
corner5	11000	0.985	1.005	1.009	μA
corner6	11000	0.985	1.002	1.000	μA
corner7	11000	0.983	1.001	1.005	μA
corner8	00111	0.996	1.007	1.004	μA
corner9	00111	0.997	1.008	1.007	μA
corner10	00111	0.995	1.003	0.996	μA
corner11	00111	0.005	1.003	1.003	μA
corner12	11000	0.992	1.010	1.010	μA
corner13	11000	0.991	1.013	1.015	μA
corner14	11000	0.989	1.009	1.004	μA
corner15	11000	0.987	1.008	1.009	μA

Table 13: Corners simulation results.

The obtained results display a total current variation of ΔI = I_{MAX} - I_{MIN} = 1.015 - 0.983 = 0.032 μA, which is equivalent to 3.2 %. Recalling the TC of the technology resistor used and the overall variation of V_{REF} in temperature, these results are positive and are within the values expected.

The results registered using the off-chip resistor are very similar to the ones presented before, with the trimmed off-chip resistor. Taking that into account, it is possible to conclude that the trimming was well done and the variation registered is mostly due to the discrepancy in the reference voltage coming from the BGR circuit designed, where only 0.6 % is originated from the use of the trimmed on-chip resistor instead of the off-chip resistor.

6. Layout Design

The layout design starts with the floor plan of the system, as represented in Figure 47. The layout was configured to occupy the minimal total area, while maintaining symmetry to avoid, as much as possible, offset errors and mismatches. As seen in the figure below, it was decided to use a ratio close to one for the occupied space, resulting in a estimated area of 0.0625 mm^2.

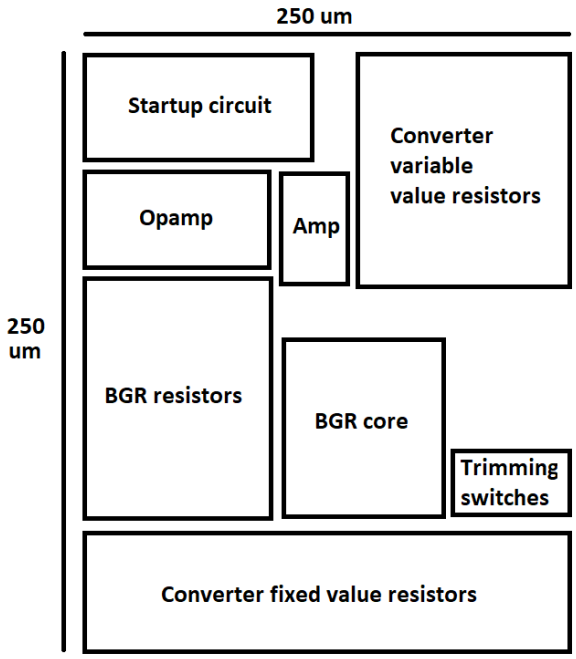

Figure 47: Floor plan of the layout.

This layout was hierarchically designed, e.g., it started with the design of the smaller individual blocks (opamp, startup, amp, resistors, etc), and after that, they were connected with each other and remaining components. The layout for these blocks will be presented in the following sections, along with an explanation for the techniques applied. All the layouts designed, and presented, respect the DRC rules and are compatible with the respective schematics, according to the LVS.

Throughout the design of the layout, any space left between the components will be filled with decoupling capacitors (DECAPs) [12]. Among power supply noise reduction techniques, inserting DECAPs is the most common practice. These capacitors hold a reservoir of charge, and are requested if a high current is being demanded. The DECAPs are made from NMOS transistors because they are the prime choice when area is a concern, whereas the PMOS transistors are used in low leakage applications.

Furthermore, if the transistors are NMOS, where the body is connected to GND, the guard ring surrounding them will be as well. In the case of PMOS transistors, the guard ring will be connected to VDD [13]. The main function of these guard rings is to polarize the transistors bodies, but will also help reduce subtract noise inside the system.

6.1 Sub-1V Bandgap Voltage Reference Circuit

6.1.1 BGR Core Circuit

The core of the BGR circuit is composed by the BJT pair, the current mirror and the resistors. First, it is applied a layout technique known as common centroid in the BJTs layout, where, as previously discussed, the transistor with multiplicity N = 8 is placed around the one with N = 1, resulting in similar adjacent structures for the inner element. The guard ring surrounding this group is connected to GND, since the BJTs used are NPN. The layout is represented in Figure 48.

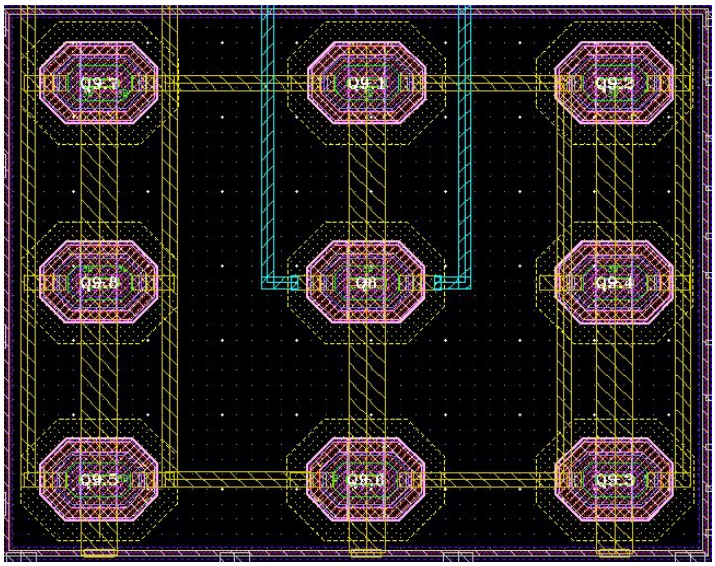

Figure 48: BJTs - layout.

Following that, the layout of the current mirror was planned. The transistors forming the current mirrors are compact, where each one has only one finger. Considering this, there is no real advantage in matching the transistors, hence, the layout can be done by just placing them side by side. The group is surrounded by a guard ring connected to VDD, since they are PMOS transistors. The layout is represented in Figure 49.

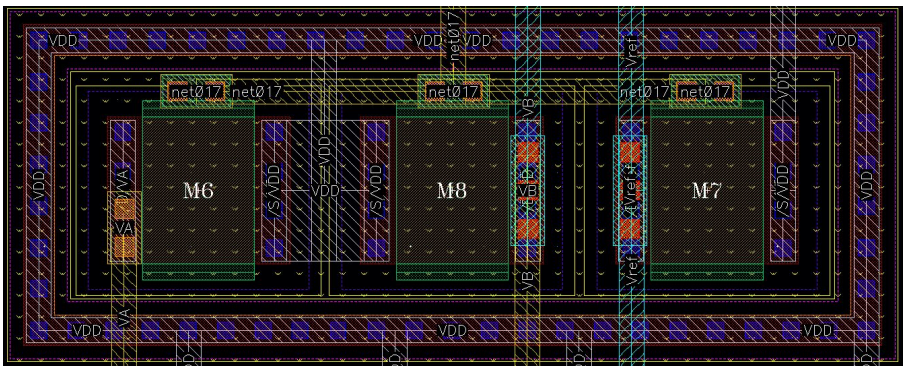

Figure 49: Current mirrors transistors - layout.

Lastly, the layout of the resistors is designed. Another layout technique is used, the matching of the resistors, in order to average the process variation between them. This can be performed by dividing each resistor into many unit resistors, and then inter-digitized them. Considering that there will be different dopant diffusion between the unit resistor at the edges of the inter-digitized and the common-centroid layout, this will lead to mismatch and is known as the end effect problem. This problem can be alleviated by placing dummy elements on the edge of the resistor layout to compensate the doping concentration difference by ensuring the unit resistors of the matched resistors have the same adjacent structures.

To reduce the impact of substrate noise on the resistors, the resistor network is surrounded by a guard ring, connected to GND, to avoid unpleasant electrical characteristics that may affect the circuit. An example of matching the resistors layout is represented in Figure 50, noting that future references of this technique were performed similarly.

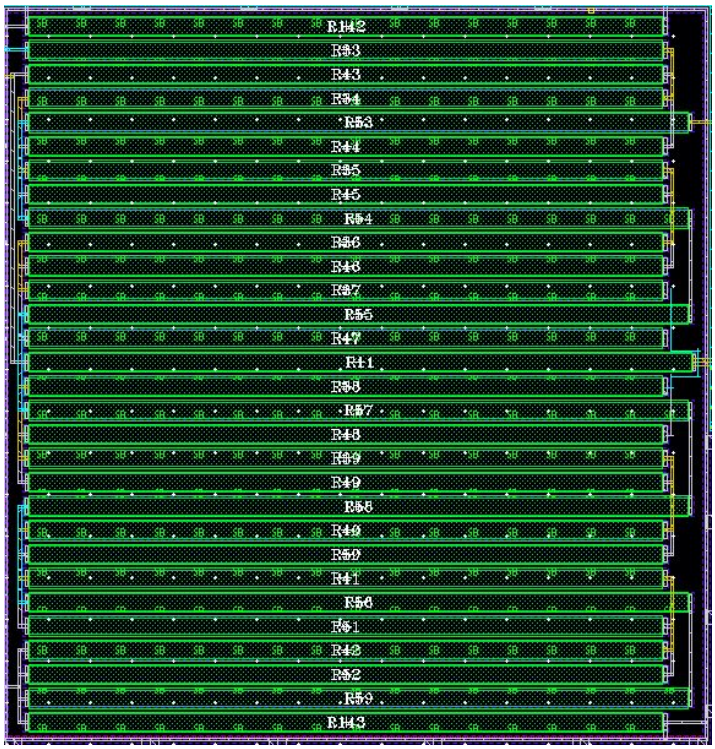

Figure 50: Matching of the resistors - layout.

6.1.2 Operational Amplifier

The layout of the operational amplifier used in the BGR circuit is represented in Figure 51. The resistor used is designed in a serpentine pattern due to its high resistance value and can not be matched since is the only resistor in the circuit. This option will minimize the area occupied, and by dividing it in a even number of fingers, the connections will be made in the same direction. After that, the PMOS transistors forming the current mirror are designed side by side, since there is no need to matching them due to their compact size. These are represented in the top right.

The NMOS transistors forming the differential pair can be matched since they have a common source, thus, the process variations among them will average out. The matching performed is according to the common centroid technique, where both components will have the same centroid. Considering both transistors (represented by their gates: A and B), and

given that each one has four fingers, the matching result is: A A B B B B A A, as represented in the middle right. The last components to be designed are the NMOS transistors forming the current mirror, part of the tail current source. The same matching technique is applied to this pair, however, in this case, the transistors have an odd number of fingers. The width value of one is 25 μA, meaning that it has five fingers of 5 μA, and the other has W = 15 μA, resulting in three fingers. Taking that into account, it was decided to add a dummy element to each one, thus each one has an even number of fingers. This would result in a total of ten fingers, and the matching configuration: A A A B B B B A A A, as represented in the bottom right. All the MOSFET pairs are surrounded by their respective guard ring, connected accordingly.

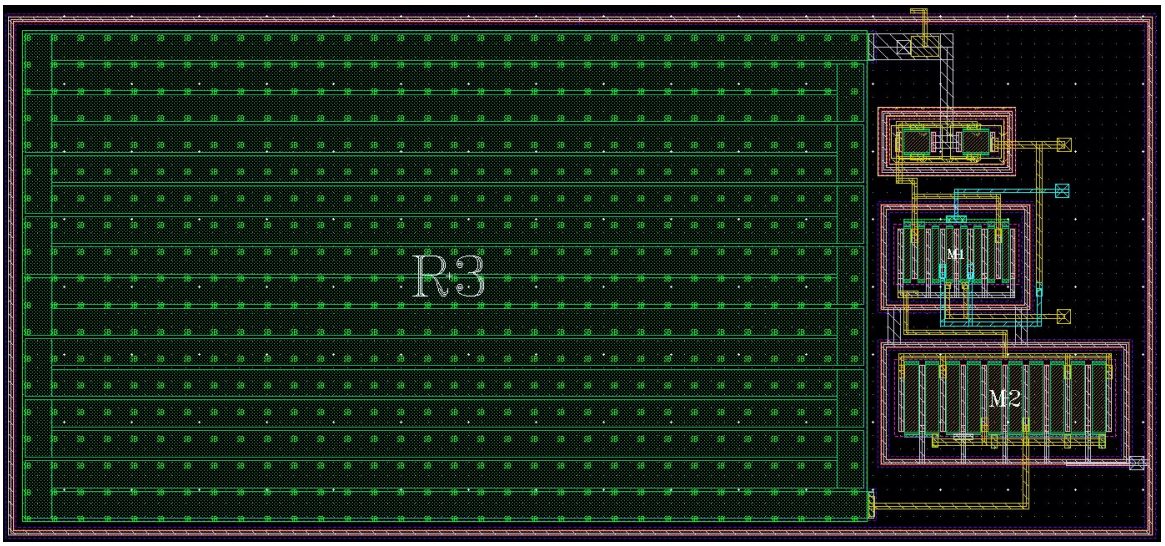

Figure 51: Operational amplifier - layout.

6.1.3 Startup Circuit

The layout of the startup circuit used in the BGR circuit is represented in Figure 52.

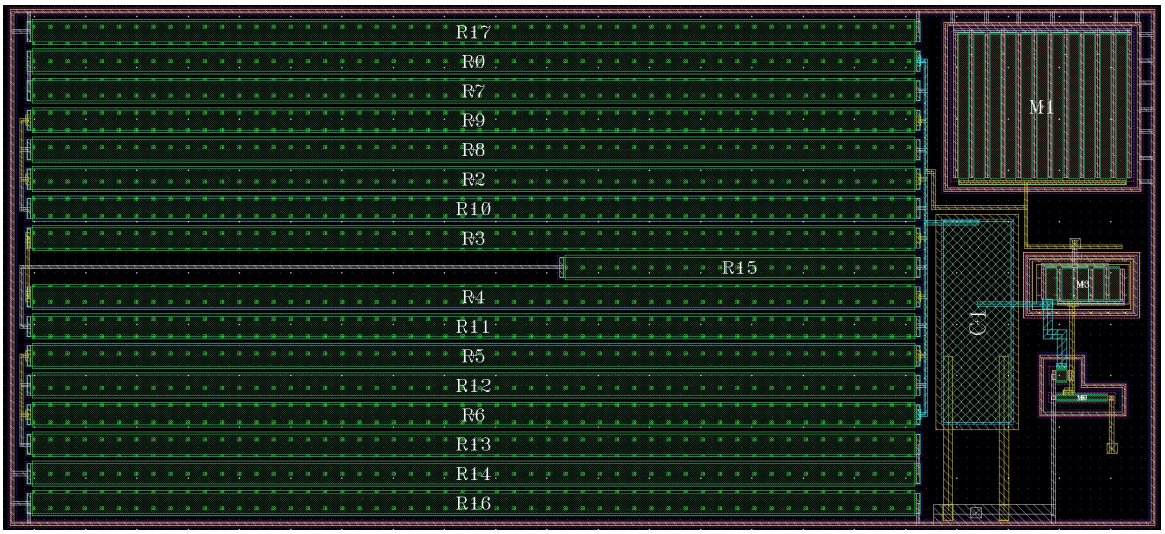

Figure 52: Startup circuit - layout.

The two resistors forming the resistive divider are matched, using the same method explained for the resistors in the BGR core. Apart from that, the transistors are placed close to others of the same type, for then to be surrounded by their respective guard ring, connected accordingly. The MIM capacitor is also represented, with its two connections, one net linking the output of the voltage divider and the input of the inverter, and another to ground. Lastly, it is possible to see the DECAP implemented in the top right of the layout, filling the area that was left out.

6.2 Voltage to Current Converter Circuit

6.2.1 Amplifier

The layout of the amplifier used in the voltage to current converter circuit is represented in Figure 53. This circuit is composed by two pairs of transistors, with both of them being matched. The PMOS pair forming the current mirror has a total of eight fingers, therefore, the matching configuration is: A A B B B B A A, as represented in the top of the figure. The NMOS pair is composed by two transistors with two fingers each, thus, one of the possible matching configuration is: A B B A, as represented in the bottom of the figure. Noting that both pairs are surrounded by their respective guard ring, as previously explained.

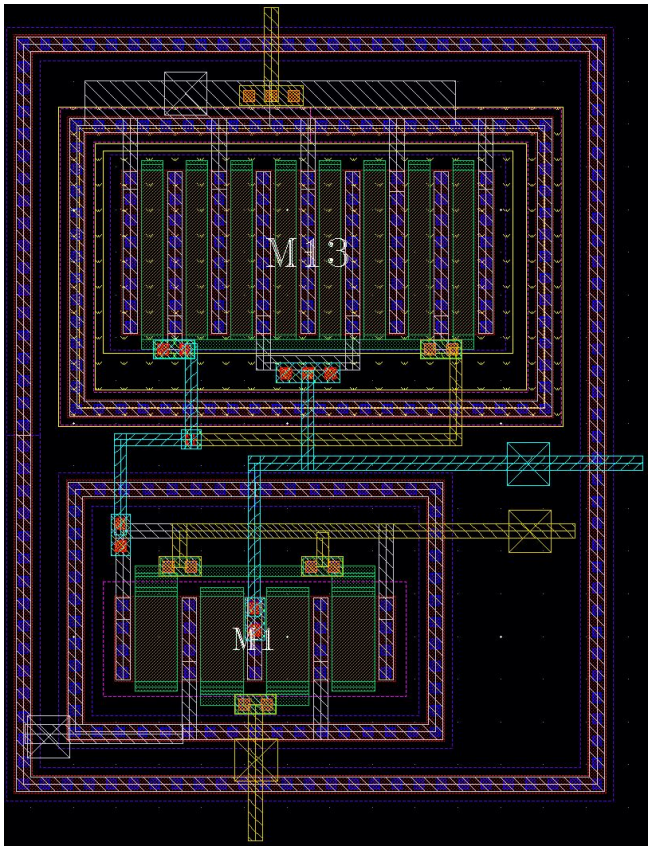

Figure 53: Amplifier - layout.

6.2.2 Trimming Circuit

The rest of the components used in this circuit make up the resistor trimming, and they are: fixed value resistors, variable value resistors and the NMOS switches.

Both resistors components, fixed and variable, are matched using the same method explained for the resistors in the BGR circuit core. In the NMOS switches case, the matching is not possible because the transistors do not have a common terminal between all of them. And for that reason, they are placed side by side in the layout, as close to each other as the DRC allows.

6.3 System Layout

This system layout is the result of the assemble all the blocks presented in the preceding section, as it is represented in Figure 54. Evidently, the disposition follows the floor plan proposed. The layout area obtained is 0.058 mm^2, where the length is L = 258 μm and the width is W = 224 μm, preserving a ratio close to 1, as desired.

Furthermore, it is visible the presence of decoupling capacitors made from NMOS transistors. These DECAPs are filling all the space left between the blocks, and for that reason, each one has its set of dimensions. Each one of these capacitors is surrounded by a guard ring connected to GND, since they are made from NMOS transistors.

Every single block in the layout is surrounded by a guard ring, either connected to GND or VDD. A precaution taken was to connect all guard rings of adjacent blocks, if both connected to GND/VDD.

Additionally, around the system layout there are two guard rings, one outer ring for VDD and one inner ring for GND. These rings are double the width of the ones used in the sub-circuits, and are now formed with two rows of contacts instead of one, to achieve better performance. These guard rings will isolate the system noise, by stopping it to propagate to neighbours systems, as well as ease the connection to VDD and GND inside the circuit. The layout is represented in a separate page, for better visibility, enabling the possibility to discern all the details.

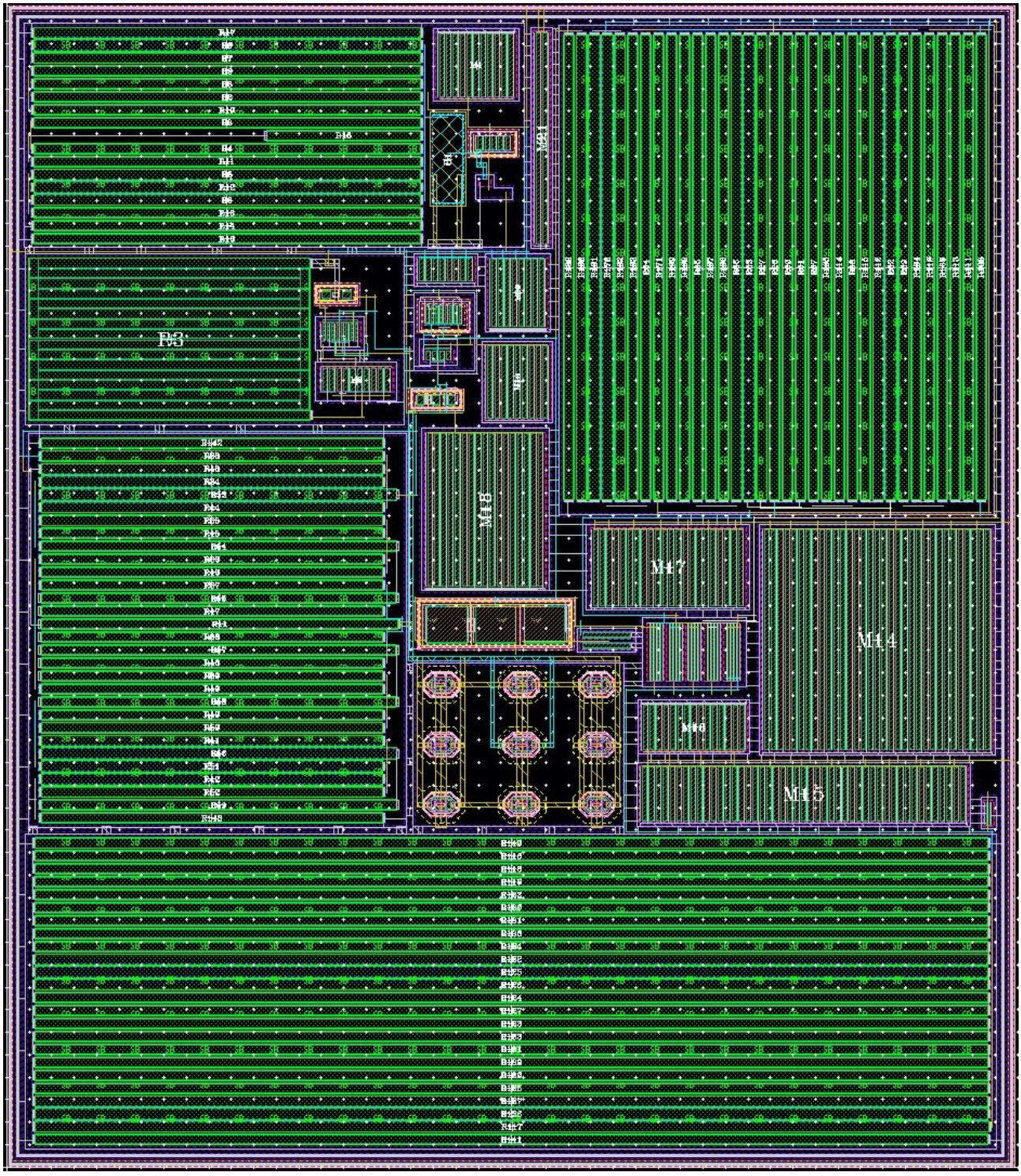

Figure 54: System - layout.

7. Post-layout Results

In this section, the post-layout results of the system are calculated through similar simulations and using the same testbench, however, they are achieved utilizing the layout extraction.

Before extracting the layout, it is performed the DRC and LVS, both part of Calibre. The DRC checks if there are any design rules that are being broken, e.g., minimum space between metals, between components, etc. The LVS, or Layout vs schematic, checks if the layout designed is connected and placed accordingly when compared to the source, the schematic. The DRC result obtained is a blank screen, meaning that there are no warnings or errors in the layout designed, the LVS result is represented in Figure 55. According to it, there are no errors, therefore the layout is ready to be extracted.

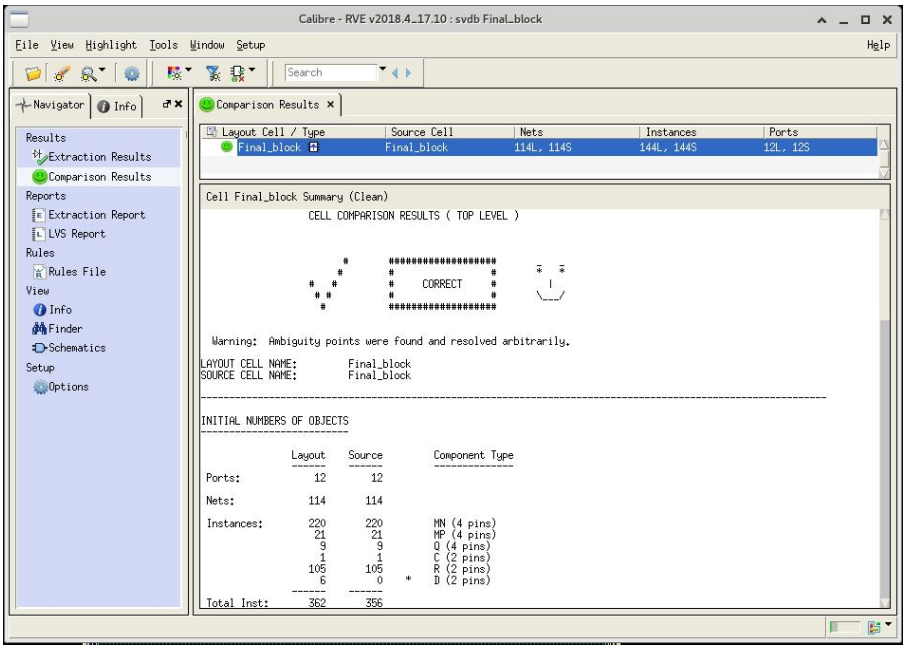

Figure 55: System - LVS.

The extraction of the layout is done through PEX, also part of Calibre. This tool will extract the netlist from the layout, however, it includes parasitic resistances and capacitances. The extracted layout is then simulated similarly to the schematic, and the results of all the simulations performed are listed in Table 14 alongside the ones obtained in section 5, from the schematic.

	Schematic			Layout			
Specification	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
LR	0.42	0.57	1.43	0.45	0.57	1.32	%
TC	21.5	33.6	57.2	20.8	35.0	59.2	ppm/°C
V_{REF}	884.5	900	908.5	882.7	898	906	mV
PSRR @10Hz	-32	-39.7	-43.2	-38.2	-45.7	-51	dB
PSRR @1MHz	-31.7	-38.2	-40.8	-34.6	-39	-42.7	dB
I_{REF} (w/ on-chip R)	0.983	1.000	1.015	0.980	0.997	1.013	μA
I_{REF} (w/ off-chip R)	0.983	1.000	1.009	0.980	0.997	1.006	μA

Table 14: Corners simulation results - schematic vs layout.

Apart from the performance measures displayed, the startup circuit was also analysed in this new environment. Through multiple transient analyses, it was concluded that the behaviour was similar to the one seen using the schematic of the circuit, e.g., it started the circuit and brought it into its normal operating point in all 32 process corners, for the three different temperatures. Lastly, it was calculated the system current consumption, because, even though it was not a concern, it is important to get represent its value. The current consumption obtained for the system is 137.1 μA.

As a way of getting a deeper understanding of the BGR obtained results, the Table 15 is comparing the post-layout results with various other works published.

Specification	This work	[14]	[15]	[16]	[17]
Supply voltage (V)	1.8	1.2	1.6	2.3	1.5
Current (μA)	66.89	50.4	17	40	1.1
Temp. range (°C)	-40 to 125	0 to 100	-65 to 140	-40 to 120	-40 to 100
Reference voltage (V)	0.898	0.72	1.202	0.8	0.6
Avg. TC (ppm/°C)	35	53.1	9.9	54	4.4
Best TC (ppm/°C)	20.8	43.5	–	–	4.4
PSRR @10Hz (dB)	-45.7	-51	-57.7	-120	-100
CMOS process (nm)	180	90	250	350	130
Chip area (mm^2)	0.058	0.028	–	0.024	0.04

Table 15: Comparison with other BGR circuit publications.

The works selected for this comparison are within the past ten years, and more importantly, have similar supply voltages, temperature ranges and reference voltage values.

The first parameter is the current measured at the power supply voltage, also known as current consumption. The higher current consumption when compared to the other works listed can be justified by the fact that this parameter was not a main concern when designing the system and it was not even defined a target value, also worth noting that the consumption value measured refers to the BGR, not including the converter circuit, in order to make the comparison on equal terms.

The TC average value simulated is approximately equal to the one in the others publications, with the exception of reference [17]. That work presents a temperature curvature compensation method, which will lower the voltage dip, seen in Figure 32, for higher temperatures, resulting in a lower total voltage variation and consequently a lower TC value. The reference [15] also presents a low TC value for the exact same reason, but by applying a different compensation method, this time resulting in a "M" shaped graph of the reference voltage in temperature.

The same occurs when analysing the PSRR specification, where one case stands out, reference [16], because that work was specifically designed to achieve a very high PSRR value. As for the area occupied, the higher value is mainly due to the trimming performed to the resistor in the voltage to current converter circuit.

8. Conclusion

This master thesis has explored the process involved in the design of both a sub-1V bandgap voltage reference circuit and a voltage to current converter circuit, all in one system. This system had to accomplish the specifications imposed, and deliver acceptable results in the rest of the performance measures. This last chapter includes the final conclusion regarding the work done, the results obtained and a discussion about the future work that can still be done in the system designed.

8.1 Results Analysis

The system was designed in a 180 nm conventional CMOS process technology. In the case of the BGR circuit, simulated results have shown temperature coefficients as low as 20.8 ppm/°C over a temperature range of 165 °C (-40 °C to 125 °C). Additionally, the circuit displays a PSRR of -45.7 dB at low frequencies and -39 dB at 1 MHz. The converter circuit presents a process corners current variation of 3.2 %, for the same temperature interval. The system current consumption is 137.1 μA. Taking that into account, it is possible to say that all the objectives established at the beginning of this project were accomplished and the results attained are considered satisfactory. An overview of the stages completed during this project is listed below.

- Study of the state of the art for similar circuits.
- Selection of the topologies to implement.
- Creation of the schematics using the technology proposed (CMOS 180 nm).
- Assembly of the testbenches and simulations to be performed.
- Analysis of the pre-layout results.
- Layout design.
- Layout validation through DRC and LVS.
- Analysis of the post-layout results and comparison with the pre-layout ones.

Every sub-circuit implemented in this project was sized to correctly operate in collaboration with the other blocks to obtain the final result, the voltage and current references. This thesis work allowed to learn how to perform a complete analog integrated circuits design flow.

8.2 Future Work

Considering the specifications of this work satisfactory, the next step is performing a Monte Carlo simulations and, in case the results are acceptable, proceed to the manufacturing process, e.g., the fabrication of the chip designed. After the chip fabrication, it is proposed to re-evaluate the system performance parameters and compare them with the values measured at the layout level. Allowing a good insight of the real differences between the simulator level and the fabricated chip.

However, even if the results meet the desired values, there are still improvements that can be done to the system implemented. The decisions taken to not implement those techniques

were based on the performance, complexity, available time and a possible inexperience in the field.

One of the critical blocks of the BGR circuit is the operational amplifier, designed to force the voltages at the inputs to be equal. The improvement that could be done is, as previously discussed, replace the resistor with a PMOS transistor, by applying the bootstrap technique. It is believed that, if applied correctly, this technique would improve the PSRR of the opamp, which is its weakest specification. Additionally, it would decrease the size of the block and the system, since the resistor to be replaced is, according to the layout in Figure 51, the largest component of the opamp. Another improvement that could be implemented is the use of a cascode configuration instead of basic current mirrors in the BGR circuit, ensuring a better mirroring of the current, probably resulting in a lower TC value of the reference voltage, and consequently the current. Furthermore, even if not a main concern, the current consumption of the BGR circuit is slightly above average. One way to improve this specification is by utilizing resistors with higher resistance values, although this would result in a higher chip area, which was already substantial.

One last possible modification is related with the amplifier used in the voltage to current converter. The amplifier used could be replaced by an operational amplifier, similar to the one used in the BGR circuit. This would result in a more reliable amplifier less affected by its transistors impairments. This would be observed in a Monte Carlo simulation. However, this change would result in a slightly higher chip area, as the resistor occupies the largest space in the circuit, as seen by the BGR opamp's layout in Figure 51.

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