Sub-1V Bandgap Voltage Reference Circuit and Voltage to Current Converter

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***Abstract*—This thesis explores the design steps of a Bandgap Voltage Reference (BGR) circuit and a voltage to current converter, implemented in one system. Both circuits are crucial blocks for high performance and reliable circuits, with a wide range of applications in many fields from analog to digital circuits. This work contemplates the design of the various sub-circuits which integrates both the BGR circuit and the voltage to current converter, including trimming sections, to improve the performance in all conditions that the system might be exposed to.**

The system was designed in a 180 nm conventional CMOS process technology. In the case of the BGR circuit, simulated results have shown temperature coefficients as low as 20.8 ppm/°C over a temperature range of 165 °C (-40 °C to 125 °C). Additionally, the circuit displays a PSRR of -45.7 dB at low frequencies and -39 dB at 1 MHz. The converter circuit presents a process corners current variation of 3.2 %, for the same temperature interval. The system current consumption is 137.1 μA.

I. Introduction

IN the field of electronics, the circuits always consist of different blocks, each one with a specific function that performs a desired task when working together. A very important block, and one of the most used, is the reference block. This reference block is responsible for generating accurate DC voltages and current, independent of variations in the process manufacturing, supply voltage and temperature (PVT).

The evolution seen in the field of electronics is immense, especially during the 20th century. Reference blocks performance and reliability developed consequently, with the creation of new topologies, techniques or just by adding different devices. Nowadays, the reference block is essential in almost every electronic equipment, them being control systems, supply sources and others. The system to be implemented takes part in a bigger project, developed by a group from INESC-ID. It was asked to develop two reference circuits, one is a voltage reference circuit and the other a current reference.

The system is supplied by a voltage of 1.8 V. The reference voltage desired value is 900 mV, and presenting a total variation in the process corners below 5 % in the temperature range of 165 °C (-40 °C to 125 °C). The reference current desired value is 1 μA, with a similar variation in the same temperature interval. These are the main goals to be achieved, the rest of the performance measures are expected to deliver acceptable results.

II. Background and Motivation

A. Voltage Reference Circuit

The voltage reference circuit is a system that generates a constant output voltage, which in theory, does not depend on the operating voltage, load current, temperature, or time.

This circuit is categorically different from the voltage regulator but with similar objectives, as both circuits generate regulated output voltages that are immune to the changes listed before, however, the accuracy is what distinguishes them. The voltage regulator presents a higher output current, resulting in a less precise output signal, higher output noise and unspecified long term stability.

Voltage reference circuits are used in all circuits that require a precise voltage, such as high resolution A/D and D/A converters, battery management systems, digital meters, smart sensors and many others.

B. Bandgap Voltage Reference Circuit

Bandgap Voltage Reference, or BGR, is the most commonly applied voltage reference circuit for bipolar and CMOS technology. One of the first, and most popular, bandgap circuits is known as Widlar bandgap voltage reference circuit, presented by Robert Widlar at the National Semiconductor in 1971 [1], and was first implemented in a commercial integrated circuit, named LM113. The idea behind the topology of this circuit is the compensation of a PTAT voltage and a CTAT voltage to reach a reference voltage with zero TC. For this, a weighted sum between these two voltages, such that

$$V_{REF}(T) = m_1 V_{PTAT}(T) + m_2 V_{CTAT}(T) \tag{1}$$

in order to get

$$\frac{\partial V_{REF}(T)}{\partial T} = m_1 \frac{\partial V_{PTAT}(T)}{\partial T} + m_2 \frac{\partial V_{CTAT}(T)}{\partial T} = 0 \tag{2}$$

For certain values of m_1 and m_2, and noting that $\frac{\partial V_{PTAT}(T)}{\partial T} > 0$ and $\frac{\partial V_{CTAT}(T)}{\partial T} < 0$, a near zero TC reference voltage can be obtained, as shown in Figure 1.

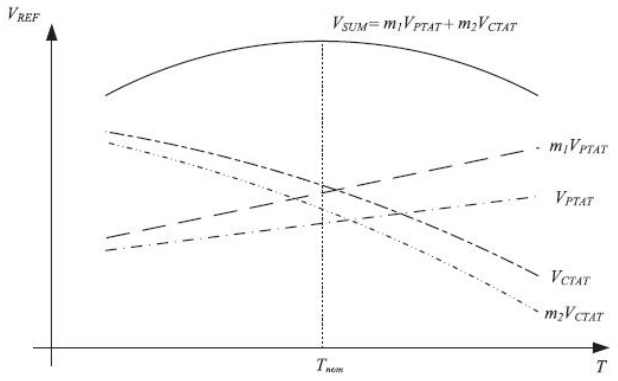

Figure 1: Temperature variation of reference voltage as a sum, from [2].

The compensated voltage obtained $V_{SUM}(T)$ is said to be a near zero TC voltage if $\frac{\partial V_{SUM}(T)}{\partial T} = 0$, at temperature T = T_{nom}. The CTAT voltage, in the Widlar bandgap voltage reference circuit, is formed by the V_{BE} of a BJT, while the PTAT voltage is formed by V_T extracted from ΔVBE of two BJTs biased with the different current densities.

According to Equation 1, a near zero TC reference voltage can be obtained by the weighted sum of V_{BE} and V_T, where

$$V_{REF}(T) = V_{BE}(T) + MV_T(T) \tag{3}$$

Differentiating the equation in temperature

$$\begin{aligned} \frac{\partial V_{REF}(T)}{\partial T} &= \frac{\partial (V_{BE}(T) + MV_T(T))}{\partial T} \\ &= \frac{\partial V_{BE}(T)}{\partial T} + M\frac{\partial V_T(T)}{\partial T} \end{aligned} \tag{4}$$

A BGR circuit, where the output is given by Equation 3, is known as a first order compensation circuit. In summary, the Widlar bandgap voltage reference circuit shows that if a CTAT voltage is summed with a PTAT voltage that has been scaled appropriately, such that both the CTAT voltage and the scaled PTAT voltage have the same temperature characteristic in magnitude, then a voltage that is almost independent of the operating temperature is obtained. Most of the BGR topologies are based on this principle, and the group which the circuit implemented belongs to will be discussed in the next section.

C. Sub-1V Bandgap Voltage Reference Circuit

Conventional BGR circuits are neither suitable for low voltage applications, nor for generating low reference voltages. The restriction on designing a sub-1 V reference voltage is the bandgap voltage itself. As previously discussed, a near zero TC voltage is generated by properly scaling the PTAT thermal voltage V_T with the weighting factor M, and summing it up with the CTAT voltage V_{BE} of the bipolar transistor. The value of the factor M is related to the thermal coefficient of V_T (e.g., $\frac{\partial V_T(T)}{\partial T}$) and the thermal coefficient of V_{BE} (e.g., $\frac{\partial V_{BE}(T)}{\partial T}$). The weighting factor M has to be greater than $\frac{\partial V_{BE}(T)}{\partial T} \Big/ \frac{\partial V_T(T)}{\partial T}$. Taking that into account, a sub-1V reference voltage can be achieved by lowering the factor M, either through reducing difference between the thermal coefficients of the CTAT term and the PTAT term, or by using different thermal devices to lower the induced thermal voltages.

There are various methods in the literature that have the purpose of reducing the magnitude of the CTAT and PTAT terms to obtain the desired low reference voltage, such as the resistive division. There are also a lot of methods in the literature to reduce the thermal coefficients of the CTAT and PTAT terms, such as threshold voltage based compensation [3] and using depletion transistors [4]. The resistive division method is widely used, it has been employed in many BGR circuits, however, these circuits use multiple resistors which will inevitably increase the chip area. The threshold voltage compensation method is another approach, which makes use of the thermal properties of the threshold voltages $V_{th,n}$ and $V_{th,p}$ of MOSFETs with transistors biased in the saturation region.

This technique allows a more compact voltage reference circuit, and is also robust to process variation. However, because of the supply voltage variation and channel length modulation effect, these circuits usually suffer from a degraded PSRR performance. In summary, in order to produce a sub-1 V reference voltage, one of these methods must be applied. The one chosen and the topology adopted will be thoroughly explained in the circuit design section.

D. Current Reference Circuit

The other main objective of this work is to generate a reference current, e.g., a PVT independent current. Current reference is also an essential block to provide internal bias current for other analog circuits with low TC, and low sensitivity to supply voltage variation.

This second part of the project began with the study of an isolated circuit that could deliver the desired result. The first studied circuit is the well known beta-multiplier current reference [5]. This circuit is an example of positive feedback use, since, with the addition of the resistor the closed loop gain is lowered (a positive feedback system can be stable if its closed loop gain is less than one). However, if the size of the resistor is decreased, the loop gain increase will push the feedback system closer to instability.

It was decided to design and simulate this circuit, with the addition of a differential amplifier to the circuit to

compare the drain voltage of NM0 (V_{biasn}) with the drain voltage of NM1 (V_{reg}) and regulate them to be equal. The transistors NM2, NM3 and PM3 form the startup circuit. Resulting in the circuit in Figure 2.

After testing, it was concluded that this topology was not appropriate for this application. The behaviour of the reference current in temperature and process corners was simulated, and the results were unsatisfactory. According to the simulations done, the circuit main objective is to generate a current stable with power supply voltage variation, which is not suitable to the proposed objectives. Taking that into account, and after analysing others isolated circuits solutions with similar results, it was concluded that another approach had to be taken.

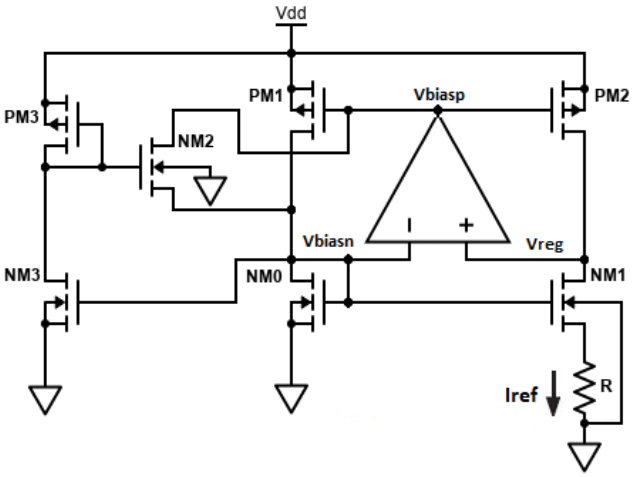

Figure 2: Improved current reference circuit.

The solution adopted was to make use of the BGR circuit already designed at that point, and its superior PVT sensitivity. The topology implemented is thoroughly explained in the circuit design section.

III. Circuit design - Sub-1V Bandgap Voltage Reference

The Bandgap Voltage Reference topology implemented is a modified conventional opamp based on the β-multiplier BGR circuit in order to achieve the sub-1 V output voltage desired. This topology is based on the principle of the one proposed in [6], which in itself is an adaption of [7]. As previously said, the target value for the reference voltage is 900 mV, for temperatures between -40 °C and 125 °C, with a VDD voltage of 1.8 V.

As discussed in section 2.3.1, there are multiple methods to lower the reference voltage of a BGR circuit, Figure 3 shows a particular one. Taking the disadvantages into consideration, it was decided to apply the resistive division method, resulting in the represented circuit. Instead of stacking two thermal complementary voltages, this bandgap voltage reference circuit is a current sum circuit that generates a near-zero TC voltage by converting a temperature independent current into a reference voltage through a resistor.

The operation of this circuit is similar to that of the conventional opamp based β-multiplier bandgap voltage reference circuit, where the operational amplifier forms an inverted feedback loop to ensure its two input nodes have the same voltage.

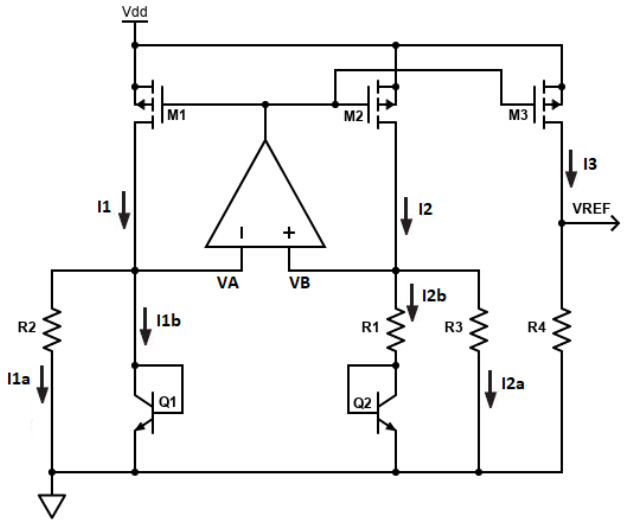

Figure 3: Bandgap voltage reference - topology.

Consider $R_2 = R_3$ such that $I_1 = I_2$, $I_{1a} = I_{2a}$ and $I_{1b} = I_{2b}$.

$$I_{2a} = \frac{V_A}{R_3} = \frac{V_B}{R_3} = \frac{V_{BE1}}{R_3}, \tag{5}$$

$$I_{2b} = \frac{V_B - V_{BE2}}{R_1} = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{\Delta V_{BE1,2}}{R_1} \tag{6}$$

The current $I_2 = I_{2a} + I_{2b}$, and $\Delta V_{BE1,2}$ is the difference in the base-emitter voltages of the two TBJs Q_1 and Q_2. This difference has the following expression.

$$\Delta V_{BE1,2} = V_{BE1} - V_{BE2} = V_T ln(N) \tag{7}$$

With N being the emitter area ratio between Q_1 and Q_2. The output voltage of the bandgap voltage reference circuit is given by

$$\begin{aligned} V_{REF} &= I_3 R_4 \\ &= I_2 R_4 \\ &= (I_{2a} + I_{2b}) R_4 \\ &= \left(\frac{V_{BE1}}{R_3} + \frac{\Delta V_{BE1,2}}{R_1} \right) R_4 \\ &= \frac{R_4}{R_3} \left(V_{BE1} + \frac{R_3}{R_1} V_T ln(N) \right) \end{aligned} \tag{8}$$

Comparing Equations 8 and 3, it is possible to conclude that this circuit is a first-order compensated bandgap voltage reference circuit, where the weighting factor

$$M = \frac{R_3}{R_1} ln(N). \tag{9}$$

IV. Circuit design - Voltage to current converter

As discussed in the section 2.4, after the examination of the results obtained for the isolated current reference circuits, it was decided to generate the current by utilizing the BGR circuit designed. The general approach to build a micro-ampere current reference is based on two different structures, shown in Figures 4 and 5 [8] [9].

The first one is a circuit where the reference current is the combination of a PTAT current, coming from the BGR core, and a CTAT current created by V_{BE}, however, since these two compensated currents come from different sources, the result would suffer from process variation.

The other topology makes use of the BGR reference voltage established, using an amplifier as a buffer of V_{REF} and an additional resistor to convert that voltage into a current, as shown in Figure 5 [10]. Feedback is used to generate the PMOS gate voltage that tries to produce a voltage drop of precisely V_{REF} across the resistor. In order to generate a stable reference current, a resistor with zero TC is preferable. However, since a zero TC resistor in CMOS process is not easily fabricated, as the doping concentration is hard to control, an off-chip resistor is usually the adopted solution.

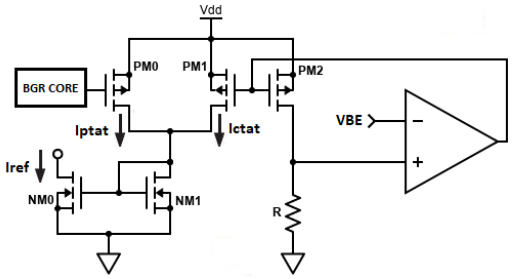

Figure 4: Combination of CTAT and PTAT current.

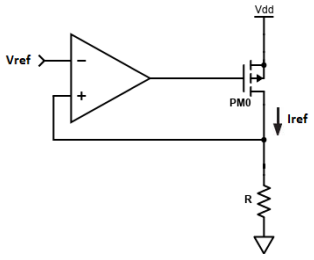

Figure 5: Voltage to current converter circuit.

In this work, the approach chosen is the latter, represented in Figure 5. As previously mentioned, an off-chip resistor is usually the solution, however, in the technology used there are multiple resistors with low temperature coefficients. It was decided to use the resistor type already used in the BGR circuit, since it is the one with the lowest TC.

In order to check the affect of the temperature on the on-chip resistor, the voltage across R is measured, while an ideal current of 1 mA is flowing through it. The total voltage variation obtained is V_{MAX} - V_{MIN} = 1.541 - 1.508 = 0.033 V, which is 2.17% of the voltage at the nominal temperature (1.52 V). The temperature coefficient is TC = 131.57 ppm/°C.

Considering this, the proposed circuit will provide both options to choose from, one where an off-chip resistor is used to calculate the current and another where it is calculated using the on-chip resistor [11]. As shown in Figure **??**, a path is created, starting in a point where the voltage is V_{REF} and ending in a pin (Trim_up), where a pad will be externally connected. Connecting to that pad will be the external resistor, if that is the option taken by the user.

Additionally, a transistor NMOS will act as a switch, controlled by the voltage at its gate, placed after the resistor, to avoid higher parasitic elements. When the voltage at the gate (ExtR) is 0, the transistor will cut and act as an open circuit, meaning the off-chip resistor will be used to generate the current. On the other hand, when the gate voltage has a high enough value, the transistor will act as a diode, connecting the on-chip resistor to GND and generating the desired current I_{REF}.

In order to reach a better variation of the current in the corners simulation, the trimming of the resistor is performed, which permits a precise adjustment of the resistance value to reach the desired value of current, in each process corner [10]. This technique consists in separating the original resistor into two parts, where one part has a fixed resistance value and another has a resistance value that will vary accordingly.

The maximum value of the current reached is approximately 1.17 uA, thus the minimum resistance value is 769 kΩ. On the other hand, the minimum value of the current reached is approximately 0.85 uA, thus the maximum resistance value is 1058 kΩ, which represents a resistance value variation of 1058 - 769 = 289 kΩ. Usually, in the trimming process, a safety margin is implemented, so, it is decided to amplify the variation obtained to 465 kΩ. This augmentation will result in a new minimum resistance value of 675 kΩ, which will be the fixed value of the resistor, and a new maximum resistance value of 675 + 465 = 1140 kΩ.

In summary, the resistor R will be formed by a fixed resistance value, 675 kΩ, and the remaining part will be

adjusted, 465 kΩ. The adjustment is done by dividing the resistance value 465 kΩ into five independently controlled resistors, represented as R_0 through R_4 in Figure 6. Each one of these resistors will be controlled through a switch, implemented with a NMOS transistor, where they will be ON (triode region) or OFF (cut off region), depending on the transistor gate voltage. The trimming result is a digital word of 5 bits, for each process corner, noting that the resistance values chosen for each resistor allow the digital word for the nominal corner to be 10000. The circuit implemented, now with the resistor R trimmed, is represented in Figure 6.

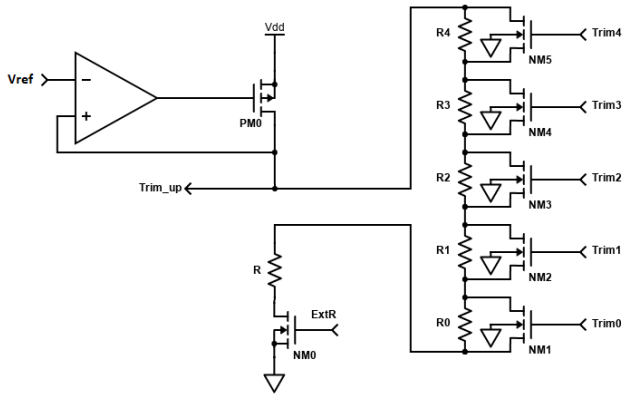

Figure 6: Voltage to current converter circuit with trimmed resistor.

Everyone of the NMOS transistors, acting as a switch, have to have a large width because the current flowing through the resistor should be negligible when compared with the one flowing through it. In order to replicate a short circuit as best as possible in the ON mode, the ratio W/L has to be extremely high.

V. Sub-1V Bandgap Voltage Reference Circuit Simulations

In this section, the performance measures of the BGR circuit are calculated through various simulations. The measures presented in this section make reference to the performance measures of a bandgap circuit, as such, these results allow to characterize and compare this voltage reference circuit with other similar circuits. The following sections will present the process corners simulation for each one of the measures, including the typical corner simulation.

A. Line Regulation

The line regulation is the variation of the reference voltage in respect to the variation of the power supply voltage. So, this measure value can be obtained by performing a DC analysis, with a sweep in the dc value parameter of the supply source. A first simulation between 1.5 and 3 V would allow to specify the interval for this measurement. Upon examination, it was decided to use an interval between 1.7 and 2.4 V to reach better results. The new simulation result is represented in Figure 7, including the 16 corners and the typical corner (red).

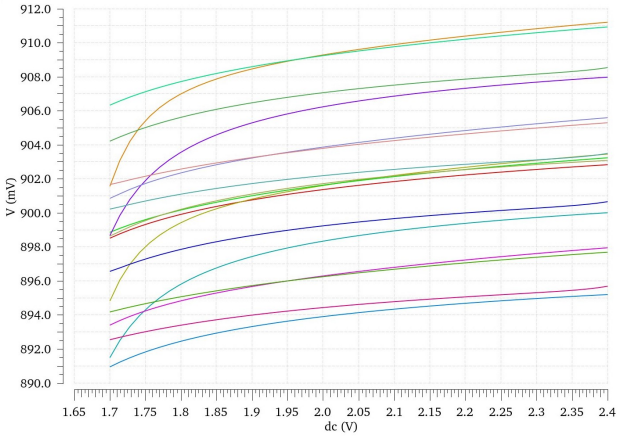

Figure 7: LR - process corners.

B. Temperature Coefficient

The next performance measure to be calculated is the temperature sensitivity of the circuit, also known as TC. This measure value can be obtained by performing a DC analysis as well, but with a sweep in temperature between -40 °C and 125 °C. The simulation result for the process corners is represented in Figure 8, including the 16 corners and the typical corner (red).

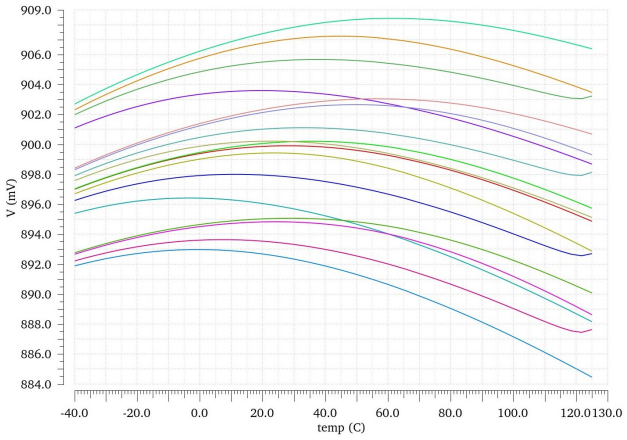

Figure 8: TC - process corners.

It is obtained the expected result for a reference voltage in a BGR, e.g., the value of V_{REF} is equal to 900 mV at T = 27 °C (nominal temperature). Additionally, as discussed

in section 2.3, the voltage obtained is near zero TC, since $\frac{\partial V_{REF}(T)}{\partial T} = 0$ at temperature T = T_{nom}.

Inspecting the result, it is possible to see that all the corners display, more or less, the same curvature. Furthermore, the largest voltage variation takes place in the higher temperatures.

C. Power Supply Rejection Ratio

The PSRR is defined as the ability of the output voltage to reject the noise and other signals at specific frequencies on the power supply. This measure value can be obtained through an AC analysis. Where, after inducing a disturbance in the power supply source, the output of the circuit (V_{REF}) is examined in frequency. The result, for a 1 V disturbance in the power supply source, is represented in Figure 9, including the 16 corners and the typical corner (red).

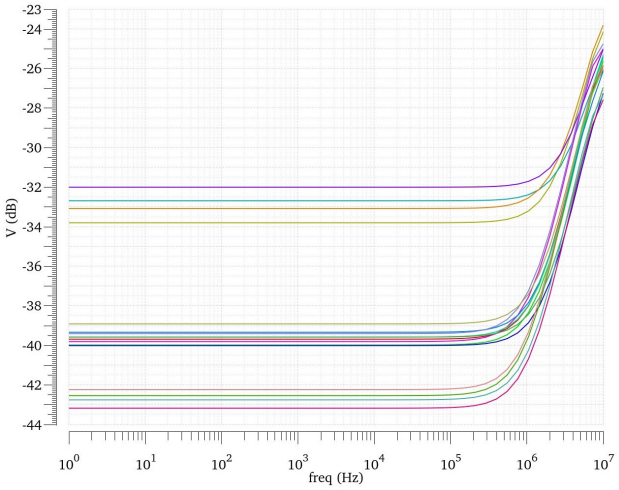

Figure 9: PSRR - process corners.

D. Startup Time

The function of the startup circuit is, as the name suggests, to start the circuit and bring it to its normal operating point. In order to check if the startup is fulfilling its purpose, transient analyses are performed for various temperature values. It was decided to perform a transient analysis for the minimum, nominal and maximum temperatures of the range worked on. After inspecting the corners simulation results, for the three different temperatures, it was possible to conclude that the startup circuit is performing its objective successfully in all cases. Additionally, the overall startup time obtained is around 325 ns, meaning the trimming vpulse sources delay time can not be lower than that.

VI. Voltage to Current Converter Circuit Simulations

A. With Off-chip Resistor

This section presents the results for the circuit using one of the options provided, the off-chip resistor. In order to perform the simulations, an analogLib's ideal resistor was used to reproduce the same effect as the external resistor. The pin ExtR will now connect to GND and the ideal resistor, with a value of 900 kΩ, will be connected to the pin Trim_up.

The result of the DC analysis with a sweep in temperature between -40 °C and 125 °C, including the 16 corners and the typical corner, is represented in Figure 10.

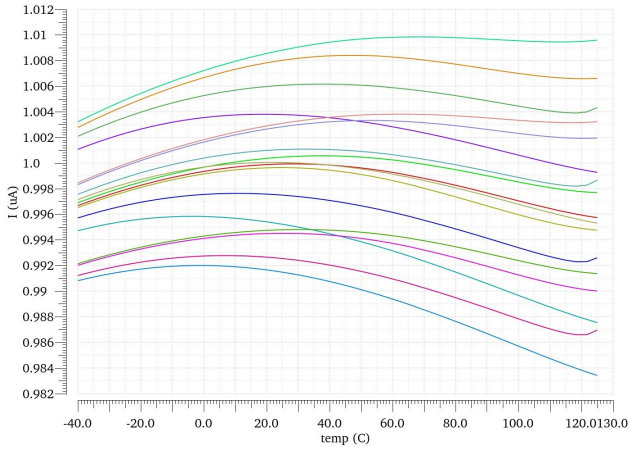

Figure 10: Current variation in temperature - process corners.

The obtained results display a total current variation of ΔI = 1.009 - 0.983 = 0.026 μA, which is equivalent to 2.6 %. Given the fact that the resistor used is ideal, it is safe to assume that most of the current variation obtained is due to the discrepancy in the reference voltage coming from the BGR circuit designed.

B. With Trimmed On-chip Resistor

In this section, it is presented the result of various simulations of the voltage to current converter circuit, using the alternative, an on-chip resistor. These results show the least possible variation in temperature suffered when using the on-chip resistor. For that, it is performed a transient analysis, where the current in the output I_{REF} is tested for all the 32 possible combinations from the five bits of the trimming circuit. All the results are listed in Table I.

The obtained results display a total current variation of ΔI = I_{MAX} - I_{MIN} = 1.015 - 0.983 = 0.032 μA, which is equivalent to 3.2 %. Recalling the TC of the

technology resistor used and the overall variation of V_{REF} in temperature, these results are positive and are within the values expected.

The results registered using the off-chip resistor are very similar to the ones presented before, with the trimmed off-chip resistor. Taking that into account, it is possible to conclude that the trimming was well done and the variation registered is mostly due to the discrepancy in the reference voltage coming from the BGR circuit designed, where only 0.6 % is originated from the use of the on-chip resistor.

Corner	Word	T = -40 °C	T = 27 °C	T = 125 °C	Unit
typical	10000	0.987	1.000	0.998	μA
corner0	00111	0.991	0.998	0.991	μA
corner1	00111	0.991	1.000	0.995	μA
corner2	00111	0.989	0.994	0.985	μA
corner3	00111	0.990	0.997	0.990	μA
corner4	11000	0.986	1.001	1.009	μA
corner5	11000	0.985	1.005	1.009	μA
corner6	11000	0.985	1.002	1.000	μA
corner7	11000	0.983	1.001	1.005	μA
corner8	00111	0.996	1.007	1.004	μA
corner9	00111	0.997	1.008	1.007	μA
corner10	00111	0.995	1.003	0.996	μA
corner11	00111	0.005	1.003	1.003	μA
corner12	11000	0.992	1.010	1.010	μA
corner13	11000	0.991	1.013	1.015	μA
corner14	11000	0.989	1.009	1.004	μA
corner15	11000	0.987	1.008	1.009	μA

Table I: Corners simulation results.

VII. Layout design

This layout was hierarchically designed, e.g., it started with the design of the smaller individual blocks (opamp, startup, amp, resistors, etc), after that, they were connected with each other and with the rest of the circuit. All the layouts designed, and presented, respect the DRC rules and are compatible with the respective schematics, according to the LVS.

Throughout the design of the layout, any space left between the components will be filled with decoupling capacitors (DECAPs) [12]. Among power supply noise reduction techniques, inserting DECAPs is the most common practice. These capacitors hold a reservoir of charge, and are requested if a high current is being demanded. The DECAPs are made from NMOS transistors because they are the prime choice when area is a concern, whereas the PMOS transistors are used in low leakage applications.

Furthermore, if the transistors are NMOS, meaning the body is connected to GND, the guard ring surrounding them will be as well. In the case of PMOS transistors, the guard ring will be connected to VDD [13]. The main function of these guard rings is to polarize the transistors bodies, but will also help reduce subtract noise inside the system.

The system layout is represented in Figure 11. As it is possible to see, the disposition follows the floor plan proposed. The layout area obtained is 0.058 mm^2, where the length L = 258 μm and the width W = 224 μm, preserving a ratio close to 1, as desired.

Furthermore, it is visible the presence of decoupling capacitors made from NMOS transistors. These DECAPs are filling all the space left between the blocks, and for that reason, each one has its set of dimensions. Each one of these capacitors is surrounded by a guard ring connected to GND, since they are made from NMOS transistors.

Every single block in the layout is surrounded by a guard ring, either connected to GND or VDD. A precaution taken was to connect all guard rings of adjacent blocks, if both connected to GND/VDD.

Additionally, around the system layout there will be two guard rings, one outer ring for VDD and one inner ring for GND. These rings are double the width of the ones used in the sub-circuits, and are now formed with two rows of contacts instead of one, to achieve better performance. These guard rings will isolate the system noise, by stopping it to propagate to neighbours systems, as well as ease the connection to VDD and GND inside the circuit.

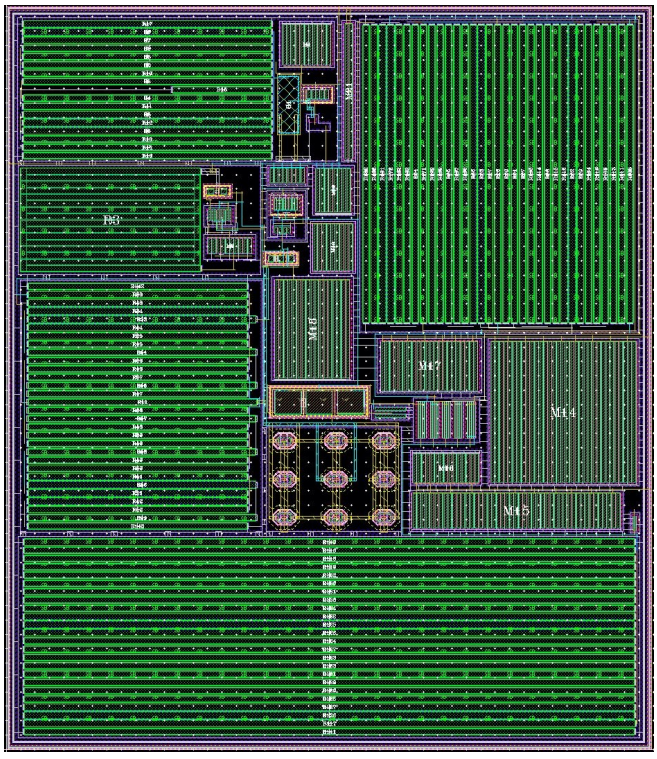

Figure 11: System - layout.

VIII. Post-layout results

In this section, the post-layout results of the system are calculated through similar simulations and using the same testbench, however, they are achieved utilizing the layout extraction.

Before extracting the layout, it is performed the DRC and LVS, both part of Calibre. The DRC checks if there are any design rules that are being broken, e.g., minimum space between metals, between components, etc. The LVS, or Layout vs schematic, checks if the layout designed is connected and placed accordingly when compared to the source, the schematic. The DRC result obtained is a blank screen, meaning there are no warning or errors in the layout designed, and the LVS result does not indicate any errors, meaning, the layout is ready to be extracted.

The extraction of the layout is done through PEX, also part of Calibre. This tool will extract the netlist from the layout, however, it includes parasitic resistances and capacitances. The extracted layout is then simulated similarly to the schematic, and the results of all the simulations performed are listed in Table II.

Apart from the performance measures displayed, the startup circuit was also analysed in this new environment. Through multiple transient analyses, it was concluded that the behaviour was similar to the one seen using the schematic of the circuit, e.g., it started the circuit and brought it into its normal operating point in all 32 process corners, for the three different temperatures. Lastly, it was calculated the system current consumption, because, even though it was not a concern, it is important to get represent its value. The current consumption obtained for the system is 137.1 μA.

As a way of getting a deeper understanding of the BGR obtained results, the Table II is comparing the post-layout results with various other works published. The other works selected for this comparison are all from the past ten years, and more importantly, have similar supply voltages, temperature ranges and reference voltages.

The first parameter is the current measured at the power supply voltage, also known as current consumption. The higher current consumption when compared to the other works listed can be justified by the fact that this parameter was not a main concern when designing the system and it was not even defined a target value, also worth noting that the consumption value measured refers to the BGR, not including the converter circuit, so the comparison is done on equal terms.

The TC average value simulated is roughly the same as in the others publications, with the exception of reference [14]. That work presents a temperature curvature compensation method, which will lower the voltage dip for higher temperatures, resulting in a lower total voltage variation and consequently a lower TC value. The reference [15] also presents a low TC value for the exact same reason, but applying a different compensation method, this time resulting in a "M" shaped graph of the reference voltage in temperature.

The same occurs when looking at the PSRR parameter, where one case stands out the most, reference [16], because that work was specifically designed to achieve a very high PSRR value. As for the area occupied, the higher value is mainly due to the trimming performed to the resistor in the voltage to current converter circuit.

Specification	This work	[17]	[15]	[16]	[14]
Supp. volt. (V)	1.8	1.2	1.6	2.3	1.5
Current (μA)	66.89	50.4	17	40	1.1
Tm. range (°C)	-40–125	0–100	-65–140	-40–120	-40–100
Ref. vol. (V)	0.898	0.72	1.202	0.8	0.6
Avg. TC (ppm/°C)	35	53.1	9.9	54	4.4
Best TC (ppm/°C)	20.8	43.5	–	–	4.4
PSRR @10Hz (dB)	-45.7	-51	-57.7	-120	-100
CMOS proc. (nm)	180	90	250	350	130
Area (mm^2)	0.058	0.028	–	0.024	0.04

Table II: Comparison with other BGR circuit publications.

IX. Conclusion

This master thesis has explored the process involved in the design of both a sub-1V bandgap voltage reference circuit and a voltage to current converter circuit, all in one system. This system had to accomplish the specifications imposed, and deliver acceptable results in the rest of the performance measures. This last chapter includes the final conclusion regarding the work done, the results obtained and a discussion about the future work that can still be done in the system designed.

A. Results Analysis

The system was designed in a 180 nm conventional CMOS process technology. In the case of the BGR circuit, simulated results have shown temperature coefficients as low as 20.8 ppm/°C over a temperature range of 165 °C (-40 °C to 125 °C). Additionally, the circuit displays a PSRR of -45.7 dB at low frequencies and -39 dB at 1 MHz. The converter circuit presents a process corners current variation of 3.2 %, for the same temperature interval. The system current consumption is 137.1 μA. Taking that into account, it is possible to say that all the objectives established at the beginning of this project were accomplished and the results attained are considered satisfactory. An overview of the stages completed during this project is listed below.

- Study of the state of the art for similar circuits.
- Selection of the topologies to implement.
- Creation of the schematics using the technology proposed (CMOS 180 nm).

- Assembly of the testbenches and simulations to be performed.
- Analysis of the pre-layout results.
- Layout design.
- Layout validation through DRC and LVS.
- Analysis of the post-layout results and comparison with the pre-layout ones.

Every sub-circuit implemented in this project was sized to correctly operate in collaboration with the other blocks to obtain the final result, the voltage and current references. This thesis work allowed to learn how to perform a complete analog integrated circuits design flow.

B. Future Work

Considering the specifications of this work satisfactory, the next step is performing a Monte Carlo simulations and, in case the results are acceptable, proceed to the manufacturing process, e.g., the fabrication of the chip designed. After the chip fabrication, it is proposed to re-evaluate the system performance parameters and compare them with the values measured at the layout level. Allowing a good insight of the real differences between the simulator level and the fabricated chip.

However, even if the results meet the desired values, there are still improvements that can be done to the system implemented. The decisions taken to not implement those techniques were based on the performance, complexity, available time and a possible inexperience in the field.

One of the critical blocks of the BGR circuit is the operational amplifier, designed to force the voltages at the inputs to be equal. The improvement that could be done is, as previously discussed, replace the resistor with a PMOS transistor, by applying the bootstrap technique. It is believed that, if applied correctly, this technique would improve the PSRR of the opamp, which is its weakest specification. Additionally, it would decrease the size of the block and the system, since the resistor to be replaced is the largest component of the opamp. Another improvement that could be implemented is the use of a cascode configuration instead of basic current mirrors in the BGR circuit, ensuring a better mirroring of the current, probably resulting in a lower TC value of the reference voltage, and consequently the current. Furthermore, even if not a main concern, the current consumption of the BGR circuit is slightly above average. One way to improve this specification is by utilizing resistors with higher resistance values, although this would result in a higher chip area, which was already substantial.

One last possible modification is related with the amplifier used in the voltage to current converter. The amplifier used could be replaced by an operational amplifier, similar to the one used in the BGR circuit. This would result in a more reliable amplifier less affected by its transistors impairments. This would be observed in a Monte Carlo simulation. However, this change would result in a slightly higher chip area, as the resistor occupies the largest space in the circuit.

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