Low-power clock generator system for wireless sensors networks

Sara Santos
Instituto Superior Tcnico
Lisbon, Portugal
sara.b.dos.santos@tecnico.ulisboa.pt

***Abstract*—Extending the battery life of devices is an objective transversal to any area of electronics. Especially when working with Wireless Sensors Networks (WSNs), usually installed in remote locations, the sensors battery life gains greater importance.**

To achieve the goal of prolonging the time a battery is powering the circuit, WSN systems often rely on duty-cycle schemes of operation: the system is periodically and briefly powered-up to receive/transmit data, being in sleep mode most of the time. Despite that technique, the block responsible for keeping track of when the communication time slots must happen waking-up other blocks from the sleep mode - the wake-up timer - must be always operating. Thus, it is of extreme importance, and also a big challenge, to implement a wake-up timer with minimum power consumption. With the reduction of power consumption comes a lower frequency stability. The solution is to design a reference frequency oscillator to operate as the system clock which is only active during communication time slots and that is used to calibrate the wake-up oscillator.

In this work a crystal oscillator is proposed as the system clock for its high frequency stability. The wake-up timer is an Ultra-Low Power (ULP) oscillator, implemented as a RC oscillator (RCO) with digital calibration of the frequency through corrections in the bias current. A Frequency-Locked Loop (FLL) is implemented to synchronize the oscillators.

***Index Terms*—Clock generator system, Crystal oscillator, Ultra-low power oscillator, Calibration, Frequency-locked loop**

I. Introduction

Wireless Sensors Network (WSN) systems are used in multiple short-range low data-rate applications. A desirable property of the battery powered sensor nodes is to have a long energy autonomy, which is only attainable if Ultra-Low Power (ULP) circuits and systems are wisely used. In a clock generator system, which is always operating, the low power is guaranteed by using an intermittent power on scheme. An ULP oscillator - operating as a wake-up timer - keeps track of time and synchronizes with the system reference clock during sensor data communication time periods. Outside these time periods all system blocks, except the wake-up timer, are powered off. WSNs for Internet of Things (IoT) applications obey communication standards that take into account the need for short-time communications slots and long periods in idle state to reduce power consumption.

Crystal oscillators (XOs) are widely used as the reference oscillator for it high frequency stability. From simpler solutions as a basic Pierce topology [1] to more elaborated ones [2], [3], where the oscillator power consumption is reduced. Several techniques to accelerate the XO start-up are presented in the literature [4]–[7], either by injecting a signal at the XO resonance frequency or by increasing its negative resistance. The XO presented in this work is Pierce-based and it is designed to allow the addition of quick start techniques in a next version.

ULP oscillators, either with or without a resonator, are used as wake-up oscillators, however the resonator-less topology is more frequently used due to its smaller area and cost when compared with other types. In literature, [8] and [9] present solutions based on a charge-pump, using voltage comparators to control the output voltage. Work [10] implements a current comparator with latch to substitute the voltage comparator used in previous works, decreasing even further its power consumption. ULP oscillators disadvantage is a low frequency stability, therefore, to improve it several works introduce digital calibration [9]–[11].

From Phase-Locked Loop (PLL) synchronization circuits [12], using a Phase-Frequency Detector (PFD) to produce an error signal proportional to the phase difference between reference and ULP oscillators, to topologies which use two different mechanisms for faster results [9], [13]. The two oscillators output signals are compared and the difference between them corresponds to the frequency error. This error is converted into a digital word or control voltage which calibrates the ULP oscillator, implemented as a Digitally-Controlled Oscillator (DCO) or a Voltage-Controlled Oscillator (VCO), respectively.

II. Oscillator theory

An oscillator produces a periodic signal, transforming DC signals into AC signals. Depending on whether or not the oscillator output is sinusoidal, the oscillators are characterized into two groups: linear or harmonic oscillators and nonlinear or relaxation oscillators, respectively. A crystal oscillator is used as an example of an harmonic oscillator and a charge-pump oscillator, an ULP topology, illustrates a relaxation oscillator operation.

A. Crystal oscillator

An harmonic oscillator can be seen as a resonator working with an active circuit which compensated the resonator losses. The XO uses a quartz crystal resonator to provide the oscillation frequency, which is an off-chip component, it can not be

integrated in the chip. Therefore, one or two pads are needed to connect it to the circuit. The crystal resonator at fundamental frequency can be approximated by the Butterworth Van Dyke (BVD) model. Figure 1 represents the equivalent circuit of a crystal resonator based on the BVD model.

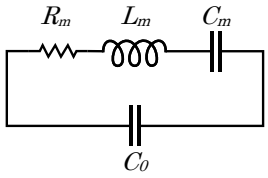

Fig. 1: Representation of Butterworth Van Dyke model of a crystal resonator for the fundamental mode.

The series of L_m, C_m and R_m, called motional arm, represent the mechanical behavior of the resonator. The inductance L_m is related to the mass of the resonator, capacitance C_m is a function of its stiffness and resistance R_m represents the losses of the crystal and mounting. The shunt capacitor C_0 is the capacitance between the metalized electrodes of the crystal and includes the package and stray capacitances due to mounting structure.

According to the model represented in 1 the crystal has two resonant frequencies: the series and parallel resonant frequencies, f_s and f_p, respectively. At the crystal series resonant frequency, f_s, L_m and C_m are in resonance and cancel each other out, meaning the crystal circuit is equivalent to the parallel of R_m and C_0. At the parallel resonant frequency, f_p, the series of L_m and C_m is inductive, resonating with the parallel capacitor C_0.

Figure 2 illustrates the reactance of crystal, modeled by the BVD model, in a tight frequency range around the oscillation frequency. Both resonant frequencies are represented in Figure 2.

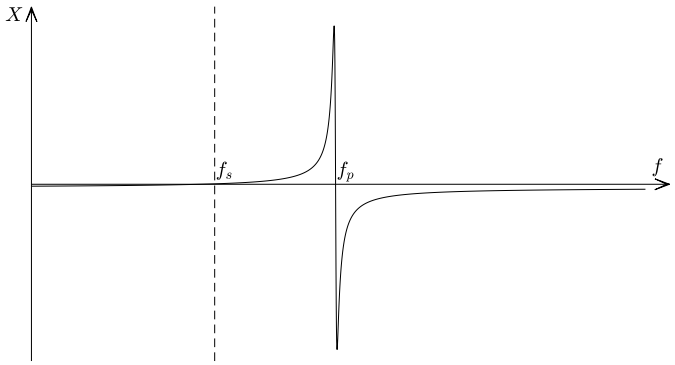

Fig. 2: Representation of the crystal resonator reactance for a 32 MHz crystal.

Between f_s and f_p, in the crystal inductive region, its reactance evolves faster than when compared to a simple inductor, which implies the crystal has a high quality factor, Q, in the order of 10^5 [14]. A high Q, necessary for a better frequency stability, means a slow oscillation start-up, thus its start-up time is an important aspect to study since it's largely responsible for its high power consumption.

The crystal is used in a Pierce oscillator topology, as represented in Figure 3, working in the inductive region.

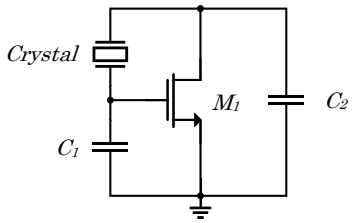

Fig. 3: Representation of the crystal Pierce oscillator small-signal schematic.

In the Pierce oscillator mentioned in Figure 3 a small perturbation in the circuit is enough to start the oscillation assuming it is dimensioned to be unstable for small signals. The perturbation can be, for example, caused by noise or the circuit power-up transient.

Considering the oscillator as a gain block and a feedback network, the Barkhausen criterion states that for a circuit to be an oscillator it must present for the loop a unitary gain and a phase shift equal to 0° or an integer multiple of 360°. This is the steady-state oscillation condition. To guarantee that the oscillations start the loop gain must be higher than one and the phase must be close to zero. This corresponds to having one pair of conjugated poles at the right-half complex plane.

With the gain higher than unity the oscillations amplitude grow, therefore a nonlinear circuit is needed to limit that amplitude. When the amplitude reaches the desired value, the loop gain equals the unity due to the nonlinear circuit, forcing the poles to the imaginary axis. At this moment the oscillator enters the steady-state regime.

To do a more profound analysis of the crystal oscillator the one-port impedance method is used [15]. The crystal oscillator can be divided into two blocks: linear and nonlinear behavior circuits, Z_m and Z_c, respectively. The shunt capacitor C_0 can be included in the nonlinear block, along with the transistor and load capacitors, C_1 and C_2. The motional arm of the crystal forms the linear block.

Considering C_m and L_m, capacitor and inductor of the resonator motional arm, as ideal elements the resonator impedance, Z_m, real part is equal R_m and its imaginary part corresponds to

$$Im\{Z_m\} = X_m = j\omega L_m - \frac{j}{\omega C_m}. \tag{1}$$

The circuit impedance, Z_c, can be also be divided into real and imaginary parts, R_c and X_c. The oscillator start-up conditions are

$$\begin{cases} R_c + R_m < 0 \\ X_c + X_m \approx 0. \end{cases} \tag{2}$$

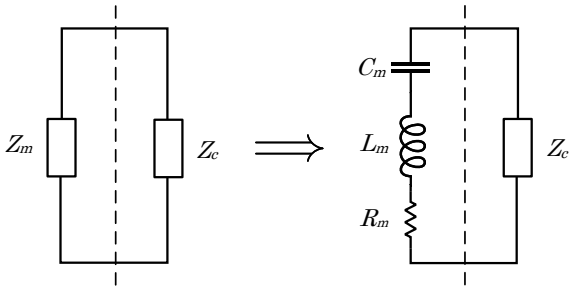

Fig. 4: Representation of the linear and nonlinear blocks of a split crystal oscillator.

Analyzing the oscillator start-up for the critical case, where the start-up condition is calculated for small signals,

$$Z_c + Z_m = 0. \tag{3}$$

With this equality the optimum point for minimum start-up time is obtained in function of the parameter g_m, transconductance of the nonlinear block active device, as

$$g_{mopt} = \frac{\omega(C_0C_1 + C_1C_2 + C_0C_2)}{C_0}. \tag{4}$$

Minimum start-up energy can be obtained from

$$E_{startup} = \int_0^{t_{startup}} v_{dd}(t) i_{dd}(t) dt, \tag{5}$$

and knowing that i_{dd} is related to transistor drain current i_{ds} (and therefore with the transistor g_m) the minimum start-up energy occurs for the minimum transconductance which guarantees the oscillation, $g_{m_{min}}$.

B. Ultra-low power oscillator

With fast start-up time and low power consumption, at expenses of the frequency stability, relaxation oscillators are good solutions to use as wake-up timers. A relaxation oscillator is characterized by the charging and discharging of one energy-storing element, which can either be a capacitor or an inductor. The charging and discharging time of the component translates into the circuit time constant which defined the oscillation frequency. Most common relaxation oscillators are ring and charge-pump oscillators.

In a charge-pump oscillator, comparators are used to verify if the capacitor voltage is between determined thresholds, adjusting the oscillator output accordingly. The capacitor charge and discharge stage is controlled by the output signal which is feedback to the capacitor switch. The simplified schematic of a charge-pump oscillator is presented in Figure 5.

The circuit includes two comparators to decide if the capacitor voltage is between the defined reference voltages. The capacitor is charge or discharge by one of the current sources, depending on the Set-Reset (SR) latch output. Comparator 1 output is high if the capacitor voltage goes below the reference level V_{min}, resetting the SR latch. When the capacitor voltage becomes larger than V_{max} comparator 2 sets the circuit output

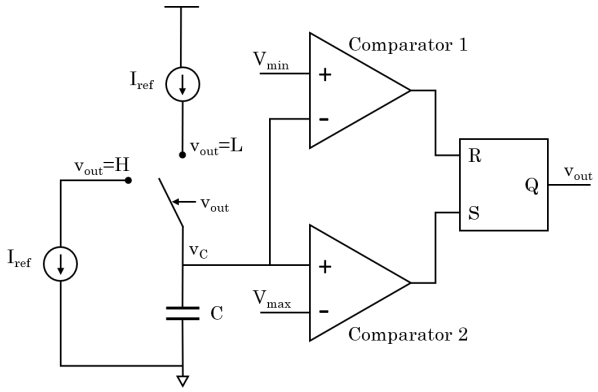

Fig. 5: Simplified schematic of comparator-based relaxation oscillator.

to high. The SR latch output, Q, controls the capacitor switch so the capacitor is charged when the output is low and discharged when it is high.

The oscillator output is a square wave generated by the SR latch which frequency,

$$f = \frac{I_{ref}}{2C\Delta V_c}, \tag{6}$$

depends on the reference current, I_{ref}, the capacitor value, C, and the capacitor voltage variation, ΔV_c.

III. Clock generator system

To achieve a solution with the lowest possible power consumption, a system is designed where the reference oscillator is turn on only during data communication time slots, short periods of time when the frequency stability is of extreme importance. Outside these time slots, the reference oscillator is powered off and an ULP relaxation oscillator is used to keep track of time. This oscillator has a significantly lower frequency stability when compared to the reference oscillator, however is enough to know when it's time for the next data communication and turn on the reference oscillator. To improve the ULP oscillator frequency stability a synchronization with the reference oscillator is made every time the latter is powered on.

A clock generator system, composed by a reference frequency oscillator, a RC Oscillator (RCO) and the calibration circuitry, is implemented in UMC130 technology, from United Microelectronics Corporation, and simulated using Cadence software. The individual circuits are then connected together as illustrated in Figure 6, where x_1 and x_2 represent the crystal resonator connections, and the clock generator system is simulated.

A XO is chosen to generate the frequency reference due to its high frequency stability and, due to its high quality factor, it can maintain the oscillation spending less energy than other references. The XO has the disadvantage of using an external resonator, which implies the use of two additional pads. The XO frequency is selected as 32 MHz, a standard frequency for

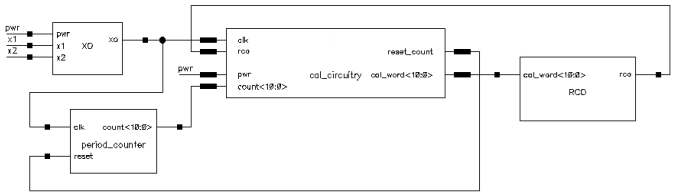

Fig. 6: Detailed clock generator system block diagram.

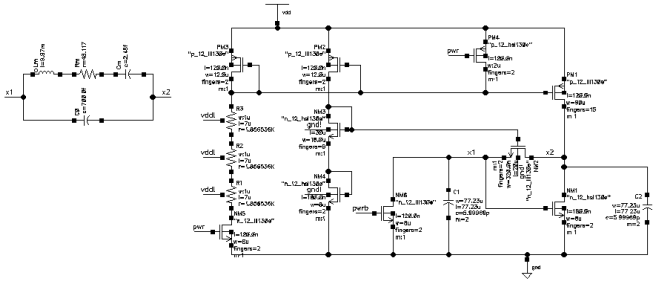

Fig. 7: Single-MOS crystal oscillator schematic with power-down.

this type of oscillators and also imposed by the sensor node receiver demodulator.

The RCO frequency is selected as 31.25 kHz, a power of two multiple of the reference oscillator so the counter used in the synchronization can be a binary counter. The wake-up timer must allow digital calibration and output a square wave signal with minimum power consumption, therefore, the topology selected is a digitally-controlled RCO, which frequency can be tuned adjusting the current charging/discharging the capacitor through a digital word from the calibration logic block.

The calibration circuitry includes a period counter and the logic responsible for implementing the calibration algorithm. The period counter counts the number of periods of the crystal oscillator during one cycle of the RCO. Any value different from 1024 implies an error in the RCO frequency. This error is given to the calibration logic block where a algorithm decides the control word to calibrate the RCO with the minimum iterations possible. After the calibration, all blocks, except the RCO, are powered off.

With the power off only the RCO is operating. XO and buffer are power down, and without variations in the input the period counter and calibration logic outputs are stable, reducing significantly the power consumption. RCO is operating normally, keeping track to time to power up the system at the correct moment.

A. Crystal oscillator

A single N-type Metal Oxide Semiconductor (NMOS), biased by a current source, is used as the active device of the Pierce crystal oscillator represented in Figure 7. Power-down is added to allow the use of a duty-cycle scheme in order to save energy.

A feedback resistor inserted in parallel with the crystal generates the biasing voltage for the P-type Metal Oxide Semiconductor (PMOS). This resistor value is proportional to the loop gain, with an insufficient loop gain the crystal oscillator would have a long start-up time or would even fail to start the oscillations. Transistor NM2 implements the large value feedback resistor, operating in weak-inversion biased by transistors NM3 and NM4. The crystal resonator is connected at x_1 and x_2 terminals.

To power-down the oscillator, PM4 imposes zero voltage at V_{SG} of current mirror transistors and the bias resistor is disconnected. When the power-down signal, pwr, turns low the circuit enters into power-down mode, reducing the total current to 716 pA.

Several solutions are simulated and the one which presents a lower start-up energy is selected as the preferred solution. Figure 8 illustrates the crystal oscillator output voltage and frequency for this solution.

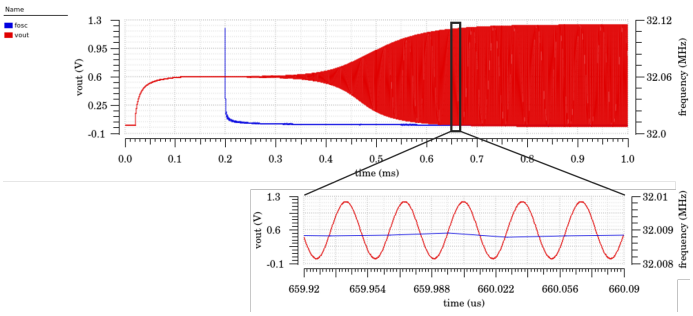

Fig. 8: Single-MOS crystal oscillator output voltage.

A voltage buffer, represented in Figure 9, is introduced at the XO output to obtain a square signal, so it can be used as a clock signal. The buffer is based on a conventional Complementary Metal Oxide Semiconductor (CMOS) Schmitt trigger with feedback to improve the output voltage transitions

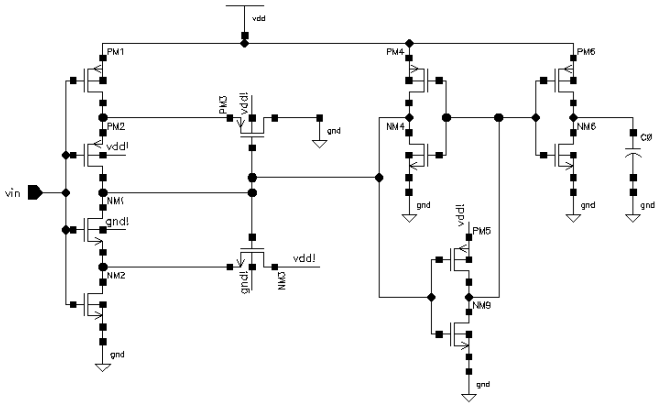

Fig. 9: Voltage buffer schematic.

The feedback loop is implemented with two back-to-back inverters, represented by transistors NM3, NM4, PM3 and

PM4. The buffer circuit is dimensioned for a 5 pF load capacitor. With the XO at the buffer input, its output is simulated and shown in Figure 10, along with the input signal. The sine wave corresponds to the crystal oscillator output - voltage buffer input - and the square wave depicts the buffer output signal.

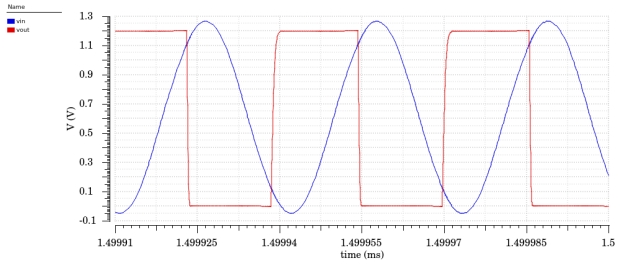

Fig. 10: Voltage buffer output voltage.

The buffer outputs a square wave signal with a duty-cycle of 49.9% and rise and fall times of 0.84 ns and 0.5 ns, respectively, for a 5 pF load, an exaggerated value to assure the correct operation of the circuit when introduced in the system. To allow for the comparison with state-of-the-art works a 500 fF load capacitor, a more realistic value, is used. For this capacitor a duty-cycle of 50.1% is obtained with rise and fall times of 0.10 ns and 0.06 ns, respectively.

The complete XO with the voltage buffer at its output is simulated for Process, Voltage Supply and Temperature (PVT) variations to understand how it performs under non-ideal conditions. The oscillator is simulated for a 10% variation of the supply voltage and temperature between -40 °C and 125 °C. The process variation covers all the on-chip components: transistors, capacitors and resistor. The output voltage response to these variations is simulated. The frequency deviation for temperature and supply voltage variation is represented in Figure 11.

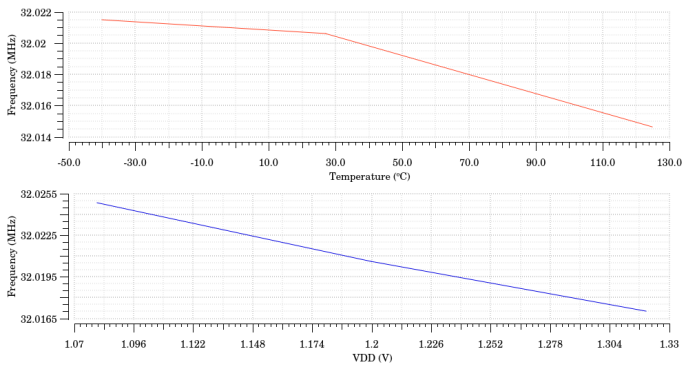

Fig. 11: XO frequency for temperature and voltage supply variation.

From the temperature variation the circuit registers a frequency deviation of -1.3 ppm/°C. For the voltage supply variation the frequency has a deviation of 7.85 kHz which translates to a -0.1 %/V deviation.

The output signal duty-cycle varies between 6.4 % and 62.5 %. This high variation represents a problem when using this signal as a clock signal and, therefore, it needs to be solved. One possible solution would be to use a duty-cycle corrector, a circuit which takes an input signal with a duty-cycle different form 50% and corrects it to that value.

Table I summarize important parameters obtained for the implemented crystal oscillator with buffer and its comparison with several works presented in literature and a XO from manufacturer Epson Seiko. Start-up time and energy are measured when the output signal amplitude reaches 90% of its final value.

TABLE I: Comparison of crystal oscillator with state-of-the-art works.

Reference	This work		[16]	[17]	[18]	[19]
CMOS process [nm]	130		180	65	90	NA
Frequency [MHz]	31.97		39.25	50	24	32
Supply voltage [V]	1.2		1.5	1.0	1.0	1.8
Start-up time [µs]	660	555 [a]	158	2.2	200	3000
Start-up energy [nJ]	640	621 [a]	350	10	40	NA
Steady-state power [µW]	899	1164 [a]	180	200	100	3960
Phase noise (@1 kHz) [dBc/Hz]	-116.3	-117.3 [a]	-147	NA	NA	NA
Quick start-up	no		yes	yes	yes	no

[a] including buffer and load capacitor of 500 fF

B. RC oscillator

The ULP oscillator topology chosen is a RC oscillator, a charge-pump based oscillator which frequency is defined by an RC circuit. Based on work [10] this oscillator uses current comparators to achieve more power-efficient results. The RCO schematic is represented in Figure 12.

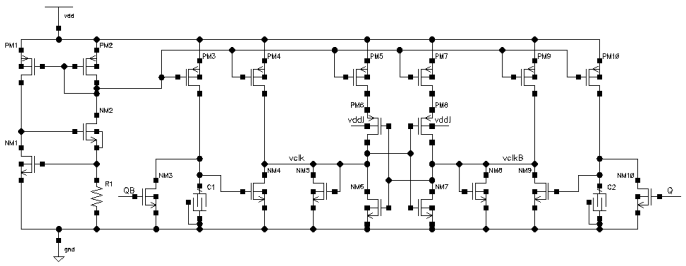

Fig. 12: RC oscillator schematic.

Capacitor voltage, v_{C1} (v_{C2}), is converted to current, i_{M4} (i_{M9}), by transistor NM4 (NM9). This current is then compared with the bias current, i_{R1} of resistor R1, in the current comparator, composed by NM4 (NM9) and NM5 (NM8). When i_{M4} reaches i_{R1} value, the latch, corresponding to transistors NM6, PM6, NM7 and PM8, toggle its outputs, v_{clk} and v_{clkB}. When one side of the latch rises the other automatically drops. Transistors NM5 and NM8 also operate as clamp transistors, limiting v_{clk} and v_{clkB} amplitude. By keeping these signals at low levels the impact of comparator

delay in the circuit frequency diminish. A digital logic block - not represented in Figure 12 - receives v_{clk} and v_{clkB} signals and outputs the complementary square signals Q and Q_B are applied to the gates of the transistors that act as switches (NM3 and NM10), controlling the charge and discharge of the capacitors. Signals Q and Q_B are the oscillator outputs. Figure 13 illustrates relevant voltages and current of the RCO.

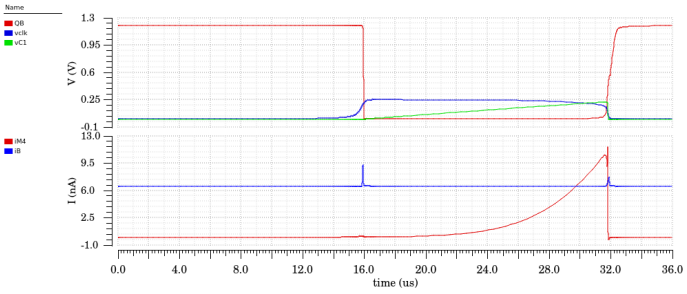

Fig. 13: Improved RC oscillator voltages and currents.

In Figure 13, i_{M4} exceeds i_{R1} before the capacitor is discharged, pulling i_{M4} to 0 A. This happens due to delays in the comparison, adding an error to the frequency and it is corrected during design by adjusting the capacitors value, pulling the nominal frequency to the desired value, 31.25 kHz.

In this RCO a self-biased current source, based on a threshold voltage reference current source, is implemented [20]. Instead of depending on the voltage supply, the PM1 current is directly dependent on the current source output current, PM2 drain current. By applying this technique to a threshold voltage reference the voltage supply sensitivity reduces significantly, however, due to the high negative temperature coefficient of the threshold voltage, this current source is temperature dependent.

Self-biased current sources have two stable points, being one the zero current point. A start-up circuit [21] is required to force the current source to operate in the stable non-zero point with I_{R1} current amplitude. Figure 14 shows the self-biased threshold voltage reference current source and respective start-up circuit.

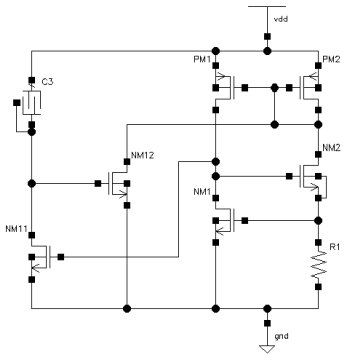

Fig. 14: Implemented current reference generator with start-up circuit.

At the initial instant capacitor C_3 is discharged and the voltage at its terminals is zero, putting the transistor NM12 gate at V_{DD}. Transistor NM12 starts conducting forcing its drain current to transistor PM2, which mirrors it to PM1. At this point PM1 and PM2 are in saturation region and v_{sd1} of PM1, which corresponds to NM11 gate voltage, starts rising, turning on NM11 which operates as a switch. When NM11 turns on forces a voltage close to zero to transistor NM12 gate. With no drain current, MN12 is disconnected from the circuit.

Regarding the current source, the voltage at NM2 terminal varies with the voltage supply variations, reducing the voltage variation at R_1 terminals, therefore decreasing the oscillation frequency dependence on V_{DD}. A triple-well NMOS is used to eliminate the body effect.

From the RCO circuit, the bias current is given as a function of NM1 gate voltage and resistor R_1,

$$i_{R1} = \frac{v_{gs1}}{R_1} \tag{7}$$

and the capacitor voltage, v_{C1}, can be expressed as

$$v_{C1} = v_{gs4} = \frac{i_{R1}}{2C \times f_{osc}}. \tag{8}$$

From (7) and (8) it follows that the oscillation frequency depends on R_1 and C_1 as

$$f_{osc} = \frac{i_{R1}}{2C \times v_{gs4}} = \frac{v_{gs1}}{2R_1C_1 \times v_{gs4}}, \tag{9}$$

showing that if NM1 and NM4 transistors have equal dimensions, gate voltages v_{gs1} and v_{gs4} cancel out and the oscillation frequency is only dependent on the resistor and the capacitor values. The process deviation consequences are diminished, since both transistors vary equally.

The RCO oscillation frequency deviation for temperature and voltage supply variations is represented in Figure 15. The oscillator is simulated for two situations: for temperatures between -40 °C and 80 °C at nominal supply voltage and with a 10 % variation of V_{DD} at nominal temperature, 27 °C.

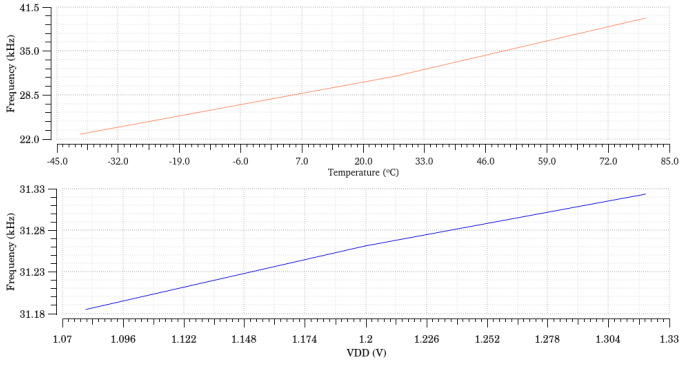

Fig. 15: RCO frequency for temperature and voltage supply variation.

For the temperature variation the RCO presents a 0.46 %/°C deviation. Regarding the voltage supply, its variation translates to 1.85 %/V. Synchronizing both oscillators reduce significantly the RCO frequency deviations.

To allow for the frequency to be adjusted according to the reference frequency, calibration is added to the RCO through a digital control word, turning it into a digitally-controlled RCO. Calibration is achieved by adjusting the capacitor bias current and is done in two phases: coarse and fine calibration. For the coarse calibration, current branches are added in parallel with the current mirror, charging the capacitor. After the coarse calibration, the fine calibration takes place. The bias resistor is divided into a fixed part plus a digitally controlled part, composing the bias current fine calibration.

The coarse calibration current branches have binary weights and, due to the size of the PMOS transistors, only four current branches are used. Simulating variations of the control word for the nominal corner the calibration performance is tested. After the coarse calibration, the frequency still has a variation of approximately 2 kHz. The fine calibration should be dimensioned to cover the variation from coarse calibration, assuring the error after 12 h of operation do not exceed 5 min. This represents a frequency deviation of 230 Hz from the desired frequency, 31.25 kHz. To achieve this results seven resistors with binary weights are used, being the least significant resistor 3.85 kHz.

Using binary-weighted resistors, instead of all the resistors with the same value (adequate for thermometer coding), the circuit area and the number of control bits needed is reduced, however in situations with a large number of bits transitions the result is more unstable. In the total, 11 bits are used in the RCO frequency calibration control.

The implemented RCO performance is summarized in Table II and it is compared with state-of-the-art works presented in literature. With a nominal frequency of 31.24 kHz, 0.032 % deviation from the desired value, the RCO has a low power consumption, better then several works in the literature and the RMS phase jitter is matched to the values reported.

TABLE II: Comparison of RC oscillator with state-of-the-art works.

Reference	This work	[22]	[23]	[24]	[10]
CMOS process [nm]	130	130	180	180	180
Frequency [kHz]	31.25	32	32.7	31.25	32.7
Supply voltage [V]	1.2	1.2	0.6	1.8	0.85
Power consumption [nW]	78.5	80	51	360	54.2
Phase noise (@1 kHz) [dBc/Hz]	-57.78	-61.33	NA	NA	NA
RMS jitter (120 Hz-20 kHz) [µs]	1.05	1.03	NA	NA	0.17

C. Period counter

Knowing the XO inputs a 32 MHz signal to the counter, if the RCO is at the desired frequency of 31.25 kHz the counter reaches 1024 cycles during one period of the RCO. A 11-bit counter allows to go up to 2047 cycles per RCO period, corresponding to a frequency of two times the nominal. The counter detects frequency variations between 15.625 kHz (2048 XO cycles for each RCO cycle) and 32 MHz (one XO cycle for each RCO cycle) with a minimal step of 30.5 Hz at the nominal frequency, a range enough to cover the RCO corners frequency variation. Figure 16 shows the 11-bit period counter schematic.

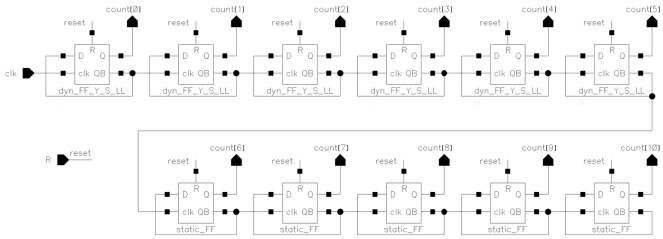

Fig. 16: Implemented calibration loop period counter.

The circuit implemented is an asynchronous up counter, each Flip-Flop (FF) clock input is connected to the previous FF output - except for the first one which clock is the XO output signal - and the Least Significant Bit (LSB) corresponds to the first FF complementary output, Q_B, and the Most Significant Bit (MSB) to the last FF Q_B signal. To obtain a better performance and lower power consumption dynamic and static flip-flops are used to design the counter. The dynamic FFs perform better at high frequencies than the static ones, however this topology fails at lower frequencies, therefore static logic is used for the last five FFs. The dynamic FFs implemented follow the True Single-Phase Clock (TSPC) topology, introduced by Yuan et al. [25], and uses low-leakage transistors to reduce the counter power consumption. The static FFs are based on 3-port NAND circuits.

Figure 17 shows the output of the four FFs with higher weight for one complete cycle of the counter - one period of the most significant output bit. The input clock signal has a frequency of 32 MHz and each FF output frequency is half the previous one.

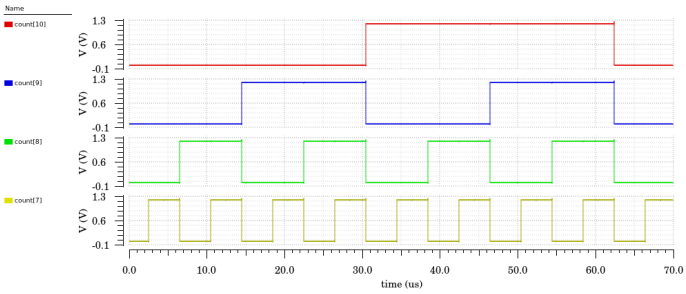

Fig. 17: Period counter output signals.

With the decrease of clock frequency each FF consumes less than the previous one. From the first dynamic FF, with a clock frequency of 32 MHz, through the last static FF, with a clock frequency of 31.25 kHz, the counter has a total power consumption of 997 nW for one counter cycle (from 0 to 2047). Being a digital circuit, the period counter has a low current during the majority of time, except for the output transitions where current peaks occur.

Situations where a high number of transitions is involve are not ideal for a binary counter. In a binary counter the bits change sequentially, therefore it goes through scenarios where the majority of bits has to change. With the FFs with different operating speeds, the transitions occur in different instants, generating unwanted intermediate states. A possible solution for this problem is to use a counter where in each cycle only one bit is changed, for instance, Gray counter ou Johnson counter.

Gray code for a counter of 11 bits implies a high number of logic gates. A n-bit Gray counter logic is usually n-1 gates deep [26], with the number of gates in each level increasing face to the previous level. About 2^n+n logic gates are needed to implemented a n-bit Gray counter. With all this logic, in addition to a high circuit complexity, the power consumption increases significantly. An alternative could be to use a binary counter and convert its output to Gray code. However, since the conversion is based in logic gates, and although its number is reduced, any change in the binary counter output is propagated to the Gray counter output, thus, intermediate undesired states are visible even after the conversion. This is not an adequate solution for this problem.

Another solution may be to use a ring counter such as a Johnson counter, a topology which also presents variations in only one bit in each cycle. Yet, this is a synchronous counter, originating a metastability problem. The need for more bits when compared with other counter topologies is also a disadvantage of the Johnson counter. While the binary counter need only n bits to originate 2^n states in a Johnson counter of 2^n only 2n state are used. For this type of counter to reach 2048 cycles it would need 1024 bits, meaning 1024 FFs.

Although good alternatives to binary counters in some situations, derived to the number of bits of the wanted counter none of the presented solution is satisfactory. The chosen solution is to use the binary counter and delay the reading of its output in the calibration logic block. Figure 18 shows the simulation of the worst case where all counter bits change.

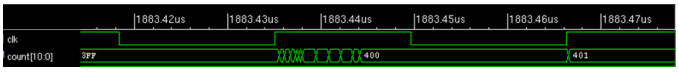

Fig. 18: Counter output example with transition of all bits.

The counter output reading is synchronized with the negative edge of the clock signal (crystal oscillator signal) to allow the output to stabilized before the reading and guarantee the read value is the correct one. The counter must be dimensioned to guarantee the worst case takes less than half a clk period to change all the counter bits.

D. Calibration algorithm

The calibration logic block is responsible for generating the correct 11-bit calibration word which will brings the RCO frequency closest possible to 31.25 kHz. This calibration word is divided into two parts: one corresponding to the capacitor charging current branches; and one to the bias resistors. As seen in III-B both current branches and bias resistors are binary weighted, with 4 and 7 control bits, respectively, and being the current branches responsible for a higher variation in the current.

Calibration word is changed after the RCO output signal positive edge. Since the calibration word is applied to the current branches and bias resistors the current is directly affected. The idea is to avoid current peaks at RCO output signal edges which would result in a bias current different from the expected for this calibration word. With a different value of bias current a different output frequency is obtained. After the current peak, the bias current, and consequently the output frequency, would settle in the correct value for that calibration word however it would take more time.

Even so the RCO frequency takes a few cycles to stabilize, thus after the calibration word update the reset signal waits for two RCO cycles before allowing the count to begin, given the frequency time to settle. At the end of the next RCO cycle the counter final value is used to select the necessary correction. A flowchart indicating the calibration algorithm is presented in Figure 19.

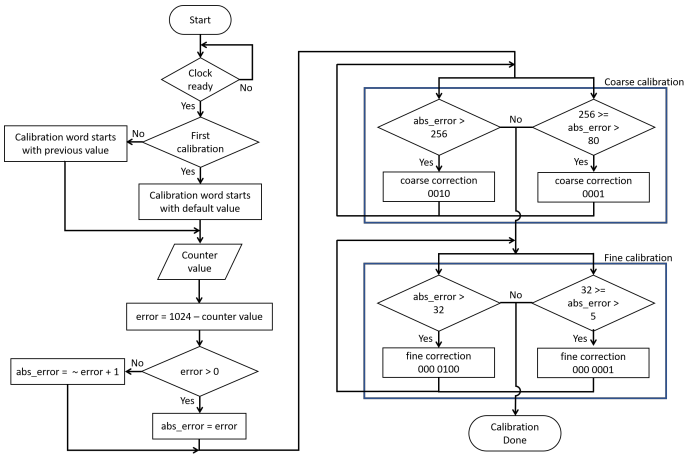

Fig. 19: Flowchart of calibration algorithm.

If it is the first time the system is calibrated it starts with the default calibration word, word simulated as the correct one for the nominal corner. Otherwise, the initial calibration word is the one selected in the previous calibration. This would allow for process variations to be corrected in the first calibration and in the next ones only errors related with temperature and supply voltage are corrected, reducing the calibration time.

When one RCO period has passed, the counter output is read and the error is calculated as the difference to 1024 cycles. To simplify the implementation of the comparison between the error value and the defined limits, the error absolute value is used. If the error is negative, that is, the number of cycles counted is greater than 1024, its absolute value is calculated as the complement for two of its value. Coarse calibration controls the 4 bits which correspond to the current branches charging the capacitors. If the error is less than 80 cycles it

automatically goes to fine calibration, otherwise depending on the error the coarse correction is 1xLSB or 2xLSB. The coarse calibration at the nominal corner covers a frequency range of 3.91 kHz and 53.2 kHz.

In the fine calibration other two corrections are available, 1xLSB for errors less than or equal to 32 cycles and 8xLSB for higher errors. During simulations of the complete system the value of the bias resistor responsible for the fine calibration defined during the RCO design is adjusted to cover the desired frequency range. After this correction, at the nominal corner, this part of the calibration covers frequency variations of approximately 3.45 kHz, with a minimum step of about 35 Hz. At other corners that not the nominal the minimum step corresponds to - in the worst case - an absolute error variation of 10 XO cycles for each RCO cycle, therefore, the distance to the nominal value (1024) is at most 5 XO cycles. This value, 5 cycles, is selected as the limit which ends the calibration. If a lower limit is defined, with some PVT corners, the system would be in the calibration loop indefinitely. 20 illustrates a calibration cycle example.

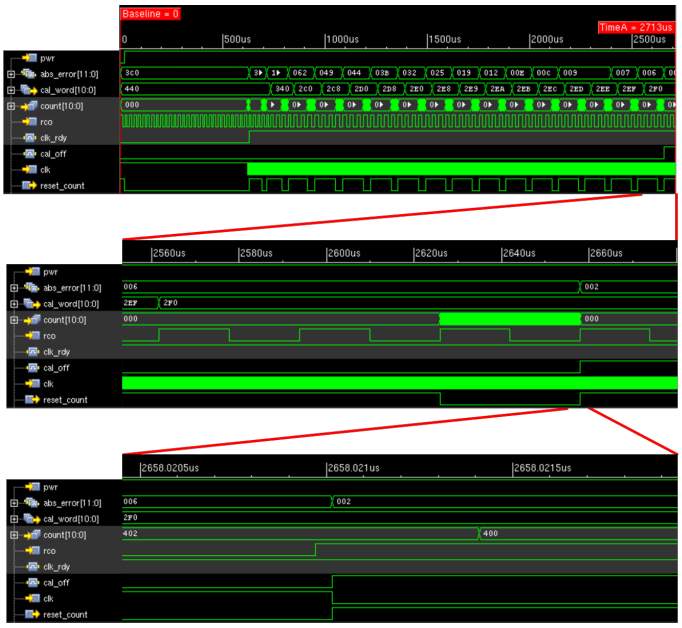

Fig. 20: System calibration simulation.

Figure 20 shows the evolution of the system calibration, from the time the XO is turned on until the calibration is complete. A signal, clk_rdy, indicates the clock start-up time has passed and it is ready for use. When this signal goes high the calibration starts; every three RCO cycles the frequency error is analyzed and the calibration word, cal_word, is actualized. The calibration absolute error, represented by the variable abs_error, decreases with each iteration. When it reaches less than five cycles of error (two cycles in the illustrated case) the variable cal_off is activated, signalizing the end of the calibration.

The calibration is limited at lower frequencies by the counter which can only detect a minimum RCO frequency of 15.625 kHz and at higher frequencies by the oscillator digital control which can only correct frequencies below 53.2 kHz. If the system is powered on every 12 hours to synchronize the oscillators an error of $\pm$ 5 cycles translates into an error of approximately $\pm$ 5 minutes before or after the power up correct instant. To improve the system performance this error must be reduced to a minimum.

Variations of temperature and voltage supply are simulated for the complete system and the RCO frequency is compared before and after calibration. For temperatures between -40 °C and 80 °C the oscillation frequency presents a deviation of 93.8 ppm/°C after calibration. Regarding the 10% variation of the voltage supply the frequency deviation after calibration is 1.75 %/V. Table III compares this work RCO frequency deviation (before and after calibration) with state-of-the-art works.

TABLE III: Comparison of RC oscillator before and after calibration with state-of-the-art works.

Reference	This work		[22]	[23]	[24]	[10]
CMOS process [nm]	130		130	180	180	180
Frequency [kHz]	31.25		32	32.7	31.25	32.7
Supply voltage [V]	1.2		1.2	0.6	1.8	0.85
Temperature deviation [ppm/°C]	93.8 [a]	4600 [b]	10	43.1	4000	99.5
Supply voltage deviation [%/V]	1.75 [a]	1.85 [b]	NA	-1.2	5	0.89

[a] after calibration
[b] before calibration

IV. Conclusions

There are many challenges to overtake in the design of a low-power clock generator system. An high frequency stability of the clock signal must be guaranteed, as well as a duty-cycle of 50%. In the case of the oscillator used to keep track of time power consumption is of extreme importance and achieve the desired performance without recurring to spend more current presents itself as a big challenge. To assure the power up occurs at the correct instant synchronization between both oscillators is introduced in the system. Synchronization should end as soon as possible without forgetting that the system must be low-power, that is, some care has to be taken to keep the power consumption to a minimum without compromising the oscillators tuning.

A 32 MHz crystal oscillator is chosen as the reference oscillator for its high Q, which translates into a high frequency stability. Keeping in mind the low-power specification of the system, the crystal oscillator transistors are thus dimensioned for the lowest start-up energy solution.

The buffer, used to transform the crystal oscillator output into a square wave, is dimensioned for a 5 pF load capacitor to guarantee it operates correctly when introduced in the system, however its simulated power consumption suffers with the decision of using a value so high. To compare the implemented XO and buffer with the literature works it is again simulated with a 500 fF load capacitor, a more reasonable value for

this application. The results obtained are not as good as the state-of-the art works. Adding a quick start-up technique to the crystal oscillator would allow a faster start-up and, consequently, a lower value of consumed energy.

A current-comparator-based RCO is chosen as the preferred ULP oscillator topology for this application for its lower power consumption and correct operation for PVT variations. The ULP wake-up oscillator frequency is chosen as be 31.25 kHz, a power of two of the XO frequency, therefore a binary counter can be used in the synchronization mechanism. This oscillator presents a high frequency deviation in the corners simulation, however the oscillation frequency error is decreased by the calibration.

In this topology, the oscillator frequency is defined both by the capacitor size and bias current (or bias resistor). To avoid large area consuming capacitors banks, it is chosen to adjust the bias current in order to correct the frequency. The implemented calibration algorithm assumes calibration is complete with errors equal to or less than 5 cycles of XO for each RCO cycle, to assure the calibration ends even in the worst case corner. After calibration, and considering the 5 XO cycles of error, the RCO still presents a maximum error of $\pm$ 5 min from every 12 h of operation. It is important to reduce this error to a minimum, possibly by adding more bits to the calibration word, decreasing its minimum step.

Comparing with others presented in the literature, this work presents a XO with higher start-up time, however no technique is implemented to accelerate this phase of the oscillator. The ULP oscillator offers comparable values of phase jitter and power consumption, surpassing some of the literature works. The temperature and supply voltage deviation after calibration is comparable to some of the literature works, however, after the calibration, the frequency still presents an error of 5 min for every 12 h of operation.

REFERENCES

[1] K. K. Lee, K. Granhaug, and N. Anderson, "A study of low-power crystal oscillator design" in 2013 NORCHIP, pp. 1-4, Nov 2013.

[2] A. Saito, Y. Zheng, K. Watanabe, T. Sakurai, and M. Takamiya, "0.35V, 4.1μW, 39MHz Crystal Oscillator in 40nm CMOS," in International Symposium on Low Power Electronics and Design (ISLPED), pp. 333-338, Aug 2012.

[3] Q. Zha, T.Lu, Y. Zong, J. Zhang, and S. Qu, "Design of CMOS Crystal Oscillator with Low Power Consumption," International Journal of Information and Electronics Engineering, vol. 3, pp. 630-633, Nov 2013.

[4] S. Iguchi, H. Fuketa, T. Sakurai, and M. Takamiya, "Variation-Tolerant Quick-Start-Up CMOS Crystal Oscillator With Chirp Injection and Negative Resistance Booster," IEEE Journal of Solid-State Circuits, vol. 51, pp. 496-508, Feb 2016.

[5] D. Griffith and J. Murdock, and P. T. Rine, "A 24MHz crystal oscillator with robust fast start-up using dithered injection," in 2016 IEEE International Solid-State Circuits Conference (ISSCC), pp. 104-105, Jan 2016.

[6] H. Esmaeelzadeh and S. Pamarti, "A Quick Startup Technique for High-Q Oscillators Using Precisely Timed Energy Injection," IEEE Journal of Solid-State Circuits, vol. 53, pp. 692-702, March 2018.

[7] M. Ding, Y. H. Liu, Y. Zhang, C. Lu, P. Zhang, B. Busze, C. Bachmann, and K. Philips, "A 95μW 24MHz digitally controlled crystal oscillator for IoT applications with 36nJ start-up energy and $>13\times$ start-up time reduction using a fully-autonomous dynamically-adjusted load," in 2017 IEEE International Solid-State Circuits Conference (ISSCC), pp. 90-91, Feb 2017.

[8] G. De Vita, F. Marraccini, and G. Iannaccone, "Low-Voltage Low-Power CMOS Oscillator with Low Temperature and Process Sensitivity," in 2007 IEEE International Symposium on Circuits and Systems, pp. 2152-2155, May 2007.

[9] M. Scholl, Y. Zhang, R. Wunderlich, and S. Heinen, "A 80 nW, 32 kHz charge-pump based ultra low power oscillator with temperature compensation," in ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pp. 343-346, Sept 2016.

[10] H. Asano, T. Hirose, K. Tsubaki, T. Miyoshi, T. Ozaki, N. Kuroki, and M. Numa, "A 1.66-nW/kHz, 32.7-kHz, 99.5ppm/C fully integrated current-mode RC oscillator for real-time clock applications with PVT stability," in ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pp. 149-152, Sept 2016.

[11] L. Joonhyung, L. Kwangmook, and C. Koonsik, "Ultra low power RC oscillator for system wake-up using highly precise auto-calibration technique," Procedia Engineering, vol. 64, pp. 377-384, Sept 2010.

[12] K.K. Abdul Majeed and Binsu J. Kailath, A Novel Phase Frequency Detector for a High Frequency PLL Design," in 2010 Proceedings of ESSCIRC, pp. 274-277, 2013. International Conference on Design and Manufacturing (IConDM2013)

[13] C. Jeong, D. Choi, and C. Yoo, "A fast automatic frequency calibration technique for a 26 GHz frequency synthesizer," International Journal of Circuit Theory and Applications, vol. 42, March 2014.

[14] W. Sansen, Analog Design Essentials. The Springer International Series in Engineering and Computer Science, Springer US, 2007.

[15] E. A. Vittoz, M. G. R. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: theory and application," IEEE Journal of Solid-State Circuits, vol.23, pp. 774-783, June 1988.

[16] S. Iguchi, H. Fuketa, T. Sakurai, and M. Takamiya, "Variation-Tolerant Quick-Start-Up CMOS Crystal Oscillator With Chirp Injection and Negative Resistance Booster," IEEE Journal of Solid-State Circuits, vol. 51, pp. 496-508, Feb 2016.

[17] H. Esmaeelzadeh and S. Pamarti, "A Quick Startup Technique for High-Q Oscillators Using Precisely Timed Energy Injection," IEEE Journal of Solid-State Circuits, vol. 53, pp. 692-702, March 2018.

[18] M. Ding, Y. H. Liu, Y. Zhang, C. Lu, P. Zhang, B. Busze, C. Bachmann, and K. Philips, "5.3. A 95 μ W 24 MHz digitally controlled crystal oscillator for IoT applications with 36 nJ start-up energy and $>13\times$ start-up time reduction using a fully-autonomous dynamically adjusted load," in 2017 IEEE International Solid-State Circuits Conference (ISSCC), pp. 90-91, Feb 2017.

[19] Epson Seiko, "Crystal Oscillator - SG-210STF." https://support.epson.biz/td/api/doc_check.php?mode=dl&lang=en&Parts=X1G0041710040

[20] P. Gray, P. Hurst, S. Lewis, and R. Meyer, Analysis and Design of Analog Integrated Circuits. John Wiley & Sons, Inc., 4 ed., 2001.

[21] Q. A. Khan, S. K. Wadhwa, and K. Misri, "Low power startup circuits for voltage and current reference with zero steady state current," in Proceedings of the 2003 International Symposium on Low Power Electronics and Design, 2003. ISLPED '03., pp. 184-188, Aug 2003.

[22] M. Scholl, Y. Zhang, R. Wunderlich, and S. Heinen, "A 80 nW, 32 kHz charge-pump based ultra low power oscillator with temperature compensation," in ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pp. 343-346, Sept 2016.

[23] Y. Zheng, L. Zhou, F. Tian, M. He, and H. Liao, "A 51-nW 32.7-kHz CMOS relaxation oscillator with half-period pre-charge compensation scheme for ultra-low power systems," in 2016 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 830-833, May 2016.

[24] L. Joonhyung, L. Kwangmook, and C. Koonsik, "Ultra low power RC oscillator for system wake-up using highly precise auto-calibration technique," in 2010 Proceedings of ESSCIRC, pp. 274-277, Sept 2010.

[25] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," IEEE Journal of Solid-State Circuits, vol. 24, pp. 62-70, Feb 1989.

[26] A. Maheshwari, W. Burleson, and R. Tessier, "Trading off Reliability and Power-Consumption in Ultra-low Power Systems," pp. 361-366, Jan 2002.