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Adaptive Neural Networks based on Metal-Insulator-Metal Nanostructures (Memristors)

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The sky above the port was the color of television, tuned to a dead channel.

William Gibson, *Neuromancer*

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Resumo

Recentemente novas arquitecturas de computação têm sido estudadas para ultrapassar os limites do paradigma tradicional de von Neumann e o fim iminente da lei de Moore. Uma alternativa promissora é a computação neuromórfica, baseada em algoritmos não lineares, altamente paralelizáveis, que mimetizam o funcionamento de redes neuronais biológicas. Estas versões artificiais podem ser implementadas usando memristors, componentes electrónicos fundamentais e passivos, que exibem mudanças de estado resistivo estáveis e reversíveis, traduzindo-se no mesmo comportamento eléctrico de neurónios biológicos.

Este trabalho foca-se na optimização do processo de microfabricação de dispositivos memristivos baseados em óxido de magnésio, tanto em configuração individual como em rede. Dois processos diferentes são implementados: o primeiro, mais completo, onde a junção metal-dieléctrico-metal é definida por litografia óptica e gravura por feixe de iões, e um segundo, mais simples, onde o eléctrodo inferior é delineado primeiro e a junção é definida através da pulverização com magnetrão do dieléctrico e do eléctrodo superior em sobreposição precisa. Microscopia SEM é utilizada para identificar defeitos na fabricação.

Um programa de computador é desenvolvido para o controlo de uma fonte de tensão-corrente, com vista à medição dos dispositivos memristivos usando varrimentos de tensão-corrente. Estruturas individuais respeitantes ao processo longo exibem grandes rácios de resistência ON-OFF, de no mínimo 10^3. O rendimento deste processo e a duração dos dispositivos é reduzida, respectivamente 43% e menos de 10 trocas completas de estado; estruturas em rede não demonstram melhorias. O segundo processo demonstra melhores resultados; no entanto, a margem para optimização continua ampla.

Palavras-chave: Memristor, Computação neuromórfica, Óxido de magnésio, Pulverização por magnetrão, Comutação resistiva

Abstract

In recent years novel computer architectures have been pursued to overcome the limitations of the traditional silicon-based von Neumann paradigm and the imminent end of Moore's law. A promising alternative is neuromorphic computation, which is based on non-linear, massively parallel, neural-like algorithms, allowing the construction of artificial neural networks. These can be implemented using memristors, fundamental and passive electric components that show reversible and persistent resistance state changes, which translate in similar electric responses to biological neural tissue.

In this work we study the optimization of the microfabrication process of individual and crossbar arrays of magnesium oxide-based memristive devices. Each configuration is implemented in two different fabrication processes: a more complete procedure where the main metal-insulator-metal pillar is defined using optical lithography and ion beam milling and a simpler, two-level process where the bottom electrode is patterned first and the junction is defined by magnetron sputtering of the insulator film and top electrode, overlapping precisely with the former. SEM imaging is used to identify defects in the fabricated structures.

A computer program is developed to control a voltage-current sourcemeter, to perform automatic voltage-current sweeps with flexible parameters for measurement of memristive devices. Individual structures fabricated with the first process show large ON-OFF resistance ratios of at least 10^3, although the process yield and average device endurance are low, respectively at 43% and less than 10 full switching cycles. Crossbar arrays do not show improved performance. The two-step process yields better results, although the margin for improvement is still extensive.

Keywords: Memristor, Neuromorphic computation, Magnesium oxide, Magnetron sputtering, Resistive switching

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Nomenclature

CF Conducting filament

HRS High-resistive state

LRS Low-resistive state

MgO Magnesium oxide

MIM Metal-insulator-metal [structure]

nm Nanometer; 10^{-9} m

OFF Off state; same as HRS

ON On state; same as LRS

Reset LRS to HRS transition

RS Resistive switching

Ru Ruthenium

Set HRS to LRS transition

Ta Tantalum

μm Micrometer, micron; 10^{-6} m

Å Angstrom; 10^{-10} m

Chapter 1

Introduction

1.1 Motivation

The unrelenting advances in silicon technology that have been proving Moore's Law correct for the past four decades are waning. We are starting to hit fundamental physical limits in our quest for ever more miniaturized and powerful electronics, and we must soon turn our attention elsewhere to keep improving the tools we use to tackle ever more complex problems [1, 2].

At the same time, aided by this "silicon explosion", we have been experiencing an enormous boost in the field of artificial intelligence: it has been twenty years since Deep Blue beat the world chess champion Kasparov in 1997. More recently, deep learning techniques have been making their way into many applications and tools, that can process huge amounts of data rather quickly, for instance in facial and speech recognition, computer vision, among others which are now ubiquitous in our daily life. [3, 4].

Despite these breakthroughs, our ability to simulate human thinking in conventional computers will eventually reach a limit, due to the end of Moore's Law but also because our brain, one of the most complex structures we know and from which we still know very little, is structured in a radically different way than the predominant von Neumann architecture; while the latter has a strict and deterministic input-processing-memory interface-output hierarchy, we benefit from having a very large number of individual processing cells, the neurons, connected with each other in a non-linear and massively parallelized arrangement. This allows us to trivially perform tasks such as learning new concepts and extrapolate our past experiences to future events, something even the most powerful supercomputers struggle with.

We must start working to build a fundamentally different computer architecture so that we can build artificial neural networks capable of having the same low power consumption as our brains and implement in a machine those tasks we excel at. To do that, very promising building blocks have recently gathered much interest, which are memristive systems. These are two-terminal passive electronic components which feature a non-linear relationship between current and voltage, and as we will see later on, this seemingly simple property makes such devices display a very similar behavior to biological synapses. Combined with their potential for miniaturization and integration, we then have an ideal starting step to build advanced neuromorphic artificial structures [5].

1.2 Framework and objectives

In the last few years memristive devices have been pursued as a way of implementing integrated and scalable artificial neural networks, resorting to a wide variety of inorganic materials.

Work done at INESC-MN in Lisbon, Portugal and in IFIMUP-IN in Porto, Portugal has focused in the optimization of thin film stacks for use in individually patterned memristors. The resistive switching properties of several junction materials have been studied at both institutions. Examples are silver sulfide (Ag_2S) [6], tantalum oxide (TaO), titanium-tungsten oxide (Ti-W-O) and magnesium oxide (MgO) [7]. For the former material gold (Au) and silver (Ag) electrodes were used; for the last three junction materials different electrodes have been tested, namely platinum (Pt), tantalum (Ta) and ruthenium (Ru). Fully patterned devices with junction areas down to 1×1 μm^2 have been fabricated with these materials.

In this dissertation I propose to start from the well established techniques and materials comprising the existing framework and further optimize the fabrication processes used for these devices. The main contribution of this work will be the microfabrication of reliable memristive structures in a crossbar array configuration, for posterior integration in a neural-like artificial network.

To that end, several intermediate objectives have been defined:

- Characterization of Pt/MgO/Ta/Ru thin film stack materials.
- Optimization of fabrication processes for the patterning of isolated memristors and crossbar arrays.
- Extension of the memristor electric characterization facilities available at INESC-MN.
- Characterization of the electric properties of the finished devices.

1.3 Thesis Outline

A synthesis of each chapter of this document is provided below.

In Chapter 2, a brief summary of the theoretical concepts applied in this work are described, namely in the topics of memristors and memristive systems, neurons and synapses, memory and functional changes to neural tissues, artificial neural networks and their development using memristive devices. A review of the state of the art literature is provided, on the topics of materials optimization and resistive switching phenomena.

In Chapter 3, a short description of the equipment and techniques used in this work is given. A study of metal and insulator thin films deposited at INESC-MN is presented. The fabrication processes of memristive devices are explained in detail.

In Chapter 4, the results of the characterization of the finished devices are presented and interpreted according to the theoretical predictions. The fabrication process is studied and improvement avenues are discussed.

In Chapter 5, the conclusions of this work are presented.

Chapter 2

Background and state of the art

2.1 Memristors and memristive systems

A memristor (from memory resistor) is a passive, two-terminal electric component whose resistance can be changed, depending on the applied voltage, or current, and for how long it has been applied.

The theoretical derivation of the memristor was first performed by Chua in 1971 [8]. In his work, he related the four fundamental electromagnetic circuit quantities - the electric charge q, the magnetic flux φ, the voltage V and the current I - to each other in a pairwise manner through 4 + 2 constituting relations:

$$\begin{aligned} dV &= R\,dI \\ d\varphi &= L\,dI \\ dq &= C\,dV \\ d\varphi &= M\,dq \end{aligned} \qquad (2.1)$$

$$\begin{aligned} dq &= I\,dt \\ d\varphi &= V\,dt \end{aligned}$$

The last two equations come from basic electromagnetism: respectively, the definition of electric current and Faraday's law, and they relate two circuit quantities to the temporal variation of the other two. The other four correspond to the four fundamental passive circuit elements (summarized in Fig. 2.1), where R, L, C, M are respectively the resistance, inductance, capacitance and memristance.

For a long time only the first three relations were realized in physical devices, and from symmetry considerations Chua realized that a fourth canonical circuit element must exist in order to satisfy the equation relating magnetic flux and electric charge. Furthermore, he also showed that the behavior of a passive device characterized by a variable memristance $M \equiv M(q)$ that satisfies Eq. 2.1 cannot be reproduced by any combination of resistors, inductors and capacitors, proving this device is fundamental.

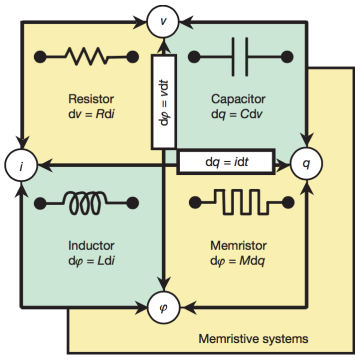


Figure 2.1: The four canonical circuit elements (reused with permission from Ref. [9]).

Using the relations in Eq. 2.1 we see right away that M has the dimensions of a resistance, and so a general memristor relating flux and charge can equivalently be seen as a non-linear resistor relating voltage and current, whose resistance at some instant t_0 is a function of the history of the current that has passed through the device at all past times:

$$M(q) = M\left(\int_{-\infty}^{t_0} I(t)\,dt\right) \tag{2.2}$$

We see that the memristor is then aptly named, since its behavior is determined by the memory of its state at all points in the past.

After Chua's pioneering work, the concept of memristor was promptly generalized to a broader category of devices, called memristive systems, by Chua and Kang [10]. In the case of current-controlled memristive systems, they are characterized by the following set of equations:

$$V(t) = R(\boldsymbol{w}, I, t)\, I(t) \tag{2.3}$$

$$\frac{d\boldsymbol{w}}{dt} = f(\boldsymbol{w}, I, t) \tag{2.4}$$

where $\boldsymbol{w}$ is a set of n internal state variables, R is a generalized resistance and f is a generic function.

The practical realization of the memristor finally came about in 2008, 37 years after its theoretical prediction, by Strukov *et al.* [9], who built a nanodevice consisting of a thin semiconductor layer mounted between two metallic contacts. This device makes use of a property widely observed in such thin-film structures called resistive switching: the resistance of the device is not fixed but can in fact be tuned with the controlled application of a particular voltage to its terminals.

In this particular case, the switching is achieved by the presence of oxygen vacancies in the semiconductor material. These can be treated as a positively charged dopant, in a way that, across the film thickness D, a restricted region has a high dopant concentration, while another is essentially undoped, and during operation, the boundary between these two regions will shift through dopant motion and drift. The dopant will contribute to an increase in the conductivity of the regions it is inserted in, and in the limit where we have the whole layer doped, we define a characteristic low resistance R_{ON}. Likewise, if

the boundary shifts in a way that we have essentially no dopant across the layer, then it has a very low conductivity and we are in a high-resistance state R_{OFF}. This way we can define an equivalent circuit of our nanodevice, depicted in Fig. 2.2.

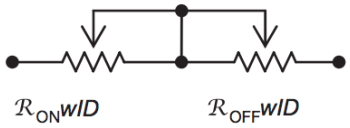


Figure 2.2: Equivalent circuit (reused with permission from Ref. [9]).

In this device, w is the effective thickness of the doped region of the layer, and this quantity is then the (scalar) state variable of interest. This allows us to find an explicit expression for the memristance of the device, considering that its generalized resistance is a weighted average, using w, of R_{ON} and R_{OFF}. Eqs. 2.3 and 2.4 take the following form:

$$V(t) = \left(R_{\text{ON}} \frac{w(t)}{D} + R_{\text{OFF}} \left(1 - \frac{w(t)}{D} \right) \right) I(t) \tag{2.5}$$

$$\frac{dw}{dt} = \mu_V \frac{R_{\text{ON}}}{D} I(t) \tag{2.6}$$

where μ_V is the mobility of the vacancies. Integrating the second equation for all past times, we get an identical expression with charge instead of current, and substituting in the first equation, we get:

$$V(t) = \left(R_{\text{ON}}^2 \frac{\mu_V}{D^2} q(t) + R_{\text{OFF}} \left(1 - \frac{\mu_V}{D^2} R_{\text{ON}} q(t) \right) \right) I(t) \tag{2.7}$$

and so we get a memristance:

$$M(q) \approx R_{\text{OFF}} \left(1 - \frac{\mu_V}{D^2} R_{\text{ON}} q(t) \right) \tag{2.8}$$

where we simplified the expression considering the approximation $\frac{R_{\text{ON}}}{R_{\text{OFF}}} \ll 1$, the desired condition and what is typically the case for practical devices.

The expression obtained for the memristance in Strukov's model immediately shows why such memristive characteristics took such a long time to be discovered in practice, after the three classical passive circuit elements: the dependence on $\frac{1}{D^2}$ means that memristance is only relevant at very short scales, on the order of the nanometer. For macroscopic devices the second term in Eq. 2.8 is essentially zero, and we recover the behavior of a classical, linear resistance.

2.1.1 Conducting filaments and resistive switching

More recent studies on the nature of memristive behavior have developed a new model for the memristance of a metal-insulator-metal structure, widely used for a variety of materials. Rather than having a uniformly doped insulator layer whose boundary shifts translate to a change in the electric resistance

of the device, resistance changes in this model are driven by the formation and destruction of very thin and localized filaments of conducting material inside the insulator film (shown in Fig. 2.3). These have been demonstrated to be responsible for a large variety of resistive switching (RS) phenomena in a huge amount of materials, particularly in the context of resistive random-access memories (ReRAMs) research [11, 12, 13, 14].

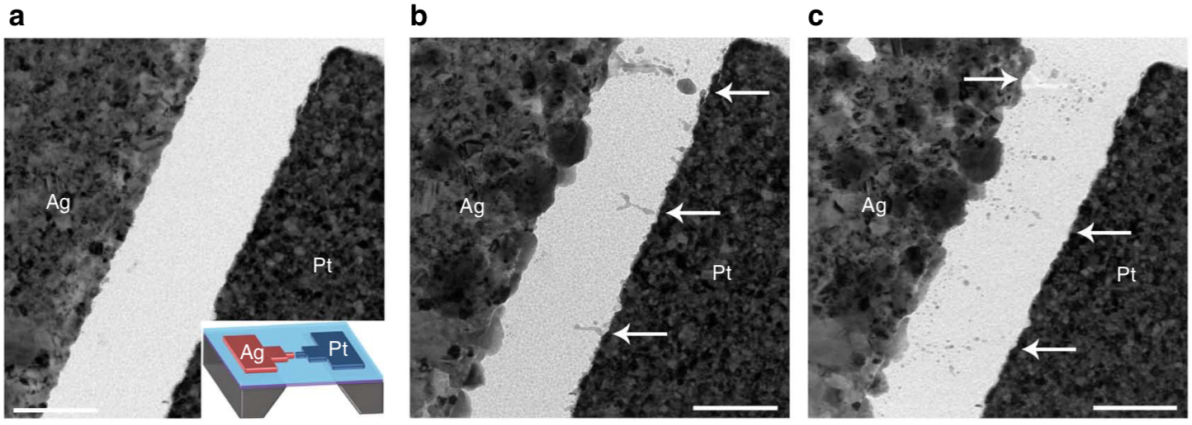


Figure 2.3: Filament formation and degradation in a Ag/SiO_2/Pt memristive structure; a): As-fabricated device; b): Filament forming; c): Filament erasure (reused with permission from Ref. [15]).

ReRAMs are devices can be programmed as non-volatile logical states (OFF - 0 or ON - 1) which are physically realized by changing the resistance of a simple metal-insulator-metal structure between at least two stable states. They present a promising evolution over conventional DRAM, SRAM and Flash memory applications, by combining the main advantages that these technologies present in separate, in terms on access and write speed, packing density and non-volatility, respectively [16, 17], while having the potential to surpass them in terms of power consumption, scalability and operation speed [12, 13].

The fundamental property of a memristor is resistance state switching as well, meaning that the concepts of memristance and resistive memory are intimately linked to one another; thus, by studying one sort of application we gain valuable knowledge about the other.

The specific kinetics and mechanisms of filament formation and degradation depend heavily on the dielectric material, the interfaces with the electrodes and the electrodes themselves, and so these studies comprise a very active topic of research. However, the basic mechanisms and their correspondence in the electric response of the device are reasonably well understood, are summarized below and shown in Fig. 2.4.

Set process and electroforming

The formation of a filament under an applied electric field to the MIM structure depends heavily on the presence of defects and imperfections inside the insulating layer and at the electrode interfaces. In metal oxides, the most common type of material used in RS application, these are mostly metal interstitials in the lattice or oxygen vacancies [18]. The electrostatic force resulting from the applied electric field will then force these defects to migrate from one electrode to the other; however, due to non-uniformities in the distribution of defects this migration will not be uniform, but will tend to originate from localized

defect nuclei. These then grow according to the direction of the electric field and the charge of the defects, forming thin filaments. When a small number of these reaches the opposite electrode the resistance across the device drops suddenly, since there are now a number of conducting paths inside the insulating layer, and filament growth stops. This is called a Set event, when the device transitions from a high-resistive state (HRS/OFF) to a low-resistive state (LRS/ON).

The sudden resistance decrease during the Set transition will result in a sharp increase in the current passing through the device, which in turn causes a significant heating in the vicinity of the filaments due to the Joule effect. It is thought that this heating enhances the reactions responsible for filament formation and thus strengthen it [18]. In order to avoid an irreversible ON state due to an overly strong filament or even physical damage, it is necessary to limit the maximum current sourced to the device. This can be done, for example, when using a transistor-memristor combination or by setting a current compliance value in the external power source [13].

In newly fabricated devices the density of defects in the mostly uniform insulator might be rather low. Defects must then be created or introduced in the oxide, for instance, by electromigration of oxygen atoms from the oxide lattice towards the cathode, thus creating vacancies [13]. This process is called electroforming, and is the reason why the first Set transition in an intact device often requires a larger applied voltage than subsequent HRS to LRS events [12, 18].

Reset process

When the filaments formed during the Set process are broken, the conducting path is interrupted and the device goes back to a highly resistive state. Unlike filament formation, which is consistently an electric field-driven process among most RS oxides, the nature of Reset events varies considerably.

One method for bringing the MIM structure back to the OFF state is simply by reversing the polarity of the applied voltage; in this case the reactions that formed the filament happen in reverse and cause the breaking of the connection. However, it is also possible to achieve a Reset event using the same polarity as the Set transition; it is thought that thermal mechanisms induced by Joule heating promote the dissolution and redox reactivity of the filament material, which eventually cause the filament to break [12, 13, 18]. These are called bipolar and unipolar resistive switching, respectively, and their characteristic I-V curves are depicted in Fig. 2.5.

For materials where the drift of oxygen ions and vacancies is the main RS mechanism a unified model for unipolar and bipolar switching has been proposed [19], in which the relative preponderance of drift, diffusion, and recombination processes dictates the main Reset behavior of the material.

2.1.2 Hysteresis

One of the most important and unique properties of memristive systems is the response they display when subject to a periodic driving signal. In particular, for a sinusoidal input $I(t) = I_0 \cos(\omega t)$, the $V(I)$ response of the system will be a pinched - zero at the origin - hysteretic loop (Lissajous figure), which will be symmetric about the origin if the additional constraint $M(I) = M(-I)$ is met. This behavior

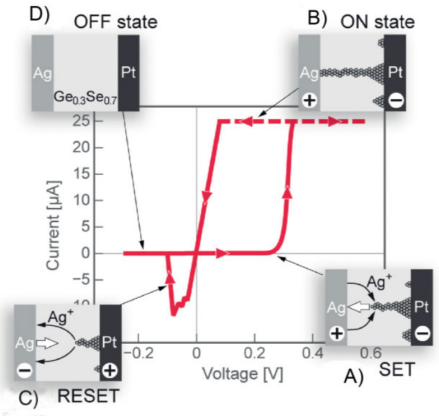


Figure 2.4: Sequential stages of filament growth and breaking (reused with permission from Ref. [12]).

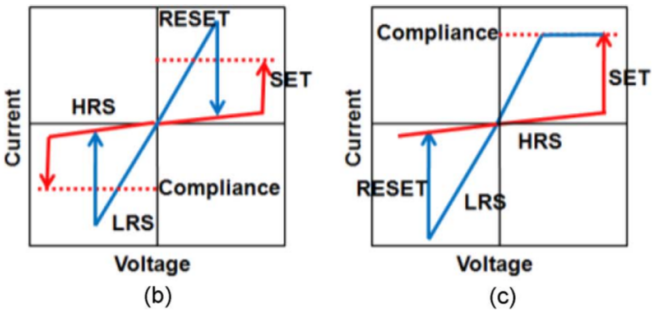


Figure 2.5: Reset transition types; b): Unipolar; c): Bipolar (reused with permission from Ref. [13], © 2012 IEEE).

is easily explained: when the voltage increases, the ions will start accelerating along the electric field, lowering the resistance of the device and thus raising the current. This happens until the voltage reaches the maximum; when it starts decreasing, the ions, due to inertia, are still moving towards the negative electrode, which is why, for a short while, the current keeps increasing while the voltage is decreasing. The same happens for the negative voltage sweep, and thus we have two symmetric lobes. In practice the experimental I-V curves of real devices are not symmetric, since, as explained previously, the Set and Reset processes are not physically identical, but depend on different mechanisms.

Furthermore, for increasing ω, the lobes of the Lissajous figure will become tighter, and will eventually degenerate to a straight line as $\omega \to \infty$. This happens because, for higher frequencies the ions, due to their mass, will have trouble following the very quick variation of the electric field and as such w will not change much, and so neither will the memristance. In the limit we get a constant resistance and a linear relationship between I and V. These characteristic are depicted in Fig. 2.6.

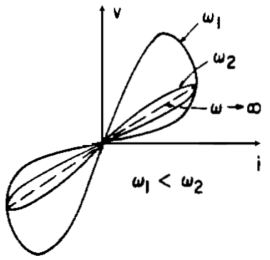


Figure 2.6: Hysteresis loops and variation with frequency (reused with permission from Ref. [10], © 1976 IEEE).

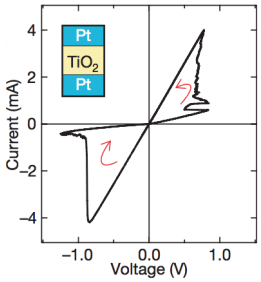


Figure 2.7: Experimental memristor $I(V)$ characteristic (reused with permission from Ref. [9]).

2.2 Neurons and synapses

Our brain is a most complex organ, responsible for everything we learn, what we see, hear and smell, the interpersonal relationships we have, our critical and logic reasoning, the emotions we feel and the memories we form of the most significant events of our life. Despite this incredible complexity and variety of functions, at a fundamental level it all boils down to the way our neurons work and how they connect with each other through special connections called synapses, forming the neural networks in our brain.

The neuron is a specialized cell that is excitable by electric signals and whose task is to receive those inputs, process them and propagate them to the other neurons connected to it. As depicted in Fig. 2.8, a neuron is comprised of several specialized structures: the dendritic branches connect the previous neurons in the network to the main cell body, called the soma, where the signal will be processed; from there, the output will be sent along a long projection called the axon, which will branch out at the termination into telodendritic branches, establishing synapses to the following neurons.

The synapse is the specialized structure that connects neurons to each other. When an electric spike V_{pre} reaches the end of the axon of the pre-synaptic neuron, chemical markers called neurotransmitters will be released to the outside of the cell, diffusing to the synaptic cleft and activating receptors on the post-synaptic neuron membrane, changing the permeability of ion channels also present there. This allows the diffusion of ions in and out of the neuron, changing the electric potentials inside and outside the membrane, and thus a second spike V_{post} forms and propagates further [20]. The mechanism is illustrated in Fig. 2.9, where the voltage spikes are defined by the potentials outside and inside the membrane:

$$\begin{aligned} V_{\text{pre}} &= V_{\text{pre+}} - V_{\text{pre-}} \\ V_{\text{pos}} &= V_{\text{pos+}} - V_{\text{pos-}} \end{aligned} \tag{2.9}$$

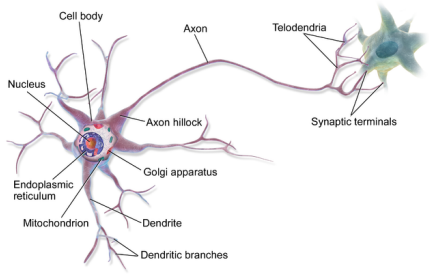


Figure 2.8: Structure of a neuron (reused with permission from Ref. [21]).

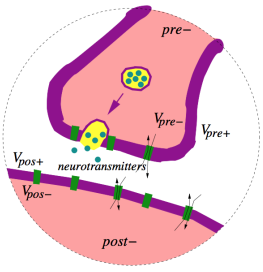


Figure 2.9: Chemical synapse (reused with permission from Ref. [20]).

2.2.1 Memory and synapse plasticity

Like a computer, our brains need a mechanism to keep information regarding the things we experience and the cognitive processing we perform, and we know that this information is codified in the strength,

or weight, of synaptic connections. However, the brain does not merely store data; we learn and forget new things, and for that to happen, there must exist a process to change the synaptic strength.

The first model relating neuronal spiking activity and synaptic weight was introduced by Hebb in 1949, whose Hebbian learning postulate stated that when neuron A repeatedly participates in the excitation of neuron B, the efficiency of the electric spike transmission from A to B is increased. In other words, when A and B fire close to each other in quick succession, the synaptic strength increases to reinforce that connection [20]. However, this model is quite limited, since it does not contemplate a mechanism for weight reduction, so a huge number of phenomena are unaccounted for.

A further refinement is achieved with the spike timing dependent plasticity (STDP) model. In this thoroughly experimentally verified framework [20, 22], the change in the synaptic weight now depends on the timing difference between the post and pre-synaptic spikes, respectively t_{pos} and t_{pre}. Formally, we have:

$$\Delta w = \xi(\Delta T), \quad \Delta T = t_{\text{pos}} - t_{\text{pre}} \tag{2.10}$$

where Δw is the synaptic weight change and ξ are typically weighted exponential functions. Depending on which pulse happens first different phenomena occur: if we have $\Delta T > 0$, the pre neuron will fire first and the synapse will be reinforced, thus causing long-term potentiation of the connection (LTP); conversely, the post neuron firing first will lead to a softening of the synapse and long-term depression (LTD) occurs. The closer the two pulses are in time, the stronger the corresponding effect will be, and for lags outside a critical ΔT, typically around 20 ms for LTP and 20-100 ms for LTD, the weight will not change at all. In addition, several pre-post pulses, around 60-100, are necessary to induce LTP/LTD.

In some specialized neural arrangements, we might get the opposite behavior from what is described above: LTP for negative ΔT and LTD otherwise. We then have an inhibitory STDP function ξ. These phenomena are depicted in figure 2.10.

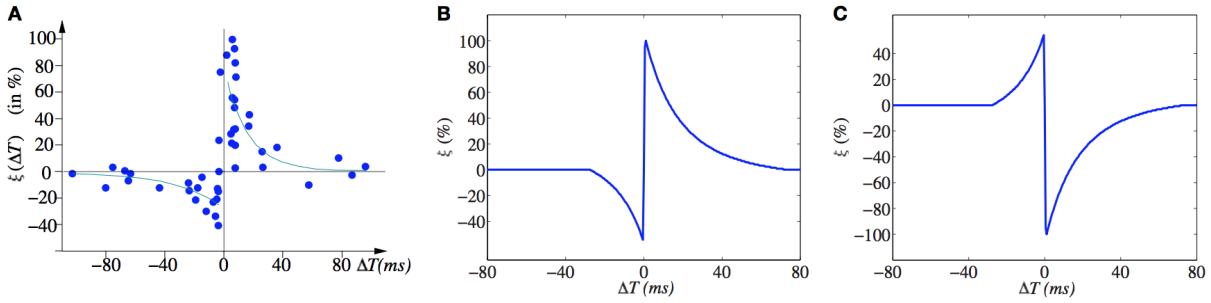


Figure 2.10: a) Experimental STDP data from biological samples; b) Ideal STDP learning function; c) Ideal STDP inhibitory function (reused with permission from Ref. [20]).

2.3 Artificial neural networks

Having a theoretical model for neural potentiation and depression, which has a high degree of experimental verification, a natural follow-up is to try and implement some sort of artificial synapse that sim-

ulates a real one, and then if possible to assemble a large number of such synapses in an artificial neural network that can perform higher-level functions, eventually even working as complete regions of the brain.

Artificial synapses are usually non-linear circuits that connect a source terminal, representing the pre neuron, to a sink, equivalent to the post neuron. The source will emit an electric pulse, resembling that of a biological neuron, which the artificial synapse will modify according to the rules of the model, and pass it to the sink. Traditionally, these source-circuit-sink structures are designed and integrated directly in silicon, in specialized hardware. However, the sheer complexity of a biological neural network imposes a number of strict constraints in the circuits: they must occupy the smallest possible silicon area for successful integration and must use as few components (transistors) as possible, for cost, space and power efficiency reasons. This means that, for reasonably complex networks, these requirements quickly become impractical for conventional implementations.

Fortunately, the memristor is an ideal candidate to replace traditional, CMOS-compatible implementations of artificial synapses [20]. It naturally exhibits a non-linear resistance that changes according to the history of previous inputs, affecting how effectively a signal is transmitted through it, exactly the sort of behavior we see in a biological synapse. It is also a passive electric component, which does not require a power supply, unlike conventional silicon synapses, and has a simple physical structure and hence a big potential for miniaturization, making very compact, complex and scalable networks possible.

2.3.1 Memristor integration in artificial synapses

The first experimental implementation of the STDP model using a memristor with a silver-silicon mixture layer was done by Jo *et al.* [23], in a hybrid CMOS-neurons/memristor-synapse crossbar configuration, sketched in Fig. 2.11.

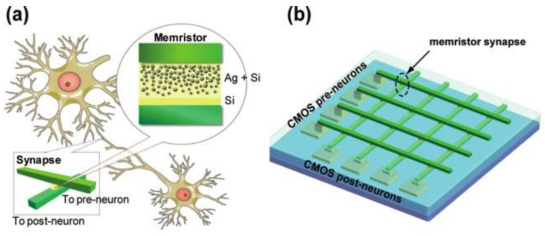


Figure 2.11: a) Cross-section of Si-Ag/Si memristor structure; b) Configuration of a crossbar array, with memristor synapses at each cross-point (reprinted with permission from Ref. [23]. Copyright 2010 American Chemical Society).

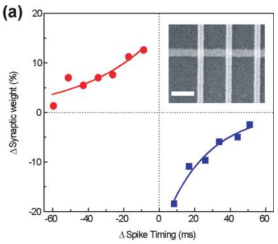


Figure 2.12: Experimental data and fit to STDP model of variation of the synaptic weight with time; inset - SEM image of crossbar array (reprinted with permission from Ref. [23]. Copyright 2010 American Chemical Society).

The transistor logic in the neurons serves to locally control the amplitude and the shape of the neural spikes, since it is possible to optimize the synaptic response by trying different pulse widths and timings. As usual, the pre neuron firing first induces a potentiation of the synapse, while depression occurs for the opposite case, and we see in Fig. 2.12 that this artificial synapse array reproduces successfully the two hallmarks of the STDP model: it shows both potentiation and depression capabilites (the branches

appear inverted because the authors define ΔT as the symmetric of Eq. 2.10) and the effect is stronger the closer together the two pulses are. We can see that this data is in agreement with the measured values from biological samples in Fig. 2.10 a), proving that memristors are indeed suited for emulation of real synapses and neural networks.

Another aspect of human memory memristors are suited to replicate, besides LTP and LTD, which are long-term memory (LTM) phenomena, is short-term memory (STM). In this sort of process, memory only gets stored for a short amount of time before the synaptic strength spontaneously decays and forgetting takes place [24]. Thus, a memory can only be kept through repeated stimulation of the synapse; however, as seen in Fig. 2.13, an STM to LTM transition can be performed if the repetition rate of the stimulus is such that complete decay in the STM region does not take place, and we can then enter the persistent memory zone, where the decay still happens but is much slower. To show this is the case, in Fig. 2.14 we can see the conductance (equivalent of the synaptic weight) of a silver sulfide atomic switch for different repetition rates: for a period T = 20 s we see that STM is taking place, as the weight is unable to stay at the persistence threshold of 77.5 µS, while increasing the rate to T = 2 s stops the complete decay of the signal and the continuous reinforcement eventually enters the LTM zone.

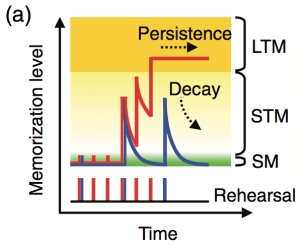


Figure 2.13: Short-term and long-term memory dependence on the repetition rate (reused with permission from Ref. [24]).

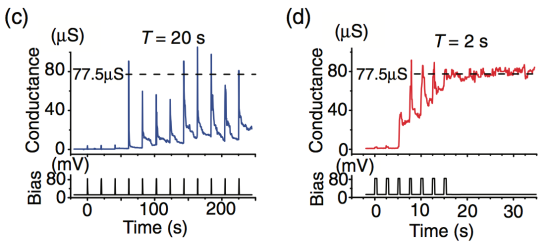


Figure 2.14: Experimental data for the conductance of a Ag_2S film for two different repetition periods - c): 20 s; d): 2 s (reused with permission from Ref. [24]).

2.4 Microfabrication and state of the art

The materials involved in the building of MIM structures are relatively common and simple, and the microfabrication of such devices is comprised of two main steps: lithography and deposition/etching. Starting with an inert substrate, like silicon, glass or an organic polymer, the successive metal-oxide-metal layers can be deposited on top of each other using a variety of thin-film deposition methods, such as physical or chemical vapor deposition (PVD/CVD), and corresponding specialized techniques. Afterwards they are patterned in the desired shape using photolithography processes and deposition and/or etching steps; these correspond, respectively, to the addition or removal of material. The specific microfabrication methods and equipment used in this work are described in detail in Chapter 3.

Regarding practical applications in the fabrication of memristive devices using the techniques described above we now present a few examples.

Mai *et al.* [25] report the memristive behavior of lithium-cobalt based MIM cells, with a bottom doped

silicon electrode, a variable-size gold top electrode and a Li_xCoO_2 interlayer, a common material in rechargeable lithium batteries. This device was built by depositing 100 nm-thick Li_xCoO_2 films in p-doped silicon using a reactive sputtering technique in an RF magnetron, with the sputtering gas an argon-oxygen mixture.

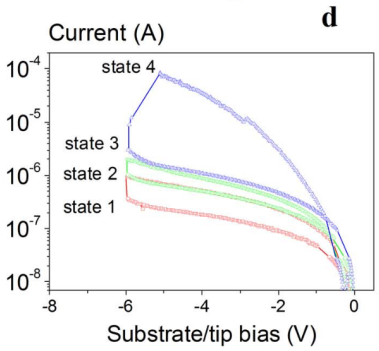


Figure 2.15: I(V) characteristic of lithium-cobalt MIM cell for four different resistance states (reused with permission from Ref. [25]).

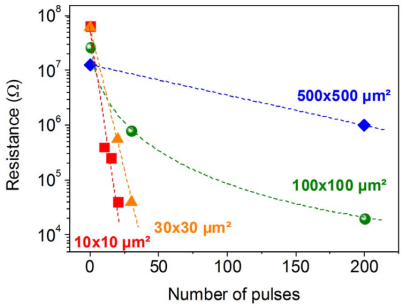


Figure 2.16: Change in resistivity of MIM cell with number of voltage pulses, for four different top electrode areas (reused with permission from Ref. [25]).

As seen in Fig. 2.15, this cell presents the already familiar pinched-hysteretic current-voltage characteristic typical of memristive systems, in four different resistance states (only negative voltage sweeps were performed), and as we saw earlier, these can be translated to changes in the weight of artificial synapses in neural networks. Another staple of memristance is the variation of the resistance with the number of applied voltage pulses. Fig. 2.16 shows that the general trend is a decrease in resistance with a larger number of pulses, and this decline is much sharper for smaller top electrode areas. This probably has to do with the microscopic phenomena and the reaction kinetics that occur in the interelectrode layer that enable resistance switching in these devices.

To attest the truly versatile nature and potential of memristive arrays, we present the example of Kim *et al.* [26], who developed a RRAM array, using a one transistor-one memristor crossbar architecture, in a flexible plastic substrate. In this chip, an Al/TiO_2/Al resistive switching structure was fabricated using plasma-enhanced ALD, similar to the work discussed eariler, with an interelectrode layer thickness of only 14 nm, and placed in the drain terminal of a flexible MOSFET. A grid of 8 by 8 such devices were then connected in a classic crossbar architecture using word, bit and source lines. A schematic of a RRAM cell is depicted in Fig. 2.17, an image of the fabricated cell in Fig. 2.19, and the complete array, demonstrating its flexibility, in Fig. 2.20.

As we can see in Fig. 2.18a, the two resistive states of the memristor are clearly separated, with the drain current I_D almost zero in the HRS and around 20 µA for a gate voltage V_G = 5 V. This, combined with the high retention times of the bits stored in the cells, as shown in Fig. 2.18b, show that this device is suited to use in a non-volatile memory. It was also reported in this work that the change in the resistance difference $R_{HRS} - R_{LRS}$ with the bending radius and the number of times it suffered a bend is very small, proving this flexible implementation with a great potential for compactification can still work in a wide range of different situations and environments, a big advantage over conventional electronic

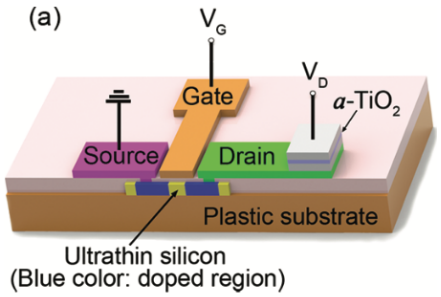
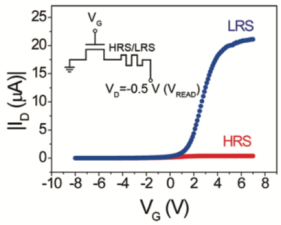
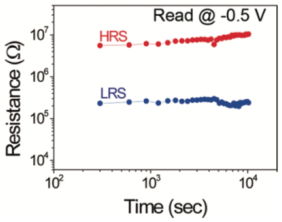


Figure 2.17: Schematic of a 1T-1M memory cell (reprinted with permission from Ref. [26]. Copyright 2011 American Chemical Society).



(a) Drain current against gate voltage in the transistor.



(b) Retention time of cell state.

Figure 2.18: Electric properties of 1T-1M cell, for both resistive states (reprinted with permission from Ref. [26]. Copyright 2011 American Chemical Society).

components.

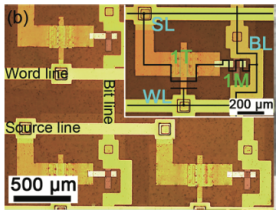


Figure 2.19: Optical microscope image detail of RRAM array; inset - circuit diagram of 1T-1M pair (reprinted with permission from Ref. [26]. Copyright 2011 American Chemical Society).

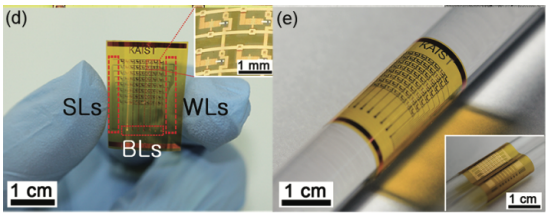


Figure 2.20: Complete RRAM array, unflexed and flexed around a tube of diameter d = 5 mm (reprinted with permission from Ref. [26]. Copyright 2011 American Chemical Society).

At a material optimization level, Huang *et al.* [27] have established the non-polar resistive switching nature of an electroforming-free Pt/MgO/Pt memristive cell. The 60 nm thick oxide has been deposited by ion beam deposition, which the authors propose might introduce a relatively high density of defects in the insulating matrix; this translates to measurements in which the initial resistance of the device and the voltage threshold of the first Set transition are nearly the same as those of subsequent transitions.

As seen in Fig. 2.21, all possible voltage polarity combinations for the Set and Reset transitions yield clearly separated HRS and LRS, with an R_{OFF}/R_{ON} ratio of around 10^4. X-ray photoelectron spectroscopy studies of the structures also seem to point to metallic Mg as the main component in the conducting filaments in this stack.

A work with a similar film stack, done by Chiu *et al.* [28], where the 60 nm MgO film was deposited by RF magnetron sputtering, focused on the conduction mechanisms in both HRS and LRS states.

The authors found that, for an applied electric field larger than 250 kV/cm the main conduction mechanism in the high-resistance state is hopping conduction, in which the current density J has an exponential dependence on the electric field E (correspondingly, the current has the same dependence on the applied voltage). The signature of this conduction mechanism is then a linear progression of the experimental points when plotted in a E vs log J graph, which can be confirmed in Fig. 2.22. The conduction in the LRS, on the other hand, was found to be Ohmic, as expected.

In accordance with the requirements of resistive states stability, separation and unipolar operation of memristive cells for memory applications, Guerra *et al.* [29] have demonstrated such properties in a Pt

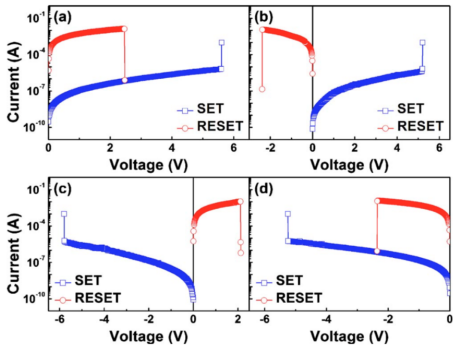


Figure 2.21: Pt/MgO/Pt thin film resistive switching for all four polarity combinations of Set and Reset events (reused with permission from Ref. [27]).

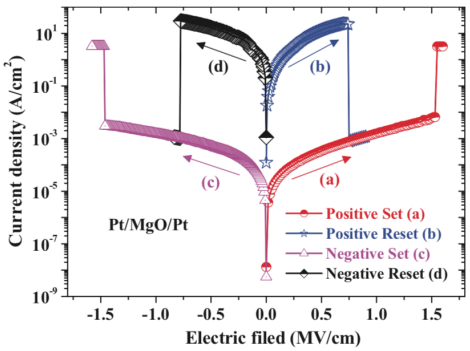


Figure 2.22: E vs log J plot of positive and negative Set and Reset transitions of a Pt/MgO/Pt memristive cell (reused with permission from Ref. [28]).

150/ MgO 15/ Ta 20/ Ru 5 thin film stack (values in nm). This MIM structure presents an average Set voltage of $\sim$1.61 V and a Reset voltage of $\sim$1.38 V, as well as an average R_{OFF}/R_{ON} ratio of $\sim$ 7, over 42 switching cycles. The cells have also demonstrated a retention of both resistive states for 10^4 s.

In a last example, Dias *et al.* [30] undertook a comprehensive study of the Set and Reset voltage and current variability using the four possible polarity combinations. Using a Pt 150/ MgO 30/ Ta 20/ Ru 5 structure (values in nm), the authors found that, after 50 Set-Reset cycles, the Set and Reset voltages variability is lower when the Set is performed with positive bias. In particular, the Set and Reset voltages are lowest when performing Set $+$, Reset $-$ cycling. A lower variability of the OFF state resistance is also lowest in the $(+,-)$ mode, where the average R_{OFF}/R_{ON} ratio is around 33. These trends can be visualized in Fig. 2.23.

The conduction mechanisms in the HRS and LRS have also been studied, and found to be Ohmic in the LRS, as expected, and space-charge-limited conduction (SCLC) in the HRS. This is in contrast with the findings of Chiu *et al.* [28].

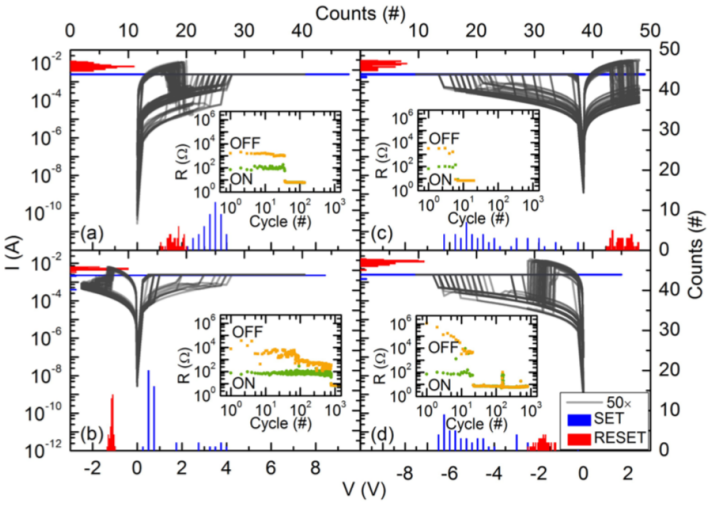


Figure 2.23: I-V curves, distributions of threshold voltages and resistance values over 50 switching cycles for four Set-Reset polarity combinations, clockwise from top left: $(+,+)$, $(-,+)$, $(-,-)$ and $(+,-)$ (reused with permission from Ref. [30]).

Chapter 3

Device fabrication

3.1 Equipment and techniques

3.1.1 Nordiko 2000 (magnetron sputtering)

The Nordiko 2000 is an ion sputtering system designed to deposit high-quality thin films using a 13.56 MHz radio-frequency (RF) magnetron. It has 6 different targets with a number of metallic and insulator materials available, and can deposit with good uniformity up to 2-inch wafers. The sample is placed on a copper holder and inside a loadlock, which is pumped and vented independently of the main chamber. After pumping and reaching the loadlock base pressure ($\sim 10^{-6}$ Torr), a robotic arm places the holder in one of 12 stations inside the chamber, where deposition occurs.

In this physical process, a plasma is produced from an inert gas, usually argon, and a magnetron confines it in the region surrounding the target. Here, highly energetic ions from the plasma collide with the target and eject material toward the substrate.

Figure 3.1: Nordiko 2000.

3.1.2 Nordiko 3000/3600 (ion beam deposition and milling)

The Nordiko 3000 and 3600 are ion beam systems, capable of doing both deposition and etching (ion milling) in the same chamber. Both feature six targets, a deposition gun, an assist gun, used primarily for etching, and a cassette system, allowing automatic multiple wafer processing. The N3000 system accepts a batch of up to eight 6-inch wafers, while N3600 can process up to twelve 8-inch wafers in sequence.

In contrast with magnetron sputtering, in ion beam processes the plasma is not generated in the vicinity of the target or substrate, but rather in separate vacuum chambers. An RF antenna produces plasma from an inert gas (Xe for deposition and Ar for milling), which is then collimated and accelerated into the main chamber by a series of voltage-biased grids. The beam will then strike the target and eject material toward the substrate, in deposition processes, or hit the substrate directly to etch its surface in a non-selective manner.

In Nordiko 3600, the assist gun has a 10º deviation from the horizontal direction, so the substrate pan angles θ used in this machine correspond to a real etch angle of θ + 10º.

Etch angle The angle at which the plasma beam from the assist gun hits the sample surface has a critical impact in a variety of properties of the patterned structure, such as the etch rate of the films, the shape of the structure, whether there is redeposition of material back into the structure sidewalls, among others [31, 32, 33]; the latter two are of particular importance to the memristor fabrication process. It has been experimentally determined at INESC-MN that an etch angle of 70º is a good compromise between vertical walls in the structure and the mitigation of trenching features, while a 40º etch angle is good to avoid redeposition and to keep the sidewalls clean [34], so that these values will be used throughout this work.

3.1.3 Nordiko 7000 (multi-process system)

The Nordiko 7000 is comprised of four modules (vacuum chambers), each one dedicated to a specific process step, and a loadlock equipped with a specially modified 1-wafer cassette; all of these are connected to a central dealer chamber, where the wafer is distributed in sequence to the modules.

This system is typically used in the final fabrication stage, to perform the metallization of the sample contacts. This sequence consists of the following steps: a brief 60 second etch in module 2, to remove any oxides and contaminants present in the sample surface and to enhance the adhesion of the contact layer, deposition of the contact material, a 3000 Å thick aluminium-silicon-copper (AlSiCu) alloy by DC sputtering, in module 4, and deposition of a TiW(N) passivation layer in module 3. Module 1 can perform flash annealing of samples, but is seldom used in this machine.

3.1.4 Alcatel SCM 450 (magnetron sputtering)

This is a magnetron sputtering machine featuring 3 targets and 4 sample stations, used in this work for the deposition of SiO_2 insulating films. It features only a single vacuum chamber, with no loadlock,

meaning that each sample must be mounted on the holders by hand and the chamber must be vented and pumped between each batch, so that long pumping times ($\sim$12 h) are necessary to reach the system base pressure of 10^{-7} Torr.

3.1.5 LAM Rainbow 4520 (reactive-ion etching)

This system consists of a vacuum chamber and loading and unloading loadlocks, with a wafer transport system capable of processing batches of 6-inch wafers. Inside the chamber, the sample holder is connected to an RF electrode to generate plasma (the wafer area pressure is around 300 mTorr).

This machine etches samples by reactive-ion etching (RIE): this process relies on chemical reactions between low-energy plasma ions and the material to be removed. This means that instead of producing plasma from an inert gas, a chemically active gas with suitable reaction pathways is used, making RIE a highly selective technique. To etch SiO_2 a tetrafluoromethane (CF_4) plasma is used [35].

3.1.6 Raith-150 E-beam system (SEM observation)

The Raith-150 system is an electron-beam lithography tool that features a thermionic field emission filament, allowing the high resolution pattern definition on large-area wafers, at a nominal resolution of 20 nm. A LEO 1500 scanning electron microscope (SEM) is also incorporated in the equipment.

In this type of imaging a highly focused beam of energetic electrons hits a substrate. The most important interaction effect is secondary electron emission: inelastic scattering causes the transfer of energy from the beam electrons to the atoms in the material. These become excited and eject low energy electrons from an inner shell, which are detected by one or more scintillator detectors.

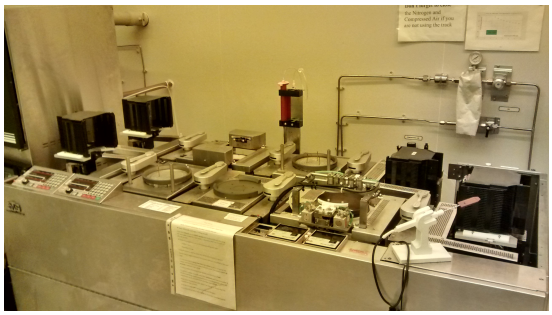
The number and energy of ejected secondary electrons that reach the detectors depend strongly on the type of films present in the sample, as well as the surface topography. Thus, very high depths of field can be achieved, yielding images with clear three-dimensional features. This makes SEM a very useful technique to inspect the shape and size of micro and submicrometric structures.

The lithography capabilities of the equipment were not used in this work; only SEM observations were performed.

3.1.7 Lithography

The lithograhy processes used throughout this work can be described by three main steps, as well as an optional sample preparation step. A brief summary of each stage is presented below:

Vapor Prime (optional) In order to improve the adhesion of the photoresist compound at the surface, the sample can be treated with hexamethyldisilazane (HMDS), an organosilicon compound. It is typically applied by placing the sample in a heated oven subject to a mild vacuum, at a temperature of 130 ^{o}C, and pumping it with gaseous HMDS for 5 minutes. Since usually there are no issues with photoresist adherence with the materials we are using, this step can be skipped without detrimental effects.



(a) SVG automatic track. Foreground: track 1, developer. Background: track 2, coater.

(b) Heidelberg DWL 2.0 direct-write laser.

Figure 3.2: Lithography equipment: coating and development tracks and direct-write laser.

Coating After the vapor priming, the sample is mounted on a 6-inch holder wafer and coated with photoresist (PR) in a spin-coater, using a programmed speed of 2500 rpm to achieve a resist thickness of 1.45 µm (SVG track 2, depicted in Fig. 3.2a). A positive photoresist, PFR7790G27cP, was used throughout this work. This type of PR is initially insoluble, and becomes soluble after the exposure. After coating, the sample is baked for 60 seconds at 85 °C to evaporate the remaining solvents and consolidate the resist profile.

Exposure The coated sample is exposed in a Heidelberg DWL 2.0 direct-write laser, shown in Fig. 3.2b. This equipment features a λ = 440 nm diode laser to directly expose up to 6-inch wafers. The areas to be exposed are defined in a `.dxf` mask file, created with AutoCAD software. The minimum feature size is 0.8 µm. For multi-layer lithographic processes, as is the case in this work, the sample stage can be aligned to a precision of 0.1 µm, using control software with two zoom levels for coarse and fine alignment and automatic alignment cross recognition and centering.

Development After exposure, the sample is baked for 60 seconds at 110 °C (track 1 in Fig. 3.2a), to finish the chemical reactions started by the laser light and to eliminate standing wave profiles in the resist wall. After this treatment, the sample is sprayed with water to clean the surface and covered in developer solution for 60 seconds, to dissolve the resist in the exposed areas. The standard development time can be modified in order to fully clean remaining resist artifacts and to obtained the desired structure features.

3.1.8 Liftoff residues and mitigation

A typical side-effect of liftoff processes is shown in Fig. 3.3: when the photoresist has a sloped profile, tapering upwards, the deposited material will follow that profile and have sloped sidewalls as well. Upon liftoff, these sidewalls might not be fully removed, thus leaving an undesirable upwards protrusion in the sample surface topography. The presence of these structures are critical in the ensuing fabrication steps.

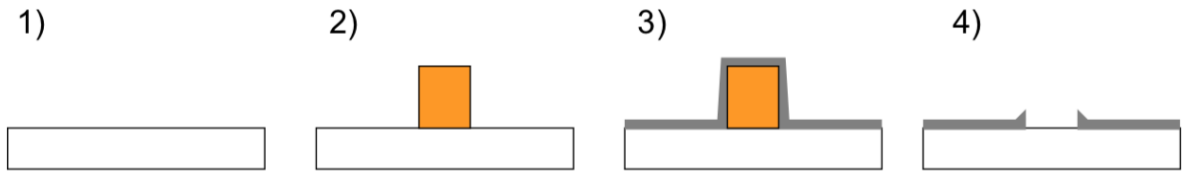


Figure 3.3: Schematic of the formation of liftoff “ears” (taken from Ref. [36])

The usual method to avoid the formation of such structures is to perform a predevelopment stage in the lithography step: after spin-coating with photoresist and before exposing in the laser, the sample is developed for a short time, typically 15 to 20 seconds [37]. This results in a more vertical or undercut profile, with less sputtered material deposited along the sidewall, so that the liftoff procedure becomes considerably faster. The residues, if formed, become more fragile and easier to break and remove from the sample surface.

3.1.9 Platinum redeposition and mitigation

A critical issue in previous iterations of the fabrication process is the redeposition of platinum from the bottom electrode on the pillar sidewalls, in the junction definition step. This phenomenon leads to short-circuits across the junction and thus to non-functioning devices.

A first step towards mitigation of this problem was to define the pillar in Nordiko 3600 by etching the top electrode materials at 60º pan angle (70º true angle) and the MgO film at 30º pan angle (40º true angle), with a 30 Å overetch to the bottom electrode layer. The latter will decrease redeposition phenomena, as discussed in Section 3.1.2. However, this combination did not yield satisfactory results as many devices were still found to be shorted across the electrodes (results not shown).

As such, a further optimization was performed. An MgO 300/ Ta 200/ Ru 50 (values in Å) stack was deposited in three Si/SiO_2/ Ti 250/ Pt 1500 1$\times$1 sq inch substrates, labeled A, B and C, in Nordiko 2000. In each of those, four samples were prepared with a single lithography step with a 16$\times$16 array of 200$\times$200 µm^2 square pillars, yielding a total of 12 0.5$\times$0.5 sq inch samples. In each sample a different etching recipe was tested, using pan angles of only 60º, only 30º or a combination of both. Control recipes and different amounts of overetching were also used. These, as well as the measured etch thicknesses and the stack thickness of each substrate are compiled in Table 3.1.

We can observe that the etched thickness was smaller than expected for all tested samples, more so for 30º-only samples. This means that checking for electric contact between the top of the patterned pillars and the die frame, which would identify short-circuits, may not yield significant results since the platinum layer is not yet exposed and MgO remains in the regions between pillars.

The reason for this very significant discrepancy between the expected and measured etched thickness is unknown. One possible cause is assist gun neutralizer malfunction in Nordiko 3600. Such an issue leads to charge accumulation in the sample once the top electrode films are removed and the insulating MgO is reached. This leads to a drastic reduction in the etch rate and etch uniformity issues. Regardless of the cause, this study yielded inconclusive results as to the mitigation of short-circuits

caused by redeposition of platinum.

It was later found empirically that increasing the ruthenium thickness in the stack from 50 Å to 200 Å, as well as etching the top electrode and most of the MgO film (around 70%) at a 60º, and the rest of the MgO (30%) and a 30 Å overetch at 30º resulted in no apparent short-circuits in test structures. These are round pillars of 100 µm, 200 µm and 300 µm, patterned in the same manner as described above. The effects for smaller junction areas remain untested, however.

Sample	Etch recipe		$t_{nominal}$ (Å)	t_{meas} (Å)	Substrate	t_{stack} (Å)
1	60º 30º	Top 100 % MgO + 10% overetch	580	407 ± 29	C	545 ± 36
2	60º	Top + 50% MgO (no Pt exposed)	400	336 ± 38		
3	60º	Top + 100% MgO + 10% overetch	580	475 ± 36		
4	30º	Top + 100% MgO + 10% overetch	580	208 ± 42		
5	30º	Top + 100% MgO + 20% overetch	610	222 ± 7	B	539 ± 32
6	30º	Top + 100% MgO + 30% overetch	640	306 ± 17		
7	30º	Top + 100% MgO + 40% overetch	670	255 ± 24		
8	60º 30º	Top + 50% MgO 50 % MgO + 10% overetch	580	363 ± 42		
9	60º 30º	Top + 70% MgO 30% MgO + 10% overetch	580	434 ± 13	A	539 ± 56
10	60º 30º	Top + 90% MgO 10 % MgO + 10% overetch	580	379 ± 35		
11	60º 30º	Top + 70% MgO 30 % MgO + 20% overetch	610	504 ± 27		
12	60º 30º	Top + 90% MgO 10 % MgO + 20% overetch	610	526 ± 37		

Table 3.1: Etch pan angle optimization using only 60º, only 30º and combinations of the two.

3.2 Material characterization

Thin films of tantalum (Ta), ruthenium (Ru) and magnesium oxide (MgO) were deposited on the N2000 system with a nominal thickness of 300 Å, and additionally for MgO, a thickness of 150 Å. The substrates used were silicon deposited with 2500 Å of alumina - Si/Al_2O_3 (since silicon is a semiconductor an insulating layer must be deposited on top to avoid current flow through the substrate) and Corning Eagle

XG borosilicate glass, both with a 1×1 square inch area. Specifically for MgO in glass substrate, for both thicknesses, additional depositions were performed in station 1, in order to check for changes in the crystalline structure caused by the external magnetic field, using X-ray diffraction analysis.

3.2.1 Thickness

The thickness of the thin films deposited on the Nordiko 2000 were measured in a Dektak 3030ST profilometer, a surface texture analysis equipment. It consists of a diamond stylus connected to a piezoresistive sensor which records changes in its height. Several operation parameters can be defined, namely the scan length, stage speed, resolution and contact force. During operation, the probe rests on the sample surface while the sample stage moves in one direction, so that changes in the surface topography will move the probe up and down; the sensor will then read a signal proportional to the probe height change.

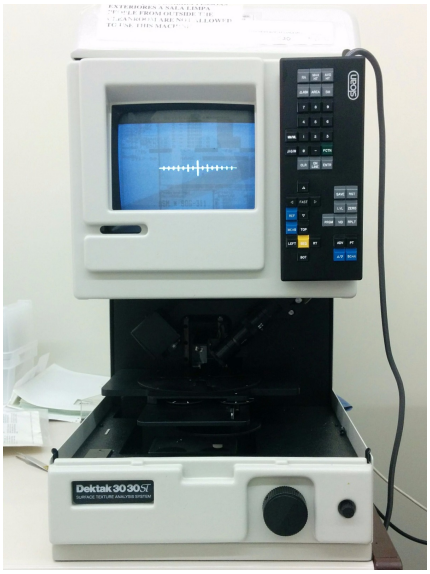


Figure 3.4: Dektak 3030ST profilometer.

A set of 8 measurements were performed in each sample, 4 on the ascending and 4 on the descending slope, taking the average thickness value and calculating the error as the corrected sample standard deviation:

$$\bar{t} = \frac{1}{N}\sum_{i=1}^{N} t_i \qquad \sigma_{\bar{t}} = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(t_i - \bar{t})^2} \tag{3.1}$$

The results obtained are present in Table 3.2:

3.2.2 Resistivity

The resistivity of a material is a property that measures how much it restricts the flow of electric current. This quantity, along with the geometric characteristics of the material, determine its overall electric

Substrate	MgO 150	MgO 300	Ru 300	Ta 300	MgO 150 (Mag)	MgO 300 (Mag)
Si	140 ± 33	313 ± 80	293 ± 48	337 ± 34	-	-
Glass	n.a.	311 ± 18	300 ± 35	319 ± 32	n.a.	325 ± 39

Table 3.2: Thickness of thin films sputtered in Si/Al_2O_3 and glass substrates (all units in Å). For MgO 150 Å in glass, the thickness was too small to accurately measure in the profilometer; no values are presented.

resistance. Assuming a uniform cross section, the resistivity is given by:

$$\rho = R\,\frac{A}{l} \tag{3.2}$$

where R is the resistance, $A = w \times t$ is the area of the cross-section and l, w, t are the length, width and thickness of the material, respectively.

In order to measure the Ru 300 Å and Ta 300 Å thin film resistivity values, glass stripes were placed in the holder during deposition. After deposition, the resistances of the metal films were calculated by applying several current values at the surface of the film and measuring the voltage difference across a known distance. By fitting these points to a linear function $y = ax + b$ (shown in Fig. 3.5), the resistance can be extracted.

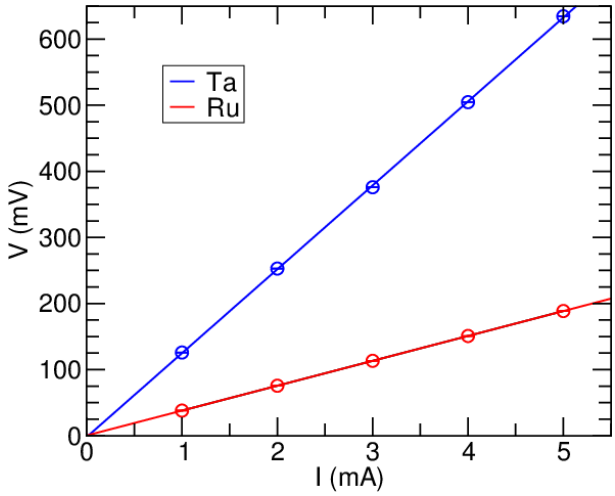


Figure 3.5: Fit of $I - V$ experimental points for Ta and Ru thin films in glass substrate (nominal thickness 300 Å)

The resistance values obtained were: R_{Ru} = 37.649 $\pm$ 0.0032 Ω and R_{Ta} = 126.93 $\pm$ 0.0032 Ω. [1]

The voltage measurements were done using a four-probe setup built at INESC-MN, using a Keithley 220 programmable current source and a Keithley 182 sensitive digital voltmeter.

The geometric parameters necessary for the calculation of the resistivity, namely the width of the glass stripes w_{Ru} and w_{Ta}, as well as the distance between the inner probes l_{probes}, were determined using a Vernier caliper. These parameters, as well as the relevant thicknesses from Table 3.2 and the calculated resistivity values are shown in Table 3.3:

[1] These values and respective errors were obtained with the least-squares fitting algorithm, using the *fitteia* software package, avaliable at `http://fitteia.org`.

Parameters	Ru	Ta
l_{probes} (cm)	0.7205 ± 0.0005	
t (cm)	$(3.00 \pm 0.35)\times10^{-6}$	$(3.19 \pm 0.32)\times10^{-6}$
w (cm)	0.312 ± 0.0005	0.311 ± 0.0005
R (Ω)	37.649 ± 0.0032	126.93 ± 0.0032
ρ ($\mu\Omega$·cm)	48.9 ± 5.8	174.8 ± 17.9

Table 3.3: Geometric parameters, resistance and resistivity of Ru and Ta thin films. The uncertainties in ρ_{Ru} and ρ_{Ta} were calculated using standard error propagation.

The resistivities obtained for the Ru and Ta thin films are in line with the values reported in the literature at similar thicknesses [38, 39], which is an indicator of the good quality of the sputtered films and that their electric characteristics are as expected, so they can be used in the complete memristor process.

3.2.3 MgO etch rate calibration

In order to achieve accurate patterning of the structures in the complete fabrication process it is necessary to know the etch rates of all materials in which this technique was used. Since the values for MgO ion beam etching for the relevant pan angles of 60º and 30º in Nordiko 3600 were not available at the start of this work, they were calculated using two different methods.

Standard method

A thick ($\sim$ 1000 Å) MgO film is deposited on a 1$\times$1 sq inch glass substrate using Nordiko 2000. Afterwards, the entire surface of the sample, except a small strip around 2 mm wide, is covered with ink using a felt pen, before being etched on Nordiko 3600 for a time t_1 = 300 s at a 60º pan angle. Afterwards, the ink is removed with acetone and the sample is cleaned with IPA and DI water, before reapplying the ink and leaving a different area uncovered. The process is then repeated for etch times t_2 = 600 s and t_3 = 900 s, and again using these three times for a 30º pan angle.

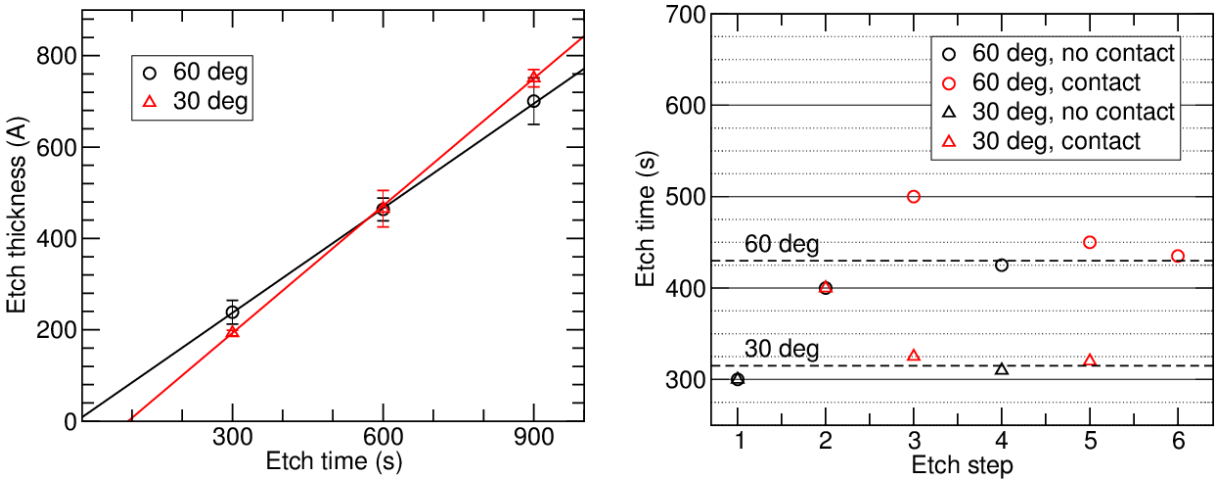
The etched thicknesses are measured on the profilometer and each set of points for a particular pan angle is fitted to a linear function, identical to the one used for the Ta and Ru resistivity measurements, which yields the etch rate. The results are shown in Fig. 3.6a.

Iterative method

An MgO film with nominal thickness of 300 Å is deposited on a 1$\times$1 sq inch Si/SiO_2/ Ti 250/ Pt 1500 substrate in Nordiko 2000, with a deposited thickness of $\bar{t}_{dep\ MgO}$ = 306 $\pm$ 23 Å measured on the profilometer. Covering the surface using the same method as described previously, the sample is etched in steps and electric conductivity is checked in between with a multimeter: if electric contact is established by placing the two probes in the exposed area, the MgO film is fully removed and the etching has reached the Pt layer, a conducting material; if not, there is still MgO present.

Starting with an etch time t_1 = 300 s, the cumulative time is increased in steps of Δt_1 = 100 s until contact is achieved and the process is stopped. The last cumulative time where contact was not registered, and so where MgO is still present in the exposed area, is denominated t_2; this means that the sample must be etched for a time between t_2 and t_2 + 100 s to fully remove the MgO film.

The sample is cleaned and the ink is reapplied, exposing a new region. The second iteration of the process will refine the upper and lower bounds of the etch time. The initial time step in the new region will be t_2 + 25 s, incrementing in Δt_2 = 25 s steps until contact is measured. The last cumulative etch time without contact is now t_3. Finally, the process is repeated, starting at t_3 + 10 s and using Δt_3 = 10 s steps. The results for both pan angles are shown in Fig. 3.6b.



(a) Standard process.

(b) Iterative process.

Figure 3.6: MgO etch rate calibration using two different methods.

The etch rates calculated from the fits in Fig. 3.6a were $r_{MgO,\,60^o}$ = 0.76 $\pm$ 0.09 Å/s and $r_{MgO,\,30^o}$ = 0.93 $\pm$ 0.03 Å/s. For the 30º fit, we have a negative value at the origin, which means that a systematic error has affected the measurements for this pan angle.

In order to confirm the values obtained through this method and to eliminate measurement errors in the profilometer, the iterative method was applied, which does not depend on thickness measurements but rather on the presence or absence of electric contact in the exposed sample area. The downside with this method is that only a range of etch times can be established for each pan angle, and the uncertainty in the deposited MgO layer thickness must now be taken into account.

The nominal values for the etch time in this method were taken as midpoint between the biggest cumulative time without electric contact and the smallest cumulative time with contact (shown in Fig. 3.6b as dashed lines); these are respectively 425 s and 435 s for 60º and 310 s and 320 s for 30º. Thus, the etch times are $t_{etch,\,60^o}$ = 430 $\pm$ 5 s and $t_{etch,\,30^o}$ = 315 $\pm$ 5 s.

The etch rates are directly calculated using the expression $r_{MgO} = \frac{\bar{t}_{dep\,MgO}}{t_{etch}}$, which yields values of $r_{MgO,\,60^o}$ = 0.71 $\pm$ 0.06 Å/s and $r_{MgO,\,30^o}$ = 0.97 $\pm$ 0.09 Å/s, using standard error propagation for the uncertainties.

The results of both methods are summarized in Table 3.4.

Both methods yielded similar results, and the values in one are contained in the experimental error

Method	60º	30º
Standard	0.76 $\pm$ 0.09	0.93 $\pm$ 0.03
Iterative	0.71 $\pm$ 0.06	0.97 $\pm$ 0.09

Table 3.4: MgO etch rates determined by two different methods, for pan angles of 60º and 30º, in Nordiko 3600 (in Å/s).

of the other. Hence, we can conclude that no procedure is better than the other, and they both give accurate results to use in the complete fabrication process.

3.2.4 X-ray diffraction

Since X-rays possess a wavelength similar to the typical distance between atoms in solids (Å to tens of Å), the diffraction pattern of a material obtained with this kind of radiation can yield useful information about its internal organization [40].

Bragg's law (Eq. 3.3) states that, when a plane wave incides in a material made of a regular arrangement of atoms (a crystal), the reflected waves from two consecutive atom planes separated by a distance d will interfere constructively with each other if the extra distance traveled by the wave is a multiple of its wavelength λ; a representative diagram is depicted in Fig. 3.7.

$$n\lambda = 2\,d\sin\theta \tag{3.3}$$

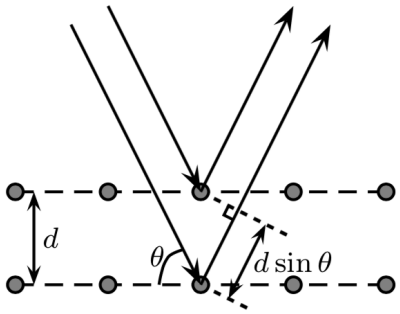


Figure 3.7: Bragg condition representation (taken from Ref. [40]).

An x-ray diffraction analysis of the films deposited on Nordiko 2000 was carried out in a Siemens D5000 diffractometer, in order to study their crystalline structure and preferential orientation of the lattice.

This equipment features a molybdenum (Mo) K_α x-ray generator, with a characteristic wavelength λ_0 = 0.70930 Å. The sample is mounted as leveled as possible in the center of the holder, in order to get accurate readings and to maximize the intensity of the reflected wave. During operation, the emitter tube (left arm) and the detector (right arm) move synchronously, so that the corresponding angles relative to the sample surface increase and decrease, respectively, by the same amount; the variable of interest is thus the full angle 2θ. The acquisition conditions were identical for all tests and are summarized in Table 3.5.

Parameters	
Tube voltage (kV)	40
Tube current (mA)	20
2θ range (º)	15-21
2θ step (º)	0.02
Acqusition time per step (s)	3

Table 3.5: Acquisiton conditions for x-ray diffraction of MgO, Ta and Ru thin films in Siemens D5000 diffractometer.

The diffraction spectra obtained for the MgO, Ru and Ta thin films are presented in Figs. 3.8a through 3.8e.

For the considered 2θ range, only one peak was present in each main spectrum. This happens because thin films, unlike bulk materials, have a high degree of anisotropy and are thus highly textured, displaying a strongly preferred orientation.

All peaks in the main spectra fitted better to a Lorentzian versus a Gaussian profile (comparison not shown), so this lineshape (defined in Eq. 3.4) was used to extract the values of the peak centroid, $2\theta_0$, and full-width at half maximum (FWHM), given by w. The value of χ^2 per degree of freedom is also presented, as a goodness-of-fit measure. The obtained values are presented in Table 3.6.

A larger sweep, from 15º to 45º, was also performed for the MgO 300 Å on Si/Al_2O_3, Ta 300 Å on glass and Ru 300 Å with Ta buffer on glass (seen in the insets in Figs. 3.8a-3.8e), to see whether the peaks obtained in the main spectra were indeed the preferential orientation of the films. The Ta film revealed a secondary peak at $\sim$ 31º, while the Ru sample has a secondary peak at $\sim$ 39º. All of these, however, are very small in comparison with the main peaks, and so we can conclude that the peaks featured in Table 3.6 correspond to the principal orientations of the crystals. Regarding the MgO film, since the sample deposited on glass did not show any peak in the principal sweep, the large sweep was performed on the sample with Si/Al_2O_3 substrate. Comparing to the large sweep for the silicon/alumina substrate alone, the very large peak present at $\theta \approx 32$º in Fig. 3.8c is thus attributed to the crystalline materials in the substrate and not to MgO.

$$y = \frac{a}{1 + \left(\frac{2\theta_0 - 2\theta}{w/2}\right)^2} + b \tag{3.4}$$

From the peak positions $2\theta_0$, the distance between adjacent atom planes d_{exp} was calculated using Bragg's law. As a simple estimate of peak broadening effects that affect the obtained spectra, the quality factor Q is calculated as defined in Eq. 3.5.

$$Q = \frac{2\theta_0}{w} \tag{3.5}$$

The main contributing factor for broadening in a polycrystalline sample is the size of the crystallites (grains). These are subdomains of a larger crystal exhibiting a continuous lattice of atoms and a certain orientation. The size of these crystallites can be estimated in XRD analysis through the Scherrer equa-

tion (Eq. 3.6), where τ is the average crystallite size, λ the x-ray wavelength, β the FWHM of the sample broadening contribution and K a factor depending on the peak shape and crystallite geometry, among other factors.

$$\tau = K\frac{\lambda}{\beta\ \cos\theta} \tag{3.6}$$

Rough estimates of the crystallite sizes for the studied materials are displayed in Table 3.6, by considering sample and instrument broadening together (effectively taking $\beta = w$). The shape factor was considered to be K = 0.9, a standard value [41].

The measured peak position values were then compared with data from the American Mineralogist Crystal Structure Database [42], a collection of XRD data reported across a number of specialized publications. The search terms used in the database were “periclase”, “ruthenium” and “tantalum”, respectively for MgO, Ru and Ta films.

Each tabled peak corresponds to a crystal orientation with a characteristic interplanar distance, labeled d_{teor}. The peak with the closest match between d_{exp} and d_{teor} is then selected as the dominant orientation of the thin films. The calculated plane separation d_{exp}, the spacing parameter d_{teor} and Miller indices $\{hkl\}$ of the best match peaks are also summarized in Table 3.6.

Thin films	$2\theta_0$ (°)	w (°)	χ^2/df	Q	τ (Å)	d_{exp} (Å)	d_{teor} (Å)	{hkl}
MgO 150 Si	19.62	0.63	1.1	31.14	58.92	2.08	2.1055	2 0 0
MgO 150 glass		-		-	-	-		
MgO 300 Si	19.65	0.63	0.8	31.19	58.92	2.08		
MgO 300 glass		-		-	-	-		
Ta 300 Si	15.68	0.25	2.5	62.72	147.68	2.60	2.3376	1 1 0
Ta 300 glass	15.57	0.26	0.8	59.88	141.99	2.62		
Ru 300 (Ta 30 buffer) Si	19.49	0.17	33.6	114.65	218.30	2.10	2.0545	1 0 1
Ru 300 (Ta 30 buffer) glass	19.39	0.23	2.3	84.30	161.33	2.11		

Table 3.6: Fitting parameters, Q-factors, average crystallite sizes, calculated and theoretical interplanar distances and Miller indices for the peaks in the thin films XRD spectra.

For all thin films, d_{exp} is in good agreement with the tabled data. Even so, the small discrepancies observed can be attributed to a number of factors. For example, the sample might not have been perfectly leveled and centered in the diffractometer holder, resulting in a systematic shift of all peaks. The ambient conditions during measurement also affect the structural properties of the material, namely the lattice cell size and consequent planar separation. This will cause shifts in the measured spectrum in comparison with the tabled data.

Regarding the peak quality factors, they were found to be higher for Ru and Ta than for MgO, meaning that the peak broadening effects are more pronounced for the latter. This points to a smaller grain size in MgO than for the metallic films, a trend confirmed with the values obtained through the Scherrer equation.

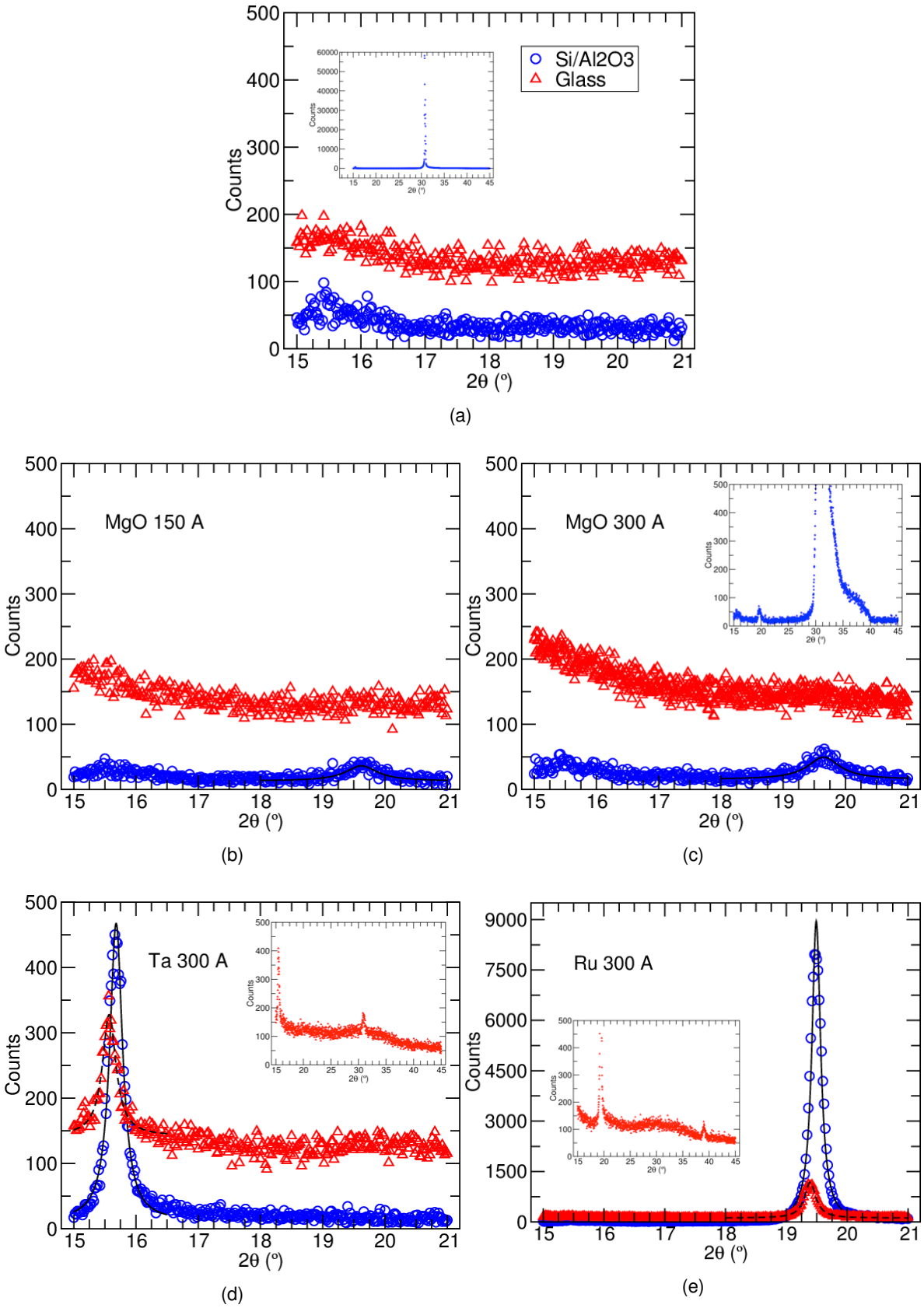


Figure 3.8: Thin film XRD spectra - a): Si/Al_2O_3 and borosilicate glass substrates; b): MgO 150 Å; c): MgO 300 Å; d): Ta 300 Å; e): Ru 300 Å (Ta 30 Å buffer); insets: 15º-45º sweeps.

3.3 Fabrication processes

The microfabrication of memristors in individual and array configurations in this experimental work was performed using two different processes, each comprised of several lithography procedures and various deposition and etching steps.

3.3.1 First process

The first process, used in samples **N3MA1** (individual devices) and **N3MA3** (crossbar arrays), is comprised of six main stages, defining in sequence the insulator junction, bottom and top electrodes, while passivating these functional structures from their surroundings with insulating material (aluminium and silicon oxides). This increases the robustness of the memristive element, better shielding against physical damage and electric interference from neighboring structures. Short-circuits between the top and bottom electrodes are also prevented.

This process is outlined in Table 3.7, and an illustration of the fabrication sequence is depicted in Fig. 3.9. A detailed step-by-step report of this process is presented afterwards. The process runsheet is available in Appendix A.1.

Step	Sketch	
0	(a)	Stack deposition
1	(b)	Junction definition and first passivation
2	(c)	Bottom electrode definition
3	(d)	First via opening to bottom pads
4	(e)	Second passivation
5		Second via opening to bottom pads
6	(f)	Top contact definition and metallization

Table 3.7: Memristor six-step fabrication process summary (**N3MA1**, **N3MA3**).

Stack deposition

The thin film stack used is the following (the numbers refer to the film thickness in Å):

Substrate	Si/SiO_2 1000
Bottom electrode	Ti 250/ Pt 1500
Junction	MgO 300
Top electrode	Ta 200/ Ru 200

The stack materials were deposited at INESC-MN: the bottom electrode material was deposited on a 6-inch wafer by ion-beam deposition in Nordiko 3000, which was then covered in photoresist to protect from physical damage and cut in 1×1 sq inch pieces in a Disco DAD 321 dicing saw. The junction and top electrode films were deposited by sputtering in Nordiko 2000.

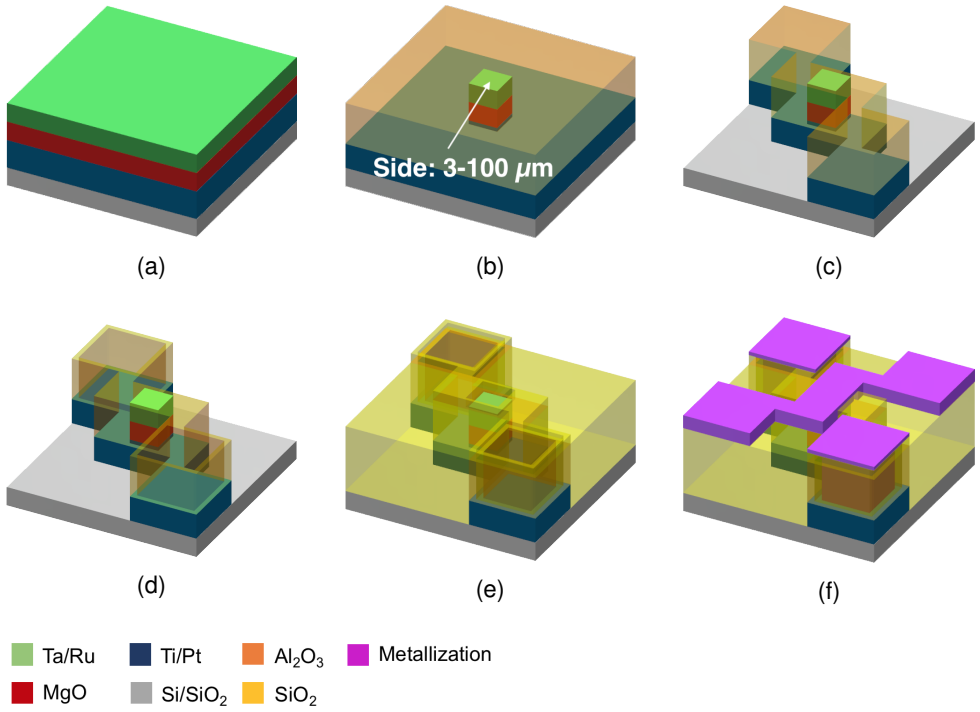


Figure 3.9: Memristor six-step fabrication process sketch.

In order to start controlling the fabrication process as early as possible, the thickness of the MgO 300/ Ta 200/ Ru 200 stack was measured using a calibration sample (S0) and a procedure similar to that described in section 3.2.1 was performed, with an obtained value of $\bar{t}_{\text{dep1}} = 697 \pm 27$ Å.

Junction pillar definition

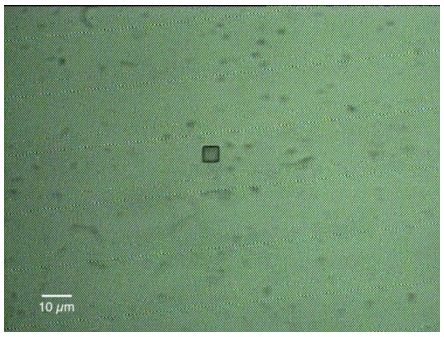
The first step of the fabrication process is the definition of the insulator junctions connecting the bottom and top electrodes. The lithography stage in this step will pattern square pillars of varying area and configuration, in two equal dies, each measuring 16.7×8 μm^2, to build both individual (sample **N3MA1**) and crossbar arrays of memristors (sample **N3MA3**), shown in Fig. 3.10.

Sample **N3MA1** features small-area junctions of 1×1 through 6×6, 8×8 and 10×10 μm^2, while large-area pillars have sizes of 20×20 through 80×80 and 100×100 μm^2.

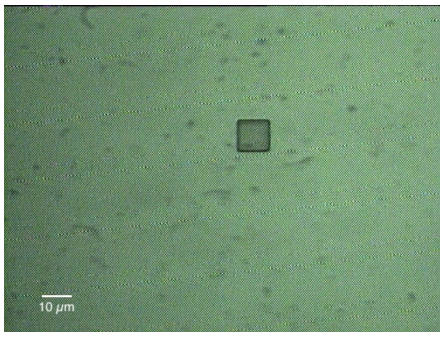
Sample **N3MA3** features small-area junctions of 3×3, 4×4, 5×5, 6×6, 8×8 and 10×10 μm^2, while large-area junctions have 20×20, 40×40, 50×50, 60×60, 80×80 and 100×100 μm^2.

After exposure, the sample is etched in Nordiko 3600, removing material and exposing the bottom electrode layer, due to a slight overetch, everywhere except directly over the pillars. Two substrate pan angles are used: 60º to etch the Ta/Ru and most of the MgO layer, in order to define the pillar walls with a nearly vertical profile, and a grazing angle of 30º for the remainder of the MgO film and a small amount of overetch into the Ti/Pt layer, which allows the minimization of redeposition of metallic material originating from the bottom layer, avoiding unwanted short-circuits bypassing the insulator. The etch conditions used are summarized in Table 3.8.

The etched thickness was measured in the profilometer, by removing with acetone a small area in



(a) 5×5 µm^2 pillar



(b) 10×10 µm^2 pillar

Figure 3.10: (**N3MA1**) Structures defined in the first lithography.

		P_f (W)	P_{ref} (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flow (sccm)	t_{etch} (s)
Set		190	0	735	105	350	0	11	
Read	60º	199.0	0	724.3	104.1	344.8	2.4	10.2	710
	30º				-				118

Table 3.8: (**N3MA1**) Operational parameters for Nordiko 3600 in the pillar definition etch. Values for the 30º pan angle etch were not taken.

the corner of the sample, covered with photoresist, which still has the full stack, and measuring the height difference to the etched area. The value obtained was $\bar{t}_{etch1} = 776 \pm 42$ Å; the experimental error interval contains the nominal value of 760 Å (700 Å of MgO/Ta/Ru layers and 60 Å overetch), indicating the etch has the correct thickness. Furthermore, to make sure the MgO is fully removed and the Pt layer is exposed, the etched die area was tested for electric contact with a hand multimeter; a resistance value in the order of dozens of ohms was registered, showing that metallic material (Pt) is indeed exposed.

After etching, an insulating layer of alumina (Al_2O_3) is deposited in UHV2, fully surrounding the pillar, to protect it and avoid short-circuits. This layer is slightly thicker than the height of the etched pillar, at a nominal thickness of 850 Å, to ensure that it is fully covered. In addition, a calibration sample (S1) of Si/SiO_2/ Ti 250/ Pt 1500 is placed alongside the sample to calibrate the deposition thickness, as well as later etching steps in the process. The deposition conditions are summarized in Table 3.9.

	P_f (W)	p (mTorr)	Ar flow (sccm)	t_{dep} (min)
Set	200	2.0	45	
Read	200	22	45.0	81

Table 3.9: (**N3MA1**) Operational parameters for the first insulating layer deposition in UHV2.

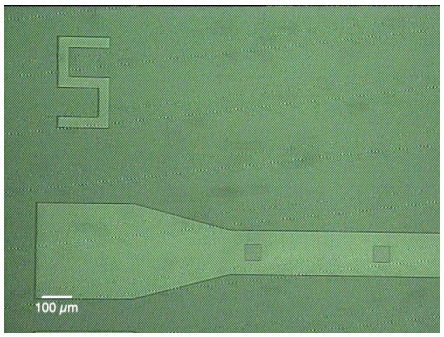
The deposited thickness was measured as being $\bar{t}_{dep2} = 466 \pm 47$ Å, nearly half of the expected value. This large discrepancy might have been caused by a very high process pressure, almost ten times the usual value. The cause was attributed to an incomplete opening of the valve connecting the turbomolecular pump and the rough pump providing the backing vacuum, which led to a deficient exhaust of the former and compromised its evacuating power.

The final step in this stage is the photoresist liftoff, to remove the Al_2O_3 directly on top of the pillars;

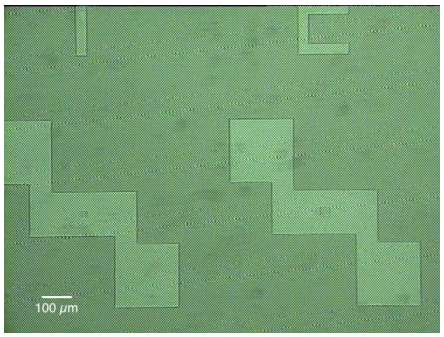
this was done by submerging the sample in pure Microstrip 3001 at a temperature of 65 °C and using ultrasounds to facilitate the removal of resist (unless noted otherwise these conditions are used for all resist strip and liftoff procedures in the course of this work), for a period of 12 hours. Inspection of the sample in the profilometer and with a 100× magnification microscope confirmed the complete removal of photoresist on top of the pillars.

Bottom electrode definition

The lithography in this stage defines the connected pads of the bottom electrode for the individual memristors and the tracks and contact pad in the crossbar arrays (shown in Fig. 3.11). In the latter case, each pillar size is available in a 4×4 grid, with 1×10 grids also defined for specific sizes.



(a) Bottom contact pads and tracks for crossbar arrays (**N3MA3**).



(b) Bottom electrode pattern for large-area individual junctions (**N3MA1**).

Figure 3.11: (**N3MA1**) Structures defined in the second lithography.

The etching in this step is performed in Nordiko 3600, at an intermediate pan angle of 45º, to remove the Al_2O_3 and Ti/Pt layers, reaching the non-conductive SiO_2 layer of the substrate and thus electrically isolating each track from its neighbours. The etch conditions are summarized in Table 3.10.

	P_f (W)	P_{ref} (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flow (sccm)	t_{etch} (s)
Set	190	0	735	105	350	0	11	
Read	199.0	2.0	724.3	104.3	344.8	2.4	10.2	2181

Table 3.10: (**N3MA1**) Operational parameters for the Nordiko 3600 in the bottom electrode etch.

The resist is then stripped from the patterned area, using the same technique as the previous step, immersing the sample for a cumulative time of 2 hours and 40 minutes.

The calibration sample S1 was etched at the same time as the sample, in order to determine the etched thickness; however, the patterned structures are large enough to be reliably measured directly on the profilometer, and as such the etched thickness was calculated as $\bar{t}_{etch2} = 2425 \pm 144$ Å. The expected nominal thickness of 2250 Å is very nearly contained in the experimental error, and the difference can be attributed to the slight deviation between the tabled and the actual etch rates of titanium, platinum and aluminium oxide in this machine.

First via opening to bottom pads

At this point, since the bottom pads are covered in thick oxide, no current can flow through the structure. As such, ion milling is used to remove the Al_2O_3 film in the areas immediately above the pads, in order to reach the Ti/Pt level.

The lithography in this step defines open 190×190 μm^2 and 280×280 μm^2 areas over the pads, in the individual devices and crossbar arrays, respectively.

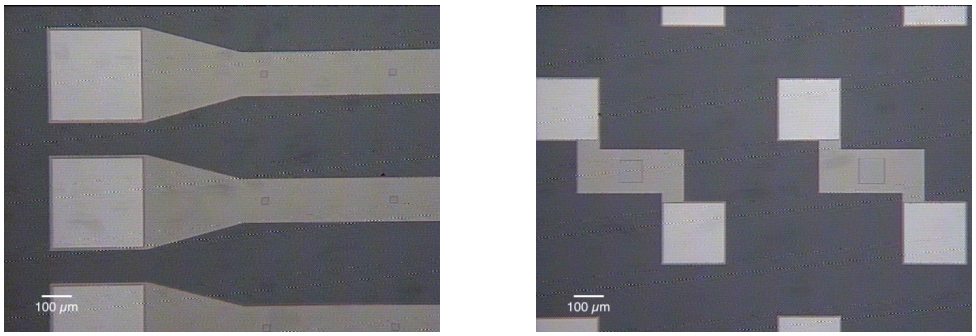
The sample is then etched on Nordiko 3600 at a 45º pan angle, with a slight overetch included to make sure that no oxide remains on top of the pads and the bottom electrode layer is reached. The etch conditions are summarized in Table 3.11.

	P_f (W)	P_{ref} (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flow (sccm)	t_{etch} (s)
Set	190	0	735	105	350	0	11	
Read	200.0	2.0	724.3	104.1	345.0	2.3	10.2	784

Table 3.11: (**N3MA1**) Operational parameters for the Nordiko 3600 in the first via opening to the bottom electrode.

Sample S1 was also used to calibrate this etching step, and a thickness of $\bar{t}_{etch3} = 558 \pm 34$ Å was measured. The nominal thickness of 520 Å ($\bar{t}_{dep2}$ + 60 Å overetch) is very similar to the experimental value, indicating the etching is complete and the Ti/Pt layer is reached. The color contrast between the exposed metal and that covered by alumina can be seen in Fig. 3.12.

The photoresist is then removed, with the Microstrip ultrasound bath lasting for approximately 40 minutes.



(a) Open area above bottom contact pads for crossbar arrays (**N3MA3**).

(b) Open area above bottom contact pads in individual device (**N3MA1**).

Figure 3.12: (**N3MA1**) Vias to the bottom pads and pillars opened by ion milling.

Second passivation and second via opening to bottom pads

After the bottom pads are exposed through the alumina layer, the entire sample is passivated with a very thick layer of SiO_2, deposited in the Alcatel SCM 450 magnetron sputtering machine. This will protect the lateral walls of the bottom electrode and cover the pads and the exposed top face of the pillar in

equal thicknesses of material. A calibration sample (S2) is included to calibrate the deposited thickness. The deposition conditions are summarized in Table 3.12.

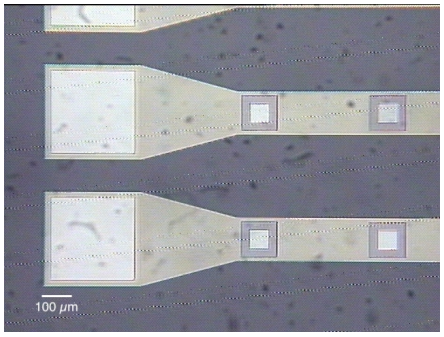
	P_f (W)	p (mTorr)	Ar flow (sccm)	t_{dep} (min)
Read	140	1.92	20	100

Table 3.12: (**N3MA1**) Operational parameters for the second insulating layer deposition in Alcatel SCM 450.

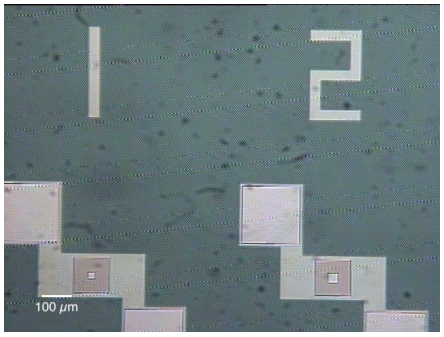
The deposition thickness was measured as $\bar{t}_{dep3} = 2727 \pm 50$ Å, a value close to the expected value of 2500 Å ($t_{Ti/Pt} + t_{MgO} + t_{Ta/Ru}$).

After the passivation step, it is essential to reopen the vias to the bottom pads and to expose the top face of the pillars again. Since the latter is a rather critical site, it is important to stop removing the deposited oxide as soon as the pillar is exposed. A reliable way of doing so is to use reactive-ion etching to selectively remove the silicon dioxide from the pads and the pillars, while keeping the rest of the structure mostly intact.

The lithography in this step defines open 35×35 µm^2 and 110×110 µm^2 areas, respectively over the small-area and large-area pillars (shown in Fig. 3.13), and 180×180 µm^2 and 260×260 µm^2 over the pads, for individual devices and crossbar arrays, respectively.



(a) Open area above bottom contact pads and pillars for crossbar arrays (**N3MA3**).



(b) Open area above bottom contact pads and pillars for individual devices (**N3MA1**).

Figure 3.13: (**N3MA1**) Vias to the bottom pads and pillars opened by RIE.

For the sizes of holes under consideration, it is expected that the RIE etch rate of SiO_2 will not change significantly for the pillar and pad areas [43, 44]. Since the oxide is equally thick in both types of sites, it is expected that the etching will finish at the same time in both.

The sample is then etched on the LAM Rainbow system, along with sample S2 in order to determine when the SiO_2 layer is fully etched. The deposition conditions are summarized in Table 3.13.

The etched thickness was not measured in this step; instead, a visual control of the calibration sample and the exposed areas in the photoresist were done on the microscope, checking for color and brightness cues of the metallic films in the pad and pillar area to conclude whether the etch is complete. In addition, special test areas in the dies, large enough to accommodate the microprobes of the characterization setup, were tested for electric contact, and after all etch steps were performed a

	P_f (W)	P_{ref} (W)	p (mTorr)	p_{wafer} (mTorr)	Ar flow (sccm)	CF_4 flow (sccm)	t_{etch} (s)
Set	100	0	140	-	200	100	
Read	103.4	2.1	138.70	172.1	200.8	100.0	450

Table 3.13: (**N3MA1**) Operational parameters for the LAM Rainbow RIE system in the second via opening etch.

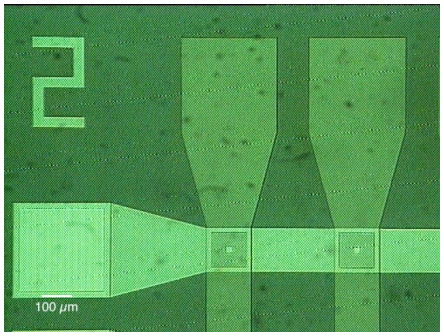
short-circuit was detected, indicating the presence of an exposed metallic material.

The ultrasound bath to remove the photoresist lasted for approximately 25 minutes.

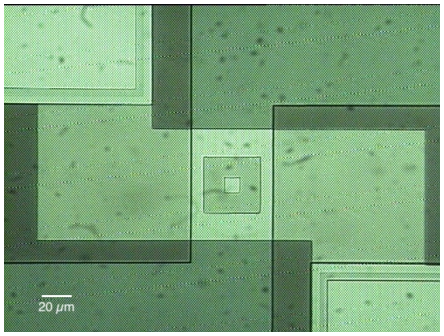
Top contact definition and metallization

The final step in the memristor fabrication process is the deposition of metallic leads, contacting with the bottom electrode and with the top of the junction pillar. They are big enough to allow the measurement of the electric properties of the device using test probes and serve also as a sacrificial material to avoid damage to the functional layers.

The lithography in this step defines open areas in the exposed pads opened by reactive-ion etching in the previous stage and conducting tracks for the crossbar arrays (shown in Fig. 3.14).



(a) Top contact pads and tracks for crossbar arrays (**N3MA3**).



(b) Detail of overlapping structures in individual junction (**N3MA1**).

Figure 3.14: (**N3MA1**) Structures defined in the fifth lithography.

The metallization process is done on Nordiko 7000 and consists of three stages: first, a 60 second soft sputter etch is done to remove impurities and contaminants from the surface of the exposed areas; the main step is the deposition of 3000 Å of an aluminium-silicon-copper ($Al_{98.5}Si_1Cu_{0.5}$) alloy by DC sputtering, which provides the conducting layer in the leads; finally, a 150 Å layer of titanium-tungsten-nitrogen compound (TiW(N)) is deposited to protect and prevent the oxidation of the exposed aluminium surface. The experimental conditions of these processes are summarized in Table 3.14 (at the time of fabrication the Nordiko 7000 module where the soft etch is performed was unavailable, so results for this step are not shown).

The final liftoff process lasted for 45 minutes, ensuring all metal outside the pads and tracks was fully removed.

	P (W)	V (V)	I (A)	p (mTorr)	Ar flow (sccm)	N_2 flow (sccm)	t (s)
AlSiCu dep	2000	398	5.04	3.1	50.1	-	80
$TiWN_2$ dep	500	428	1.18	3.0	49.9	9.8	27

Table 3.14: (**N3MA1**) Operational parameters for the metallization process in Nordiko 7000.

3.3.2 Second process

A second process, simpler than the former (samples **F3N2** and **F3N3**), features only two steps and a single oxide deposition. The bottom electrode is patterned first, which is immediately followed by deposition of a passivating oxide to level the sample surface; afterwards, the junction and top electrode layers are deposited in such a way that they overlap with the exposed bottom level in a well-defined area, allowing current flow between the two electrodes. A big advantage of this process is its greatly reduced complexity and corresponding faster fabrication time, as well as the complete elimination of redeposition phenomena from the bottom electrode material. The drawbacks are that the insulator and the top electrode have exposed sidewalls at the end of the process, resulting in damage-prone structures with potentially reduced reliability. The minimum junction area also cannot be as small as in the previous process, since a very close alignment between the two levels is necessary so that the entire stack overlaps in the intended area.

A summary of the process is shown in Table 3.15, as well as an illustration in Fig. 3.15. The process runsheet is available in Appendix A.2.

Step	Sketch	
1	(a)	Bottom electrode definition
2		Leveling oxide deposition
3	(b)	Junction and top electrode definition
4		Metallization

Table 3.15: Memristor two-step fabrication process summary (**F3N2**, **F3N3**).

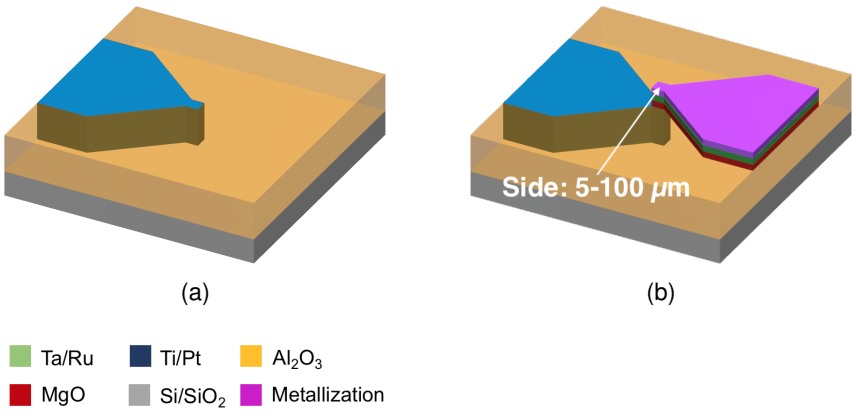
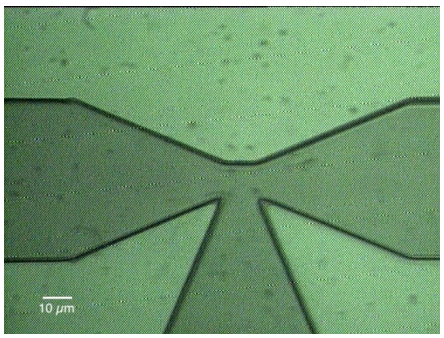


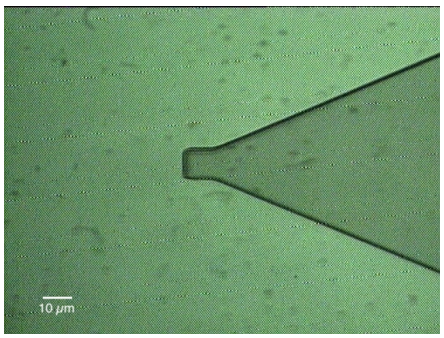
Figure 3.15: Memristor two-step fabrication process sketch.

Bottom electrode definition

The lithography in this stage defines the bottom electrode, both in individual and crossbar configurations; the shape consists in a 300×300 μm^2 pad and a short track, terminating in a tapered shape with the intended size for the junctions (seen in Fig. 3.16), to direct the current to the junction and to distribute the heat dissipated by Joule heating along the electrode tracks, since relatively high currents will be involved in the operation of the device.



(a) Detail of bottom electrode tapered area for memristor arrays.



(b) Bottom electrode pattern for individual 10×10 μm^2 individual junctions.

Figure 3.16: (**F3N2**) Structures defined in the first lithography.

The etching is performed on Nordiko 3600 with a pan angle of 60°, to remove the Ti/Pt layer and reach the insulating substrate. The etch conditions are summarized in Table 3.16.

	P_f (W)	P_{ref} (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flow (sccm)	t_{etch} (s)
Set	190	0	735	105	350	0	11	
Read	202.0	2.0	723.4	104.5	344.5	2.3	10.2	1636

Table 3.16: (**F3N2**) Operational parameters for the Nordiko 3600 in the bottom electrode etch.

The etched thickness was measured using the same technique as that used in the junction pillar definition in the previous sample, with the value obtained being $\bar{t}_{etch1} = 2341 \pm 109$ Å was measured, a very distinct value from the expected thickness of 1800 Å ($t_{Ti/Pt}$ + 50 Å overetch). The difference might be due to the fact that the etch rate of the bottom electrode materials is greater than expected for the pan angle used in this step; however, the functional integrity of the device is not compromised since the substrate layer was reached and the bottom layer can still be leveled by depositing a thicker layer of oxide.

Without removing the photoresist, a layer of Al_2O_3 is deposited in UHV2 to fill the areas from where material was removed, in order to level the sample surface again. The deposition conditions are summarized in Table 3.17.

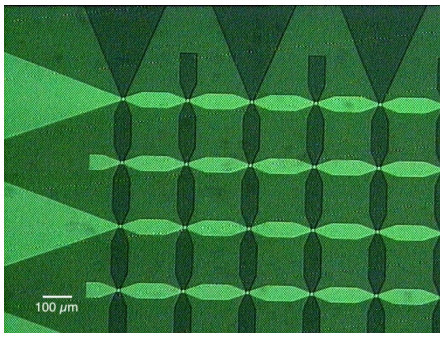
The sample then undergoes a liftoff process to expose the bottom tracks, using the ultrasound bath for around 75 minutes.

	P_f (W)	p (mTorr)	Ar flow (sccm)	t_{dep} (min)
Set	200	2.0	45	
Read	199	3.2	45.1	175

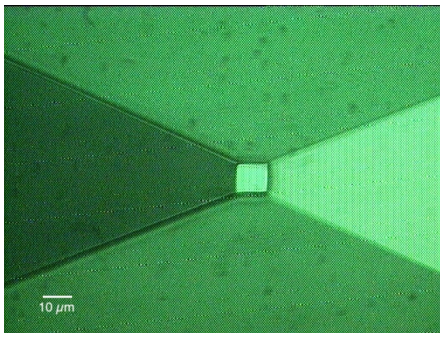
Table 3.17: (**F3N2**) Operational parameters for the first insulating layer deposition in UHV2.

Junction and top electrode definition, metallization

The lithography in this step defines the open tracks, orthogonal to the bottom tracks, where the junction and top electrode films will be deposited. These arrays have the same tapered shape at the crossings as their bottom counterparts (shown in Fig. 3.17), so that the intersection has exactly the intended area for the junctions.



(a) Top electrode pattern for 10×10 μm^2 memristor crossbar arrays.



(b) Top electrode pattern for individual 10×10 μm^2 individual junctions.

Figure 3.17: (**F3N2**) Structures defined in the second lithography.

The MgO, Ta and Ru films are deposited on Nordiko 2000, alongside a calibration sample to measure their combined thickness; the calculated values were $\bar{t}_{dep1} = 533 \pm 38$ Å. The nominal value of 550 Å is therefore contained in the experimental error of the measure.

The top tracks are then reinforced by a layer of AlSiCu, 1000 Å thick, deposited in Nordiko 7000, in sample **F3N2**. The thickness of this layer is increased in sample **F3N3**, from 1000 Å to 6000 Å. Since Nordiko 7000 was unavailable at the time of fabrication, the metallization layer in this sample consists of a [Cr 30 Å/ Au 3000 Å] × 2 stack deposited in Alcatel SCM 450. The deposition conditions for sample **F3N2** are summarized in Table 3.18.

	P (W)	V (V)	I (A)	p (mTorr)	Ar flow (sccm)	N_2 flow (sccm)	t (s)
AlSiCu dep	2000	393	5.12	3.0	50.1	-	80

Table 3.18: (**F3N2**) Operational parameters for the metallization process in Nordiko 7000.

The process is finalized by a liftoff step, which lasted for 4 hours and 20 minutes.

Chapter 4

Device characterization

4.1 Voltage/current sweep measurement program

Sample testing was carried out using a bipolar voltage-current sourcemeter (Keithley 2400-C at IFIMUP, 200 V or 1 A (max power = 22 W) and Keithley 2401 at INESC-MN, 21 V at 1.05 A) connected to two tungsten microprobes. These are placed in the bottom and top contact pads using a small amplifying microscope and lamp assembly, to aid the identification of the relevant structures in the sample surface. The measurement setup at INESC-MN is shown in Fig. 4.1.

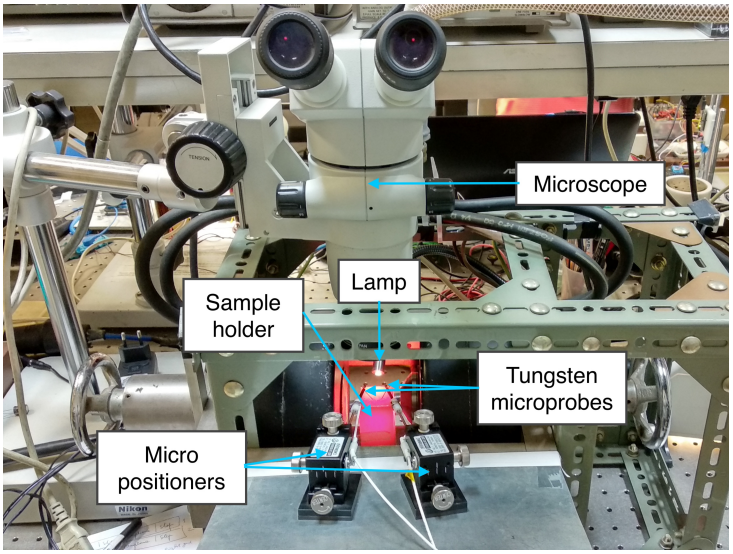


Figure 4.1: Measurement setup installed at INESC-MN.

The automated sourcemeter control at IFIMUP is performed through a LabVIEW program installed in a PC, with standard GPIB connections. While the same general setup is also installed at INESC-MN, the available measurement programs lacked the versatility necessary for the characterization of the samples fabricated in the present work. As such, this difficulty prompted the development of a basic LabVIEW program compatible with the Keithley 2401 sourcemeter, implementing the required measurement modes and data output.

The main interface of the program is shown in Fig. 4.2 and summarizes its operation mode, described as follows:

1. The source mode can be defined as either voltage or current. The minimum and maximum values of the stepwise sweep are entered, as well as the compliance value. A programmable delay time between source and measure operations can also be defined. This is useful for applications where the load electric response takes a certain time to stabilize after the source value is applied by the equipment.

2. The sweep step can be defined in one of two ways: either by defining the number of points to source and measure, including start and stop, or by defining the step size. In the latter case the sweep will only go up to the largest multiple of the step size still inside the start-stop interval. The sweep can also be defined as uni or bidirectional (Start $\rightarrow$ Stop or Start $\rightarrow$ Stop $\rightarrow$ Start).

3. The sweep points are calculated from the input parameters and stored in a queue. Other parameters can then be defined and a new sweep is appended to the queue. This allows two or more sweeps, with different endpoints, step sizes and compliance values to be run sequentially in a single execution of the program. The full queue can then be run a single time or a set number of times, which is useful for repeated, prolonged measurements.

4. The name and location of the output data file is defined. The file will be saved as *filename_suffix*, where suffix a four-digit number ranging from *0000* to *9999*. Before each write operation the current folder is automatically searched for files containing the entered file name. If one or more exist, the next suffix is incremented by one when the file is saved, which avoids overwriting any existing file.

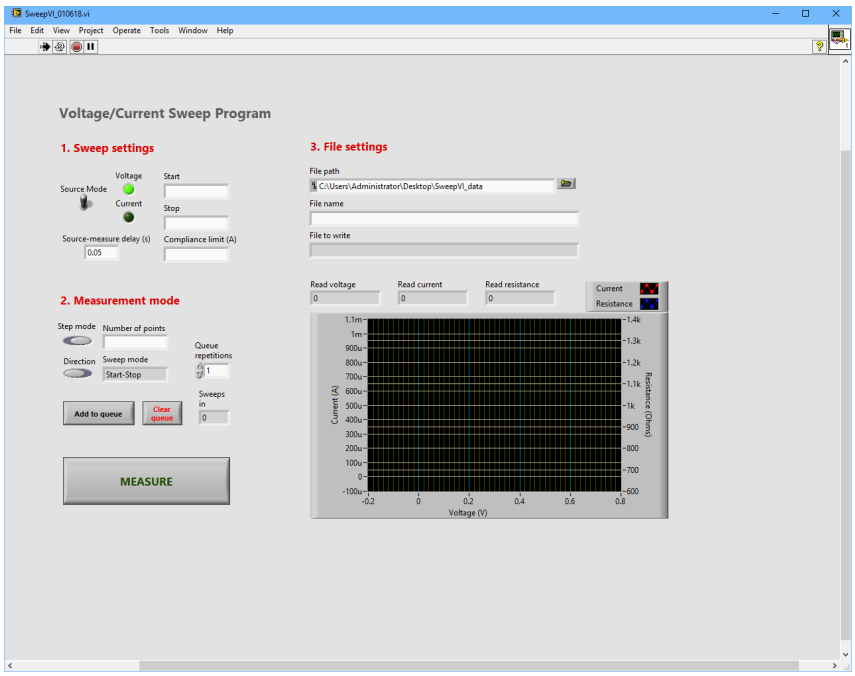


Figure 4.2: User interface of voltage-current sweep LabVIEW program.

The main source-delay-measure continuous loop is implemented in the LabVIEW block diagram shown in Fig. 4.3. The temporal evolution of the voltage applied to the device under test (the same applies for current sweeps) is represented in Fig. 4.4. Each part of the sweep has a different voltage step and time delay, respectively $\delta V_{1,2}$ and $\delta t_{1,2}$. The measured values of voltage, current and resistance are plotted in real time in the user interface.

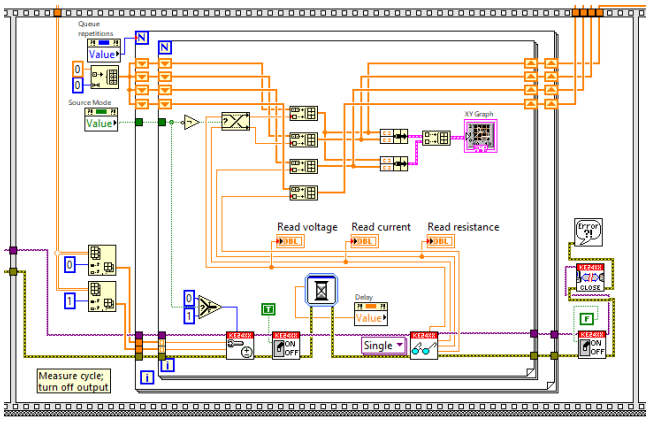


Figure 4.3: Main measurement loop and visual data printing of voltage-current sweep LabVIEW program.

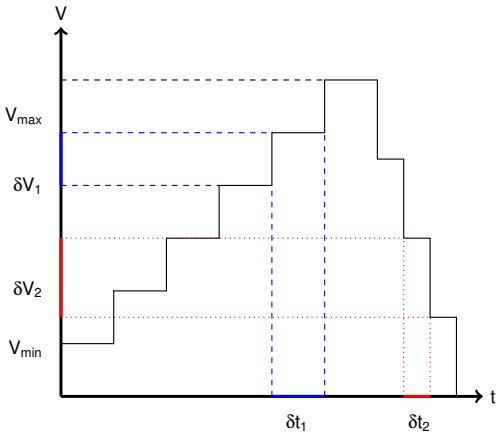


Figure 4.4: Source-delay-measure temporal diagram of voltage-current sweep LabVIEW program.

4.2 Device characterization

As discussed in Chapter 2, the most important tool for characterizing the behavior and performance of a memristor is a voltage/current sweep. The most important parameters to quantify are the Set and Reset thresholds (the voltage/current value at which the transition occurs) and the resistance values at each resistive state (R_{ON} and R_{OFF}), or their ratio.

This work focused on studying the resistive switching of MgO junctions in bipolar operation mode, so positive Set and negative Reset, using continuous voltage sweeps (the positive direction is defined as current flowing from the top to the bottom electrode). Other kinds of switching are possible in this material, by reversing polarities, using current sweeping or performing unipolar switching, but the above combination is thought to be better for prolonging device life and using smaller voltage thresholds [30].

Other measurement modes, such as pulsed sweeps, can also be used. A single voltage value is applied to the device during a specified time to induce a state transition. After a time δt a less intense pulse is applied to read the resistance value across the junction without affecting its state. However, this sort of measurement is better suited for devices which have switching thresholds and resistance values reasonably well determined beforehand, which was not the case for the samples fabricated throughout this work. As such, only continuous measurements were performed.

The delay time between source and measure operations in all measurements in this work was defined as 50 ms. The measurement protocol used is summarized in the flowchart in Fig. 4.5.

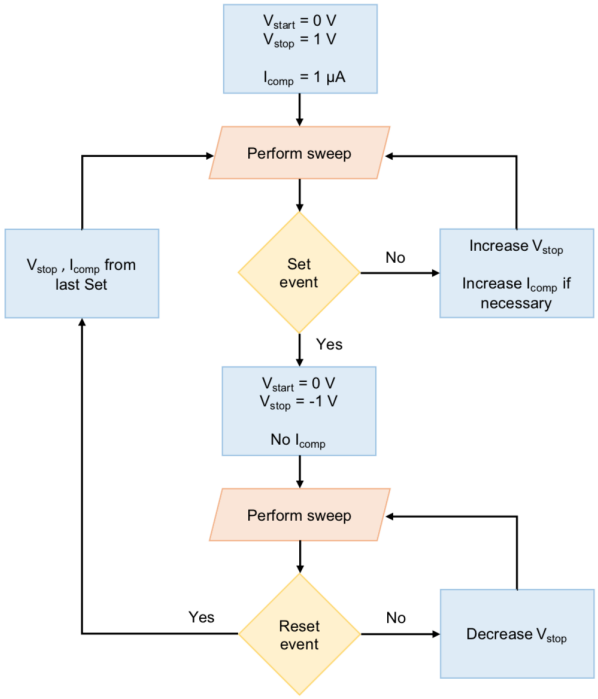


Figure 4.5: Bipolar measurement protocol flowchart for memristive devices.

4.2.1 Sample N3MA1

Electric measurements

For the initial testing of the present sample, a number of devices with different areas were sampled, in order to search for variations of the key parameters described above with the junction area. For each memristive device the maximum number of Set-Reset cycles was determined, to probe the durability of the switching behavior and whether it deteriorates with consecutive cycles.

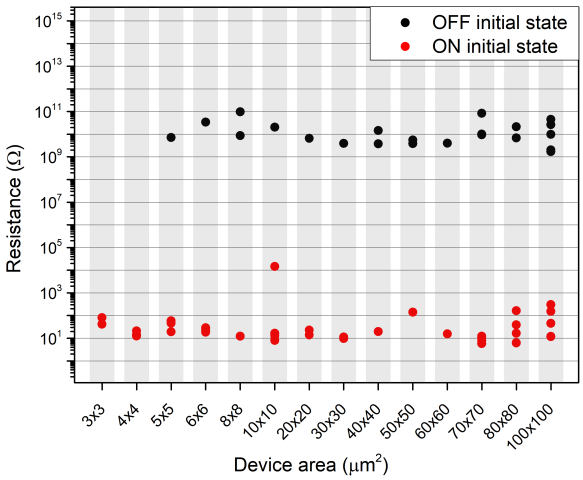


Figure 4.6: (**N3MA1**) Initial resistance values and states of all tested devices, before measuring, by area. The gray columns aid visualization by highlighting the experimental points pertaining to a single area value.

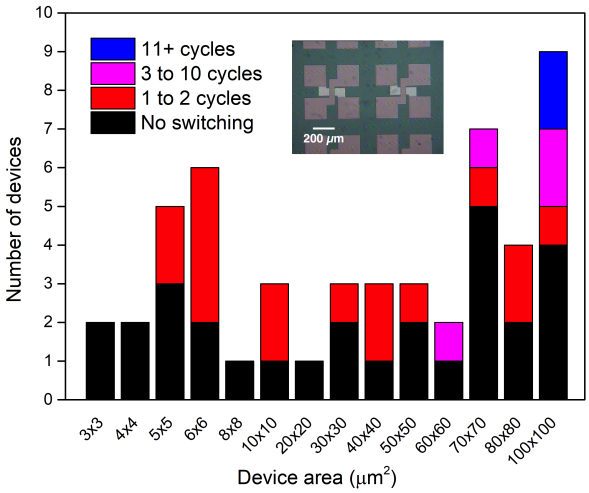


Figure 4.7: (**N3MA1**) Histogram of number of complete Set-Reset cycles per device, before failure, by area; inset: optical microscope image of finished devices.

The resistances of the as-fabricated individual devices patterned with the first process were analyzed. As shown in Fig. 4.6, the starting state of the junctions is distributed almost evenly between the ON and OFF states, with a slight larger number of devices ($\sim$ 65%) starting in the LRS. The smaller area junctions always start in the ON state, which may indicate that the platinum redeposition is not fully eliminated in these areas and short circuits are still present.

The resistance values of both states are also independent of the junction area, with a variation in each state of about two orders of magnitude around the average value:

$$R_{init}(OFF) = 10^{9} - 10^{11}\ \Omega\ ;\ R_{init}(ON) = 10^{1} - 10^{3}\ \Omega$$

The switching reliability does not seem to be determined by the starting state of the device, since some devices attain a high number of Set-Reset events even though they start in the LRS. Still, for some devices, where no switching was obtained, the low initial resistance value indicates a short-circuit across the junction, particularly for small 3$\times$3 µm^2 and 4$\times$4 µm^2 areas.

As described in Section 2.1.1, it was expected that all devices would start in a highly resistive state, since no electric field had yet been applied to the junction to form the initial conductive filament. In addition, MgO with the thickness used in this stack is a very resistive material. At the moment, the reason why some devices start in the ON state and are still able to perform resistive switching is unknown.

The overall yield of the fabrication process, summarized in Fig. 4.7, is low. The sampling across all areas has revealed that $\sim$60% of devices, regardless of starting state, do not exhibit any sort of reversible switching. In devices that do show some switching, it is nevertheless very limited: $\sim$33% of structures can only complete one or two full cycles before failure. These results are indication that one or several steps in the fabrication process were not performed adequately and have compromised the memristive device.

We now present a number of representative results of the initial transitions and complete Set and Reset resistive switches for given junction areas. These are shown in Figs. 4.8-4.12.

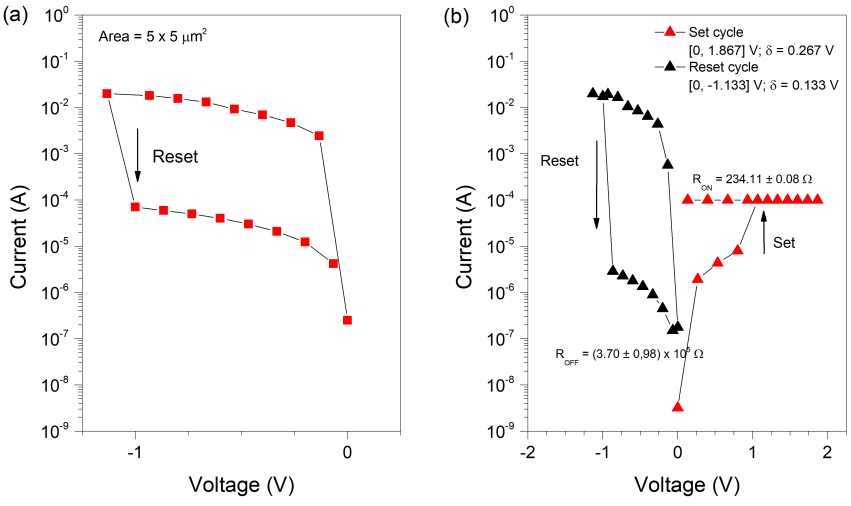


Figure 4.8: (**N3MA1**) Voltage sweeps in 5$\times$5 µm^2 individual junction: (a) First transition; (b) Complete Set-Reset cycle.

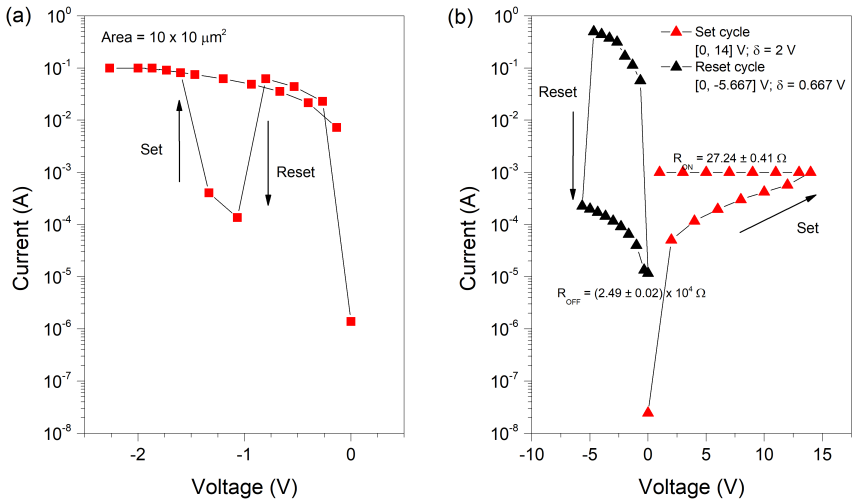


Figure 4.9: (**N3MA1**) Voltage sweeps in 10×10 μm^2 individual junction: (a) First transition; (b) Complete Set-Reset cycle.

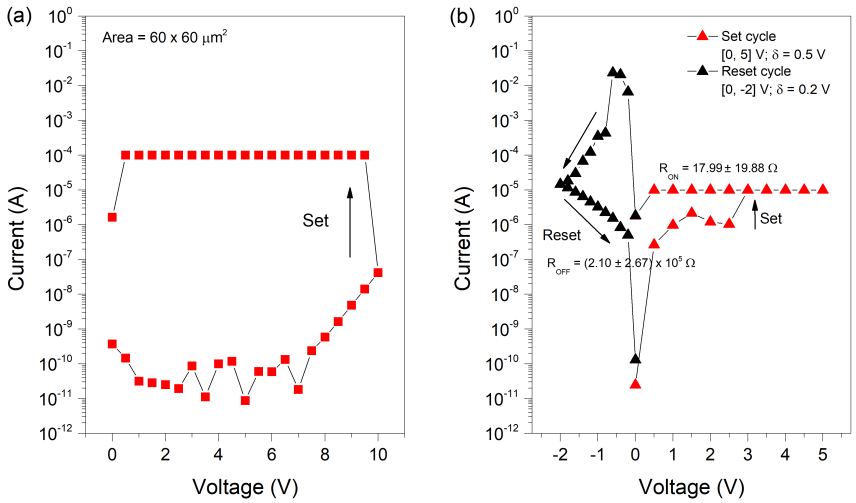


Figure 4.10: (**N3MA1**) Voltage sweeps in 60×60 μm^2 individual junction: (a) First transition; (b) Complete Set-Reset cycle.

We first observe that all depicted devices show a clear separation between the ON and OFF state resistances, with a R_{OFF}/R_{ON} around 3 orders of magnitude for the smaller area devices and up to 8 for the larger structures.

Regarding the switching threshold voltages, V_{Set} values were always higher than V_{Reset}, independent of area. The Reset voltages do not vary significantly for different areas, typically falling in the range of 0 V to -5 V; the same is not observed for the Set thresholds, which vary between 1 V and 14 V.

Although the larger spread of V_{Set} values in comparison with V_{Reset} is expected for MgO devices [29, 30], we were unable to quantify the specific dependency of both quantities with device area. This stems directly from the low yield of the fabrication process, which prevents the gathering of a sufficiently large number of switching voltages across the available areas.

The first transition in the majority of devices, as seen for example in Figs. 4.10a, 4.11a and 4.12a is a Set event at high voltage ($\sim$ 10 V), with the subsequent Sets requiring a lower value. This observation is consistent with the electroforming process generally necessary to start reversible RS cycles in insu-

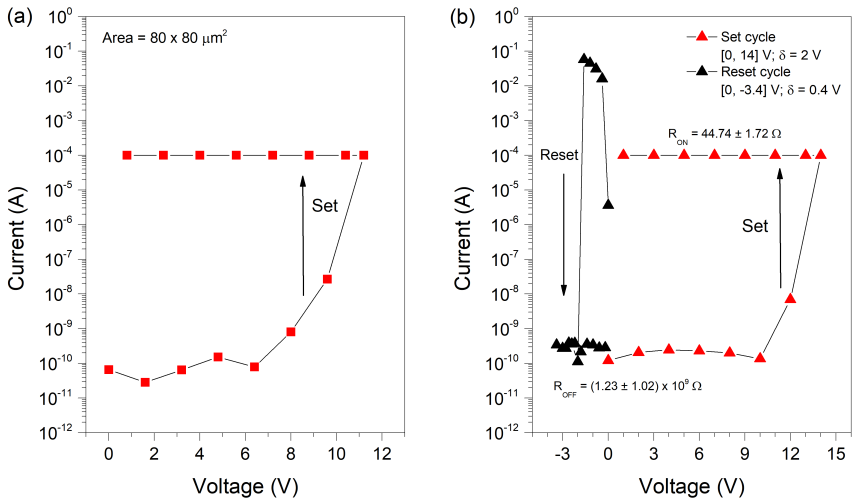


Figure 4.11: (**N3MA1**) Voltage sweeps in 80×80 μm^2 individual junction: (a) First transition; (b) Complete Set-Reset cycle.

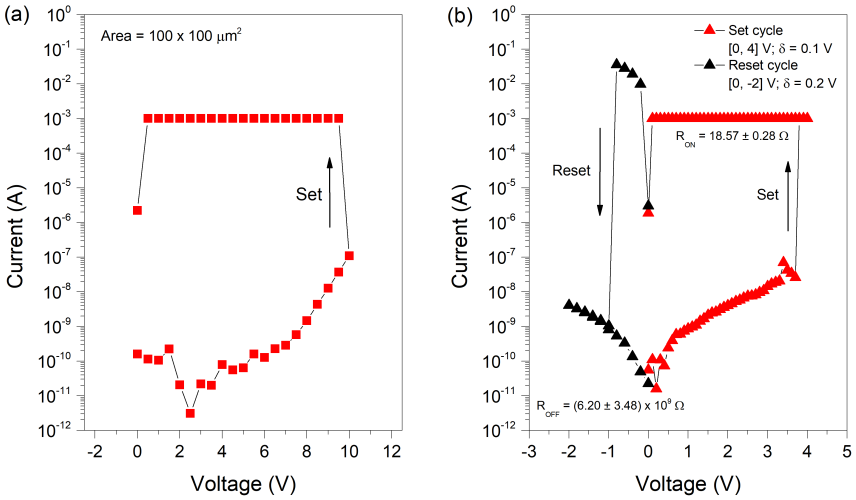


Figure 4.12: (**N3MA1**) Voltage sweeps in 100×100 μm^2 individual junction: (a) First transition; (b) Complete Set-Reset cycle.

lator materials. However, for MgO in particular, several works report both electroforming-required and electroforming-free devices; the mechanism responsible for this discrepancy is not fully established. It is proposed that variations during the sputter deposition [28] or ion beam deposition [27] conditions may result in different levels of defects in the MgO crystalline structure. This in turn facilitates or impedes the formation of the first filament and corresponding transition [28, 29, 30].

In some devices each Set event happens at a progressively higher voltage than the last, as depicted in Fig. 4.11. This evolution is an indicator of accumulated damage in the active layers of the structure, and commonly seen when device failure is imminent.

As the device area decreases more devices start in the LRS in comparison with the HRS. As such, the first transition in these devices is often a Reset done at negative voltage, as seen in Figs. 4.8a and 4.9a.

Another cause of device failure are the sporadic unipolar transitions when attempting a single Reset switch. In this situation, illustrated in Fig. 4.9a, a Reset transition is immediately followed by a Set event

back to the LRS, during the same voltage sweep. Since Reset switches are performed without establishing a current compliance, if a Set event unexpectedly occurs the resistance will decrease sharply and provoke a sudden current surge. Such a transition thus severely impacts the lifetime of the device, with residual RS cycling in the structure only possible at very high voltages and currents.

In summary, the voltage-current characteristics taken in this sample uncovered a large variability of V_{Set} values, while V_{Reset} voltages are less spread between measurements. In conjunction with the low yield of the fabrication process and damage sustained by the structures after repeated measurements, this observation makes the study of the dependence of the threshold voltages with junction area very difficult.

All memristors tested show clearly distinguishable LRS and HRS resistances, with $R_{OFF}/R_{ON} \approx 10^3$ for the smallest areas, making these MgO-based devices potentially good candidates for memory applications. However, the process yield must be improved and reliability issues mitigated. The RS cycles show that the electric response near the state transition values are not smooth, like expected for neural-like behavior discussed in Chapter 2. In contrast, they are very sudden and without any discernible dynamic behavior in these regions. This may indicate that other measurement modes, such as pulsed current-driven sweeps may be necessary to uncover this electric response [7, 45].

Going back to the sample endurance data summed up in Fig. 4.7, we see that, in a limited extent, junctions with larger areas seem to be more reliable. Of all measured devices only two, both with an area of 100×100 μm^2, have presented several dozen consecutive Set-Reset transitions. This allows a more in-depth understanding of device performance after several consecutive switching events.

A general overview of the performance of both devices is depicted in Fig. 4.13. All measurements in both devices were performed with a 1 mA Set current compliance.

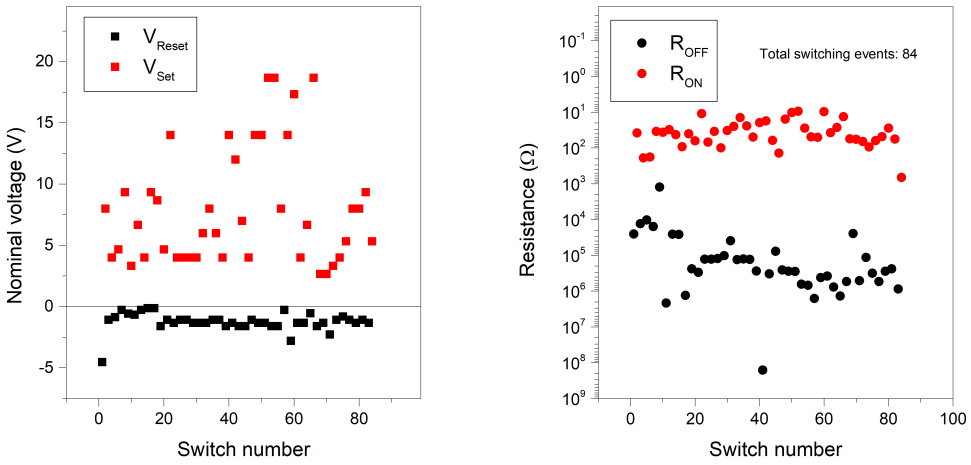
In the first memristor (Fig. 4.13a) V_{Set} values are generally high and have a large dispersion, varying from around 2 V to 18 V. No clear evolution with increasing number of cycles is visible in the graph. On the other hand, V_{Reset} values are stable throughout the measurement, varying from near zero to -3 V. In the first transition a hard reset event took place, as evidenced by the larger than usual voltage (-5 V) needed to bring the device to the HRS.

Regarding the resistance values represented in the figure, the ON state has a tight distribution of values, varying from 10 Ω to 1 kΩ. Although the OFF state resistances are more slightly spread out, the two states can nevertheless be clearly distinguished from each other.

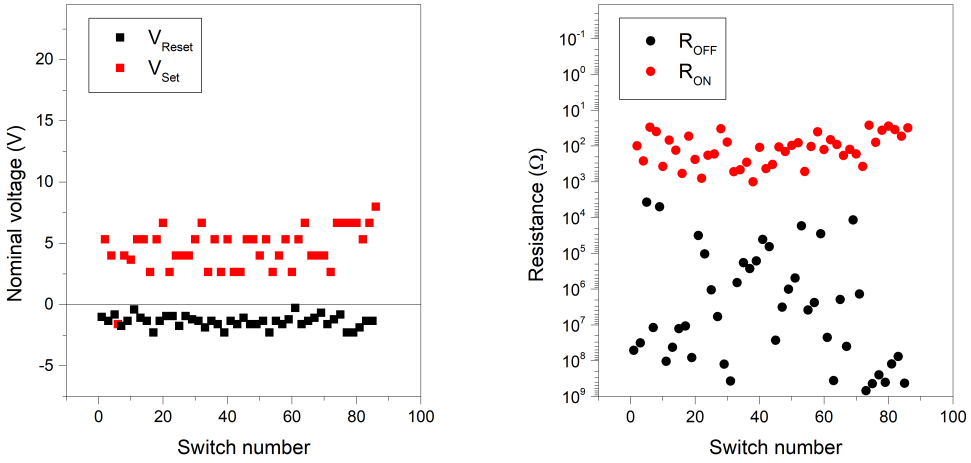
The second device, unlike the first, displayed a stabler distribution of threshold voltages for both Set and Reset events. While the Reset voltages, seen in Fig. 4.13b, are similar to the previous example, the Set values are restricted to an interval between 2 V and 8 V. Again, no apparent time evolution is visible.

The trends observed for the voltage thresholds are confirmed by other experimental studies done on MgO resistive switching [30, 29].

The resistive states of this device are still distinguishable. Despite the fact that the HRS resistances present a much larger dispersion than the first case, they do not overlap with those of the LRS, which vary between the same orders of magnitude. This contrasting distribution of values between the two states has been observed in other experimental work [29, 30, 45], and can be explained by the fact that



(a) First 100×100 µm^2 individual junction (after 84 Set/Reset transitions).



(b) Second 100×100 µm^2 individual junction (after 86 Set/Reset transitions).

Figure 4.13: (**N3MA1**) Set and Reset voltage thresholds and resistances in the On and Off states, for two 100×100 µm^2 junctions with large number of cycles (I_{comp} = 1 mA).

both Set and Reset transitions present different dynamics. In the former only a few conducting filaments form the connection between the top and bottom terminals, a number independent of the junction area [27], due to the self-limiting nature of the process. In the latter those filaments can break in a variety of places along the length and to different extents. This translates into a larger dispersion of R_{OFF} values in comparison with R_{ON}.

In summary, the electric characterization of this sample uncovered the low yield of the fabrication process. The memristive devices show a generally poor robustness when subject to consecutive switching cycles. The performance was inconsistent across junction areas, although a slightly better endurance during the switching process was observed on larger structures.

The next step in understanding potential shortcomings of the fabrication process, and how it results in poor electric reliability of the devices, is to perform a direct physical inspection of the sample.

SEM inspection

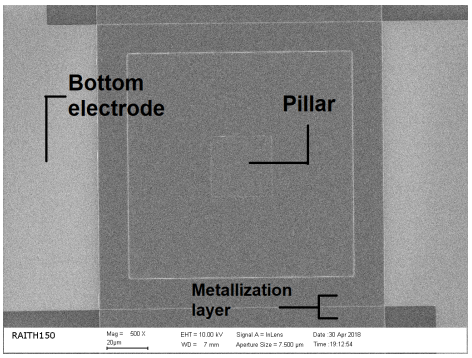
In order to try and understand the impact of the fabrication process in the electric behavior of the devices a SEM inspection was performed on the Raith-150 E-beam system. The focus of the observation was in

and around the pillar area, since it contains the MgO thin film responsible for the resistive switching. It is thus the most critical location in case the fabrication process results in defects that affect the topography or composition of the active structure. The conditions used for SEM inspection throughout this work are summarized in Table 4.1.

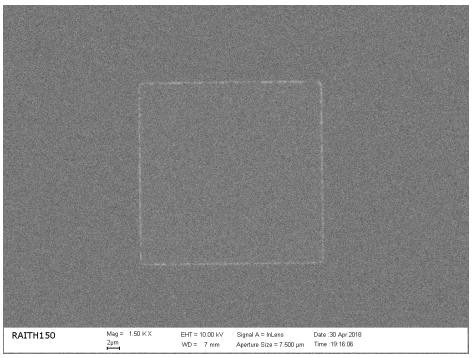
Parameters	
Beam aperture (µm)	7.500
Electron high-tension (kV)	10.00
Working distance (mm)	7
Magnification (×1000)	0.500 to 7.50

Table 4.1: Inspection conditions for SEM observation in Raith-150 E-beam system.

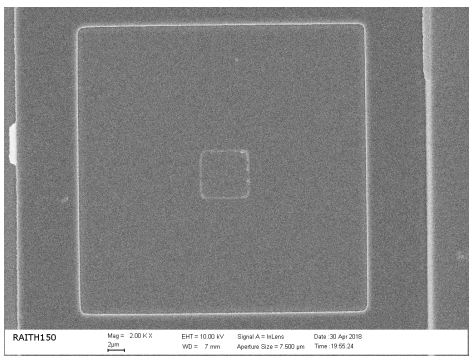
Several elements, both in a virgin state and after measurement, were observed. The SEM images of representative devices are shown in Figs. 4.14-4.16.



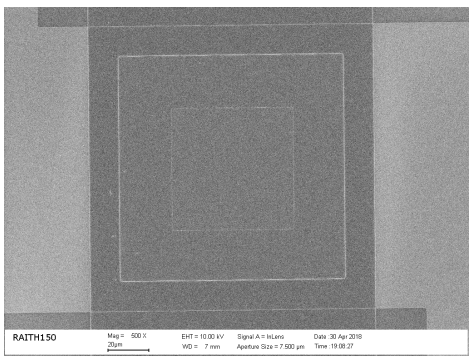
(a) 30×30 µm^2 individual junction.



(b) 30×30 µm^2 individual junction (detail of pillar region).



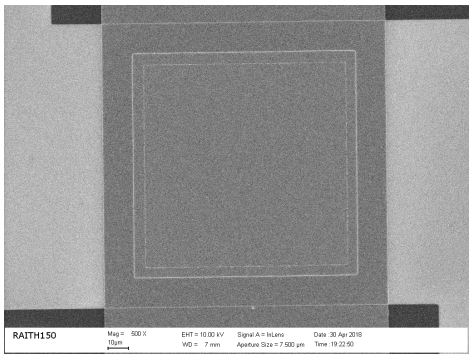
(c) 6×6 µm^2 individual junction.



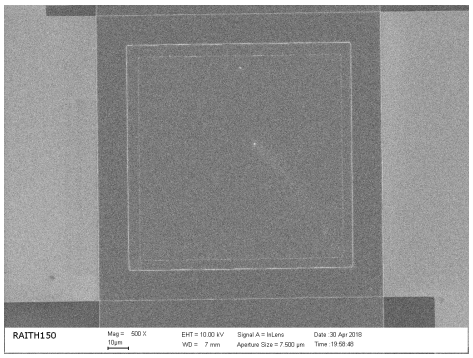
(d) 60×60 µm^2 individual junction.

Figure 4.14: (**N3MA1**) SEM observation of 6×6 µm^2, 30×30 µm^2 and 60×60 µm^2 unmeasured devices.

The virgin structures depicted in Fig 4.14 have pillar junctions with the intended areas and well-defined borders in the bottom and top tracks and oxide passivation walls. On closer inspection (Figs. 4.14c and 4.14b), we can see that the pillar walls are not uniform. Brighter segments along the contour indicate material accumulation or topography changes in those areas. This visual aspect points to the presence of liftoff residues formed after the first passivation of the pillar sidewalls with Al_2O_3. These are formed because the resist profile is sloped and is further affected by the etching step in the pillar

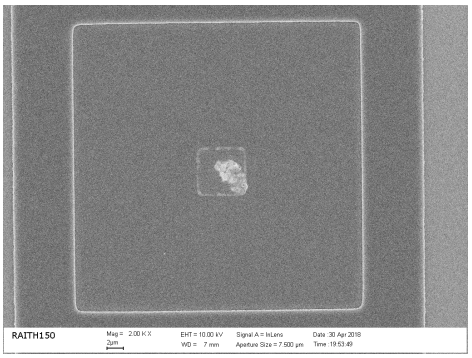


(a) 100×100 µm^2 individual junction (after 7 Set/Reset transitions).

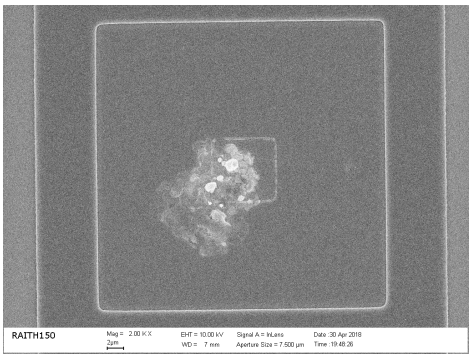


(b) 100×100 µm^2 individual junction (after 86 Set/Reset transitions).

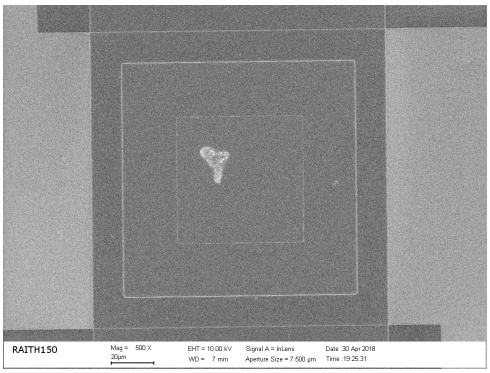
Figure 4.15: (**N3MA1**) SEM observation of 100×100 µm^2 devices after measurement.



(a) 6×6 µm^2 individual junction (after 2 Set/Reset transitions).



(b) 8×8 µm^2 individual junction (after 2 Set/Reset transitions).



(c) 60×60 µm^2 individual junction (after 5 Set/Reset transitions).

Figure 4.16: (**N3MA1**) SEM observation of 6×6 µm^2, 8×8 µm^2 and 60×60 µm^2 devices after measurement-induced failure.

definition.

Devices that exhibit several Set-Reset events during normal testing, such as those shown in Fig. 4.15, seem identical to as-fabricated devices, with no morphology changes apparently caused by the measurement process. In contrast, the analysis of structures that have undergone electric failure during testing reveal that this deterioration translates in material disintegration in and around the pillar.

Due to the rather large electric fields and current densities involved in the Set and Reset processes (a

quantitative analysis is provided in the discussion of sample **F3N2**), it is likely that device disruption happens due to electromigration in the AlSiCu metallization layer. When a conducting material is subject to a DC electric current, the conducting electrons scatter off the atoms in the lattice due to interaction with phonons. Electric resistance is the macroscopic manifestation of the momentum transfer from the electrons to the crystal lattice atoms due to this interaction [46]. For high enough current densities, around $10^4 - 10^5$ A/cm^2, the transfer of momentum is such that the atoms are displaced from their equilibrium positions in the lattice and diffuse along the direction of the electron flow. This movement causes material depletion from certain regions and accumulation in others; this process is called electromigration, and is a major factor in the limitation of the useful lifetime of integrated circuits [47].

These structural defects always appear in or around the junction pillar, and even though they can be fully contained in the pillar section (particularly for large-area devices, such as in the case of Fig. 4.16c), more commonly they happen along the pillar border. The most likely reason the devices only survive a few switching cycles before a permanent resistance change occurs are the liftoff residues seen previously in Fig. 4.14. These sharp upward features around the edges of the junction are produced near the start of the process, so that all materials deposited on top of them will follow their shape (according to Fig. 3.3). Particularly in the metallization stage, the AlSiCu reinforcement layer will be thinner than expected along the pillar walls, which leads to a localized increase in current density. This in turn leads to accelerated electromigration in this region and eventually to the disruption of the electrode and the device.

4.2.2 Sample N3MA3

Electric measurements

Similarly to sample **N3MA1**, a global overview of the initial resistances and the endurance of the devices in sample **N3MA3** (crossbar array configuration) are shown in Figs. 4.17 and 4.18.

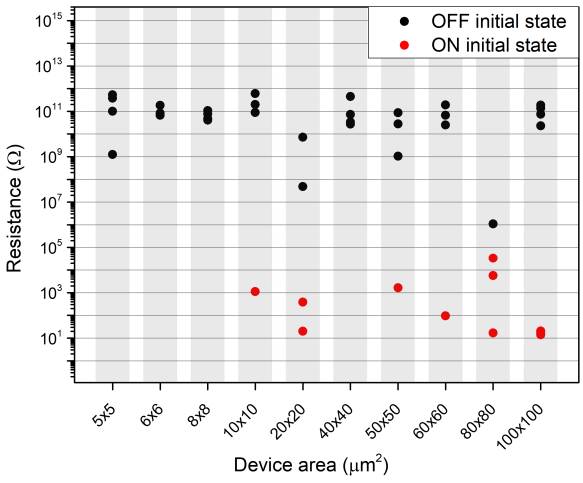


Figure 4.17: (**N3MA3**) Initial resistance values and states of 44 tested devices, before measuring, by area.

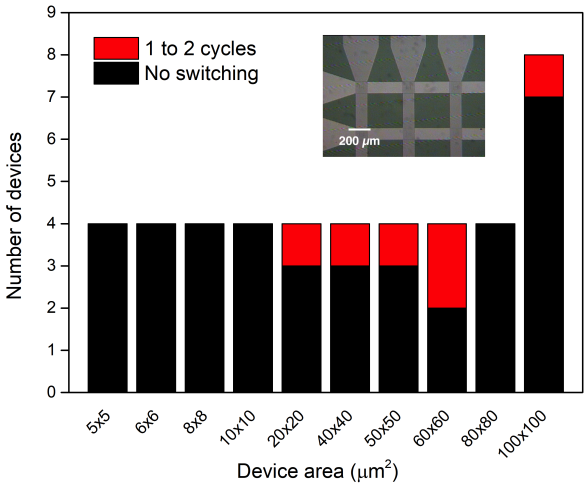


Figure 4.18: (**N3MA3**) Histogram of number of complete Set-Reset cycles per device, before failure, by area; inset: optical microscope image of finished devices.

In general terms this sample presents a worse performance than individually patterned devices. Out of 44 measured memristors only 6 exhibited switching behavior, and in those only one to two cycles were possible before a permanent state change rendered the structure inoperable.

With regards to the initial resistances of the devices, we found that a majority of as-fabricated devices start in the HRS, in contrast with the individual devices in sample **N3MA1**. Elements with smaller areas show exclusively this property, while more devices with larger areas present a lower initial resistance.

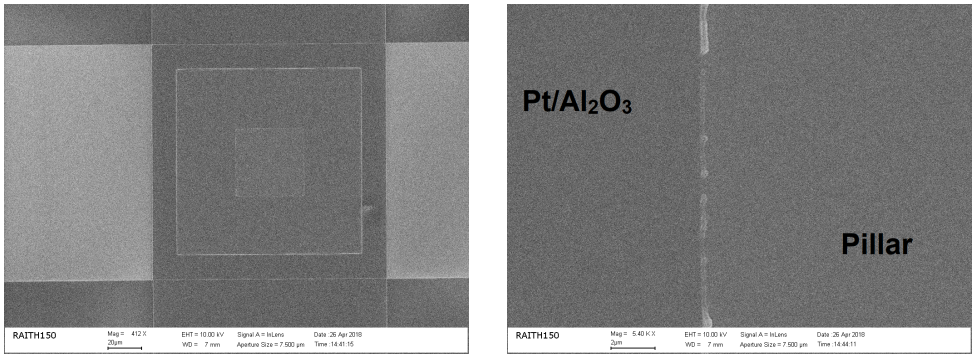
Again, the presence of resistive switching is not influenced by the starting state of the device, since among the elements that attained at least a full Set-Reset cycle, some start in the LRS and others in the HRS. On the other hand, all but one of the smaller area devices (5×5 µm^2 to 10×10 µm^2) start in the HRS, while none achieve switching. A possible explanation to this correlation is that the RIE step to open the vias to the bottom electrode pads and to the top face of the pillar (Fig. 3.9e in the long process schematic) failed to do so. This means that some oxide remains in the area, and the electric connection through the junction is interrupted. Even though the RIE endpoint was controlled using profilometry and electric contact testing in calibration areas and bottom electrode pads, the pillar areas are too small to test directly using these methods. Thus, no definitive conclusions can be drawn.

The complete fabrication process used for individual memristors presented a low yield, but nevertheless resulted in some devices that displayed a meaningful number of RS cycles. However, the same process when applied to a crossbar configuration failed to do so. Thus, due to the lack of working devices in this sample no further electric characterization is possible, and we can conclude that the fabrication process, as is, is not adequate for the patterning of memristor crossbar networks.

The most likely explanation for these results is the aggravation of the liftoff issues, identified in the SEM inspection of the previous sample, which prevent operation in nearly all structures. To confirm this hypothesis a SEM analysis was also performed in this sample, and is presented below.

SEM inspection

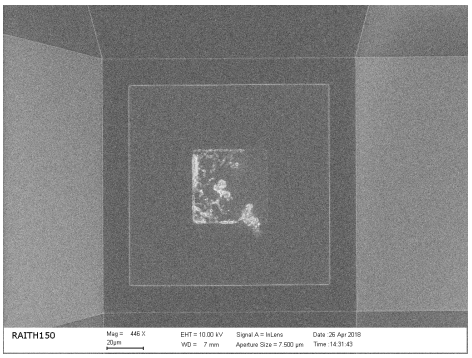
A SEM inspection was performed for this sample as well, using the same conditions, and the results are shown in Figs. 4.19 and 4.20.



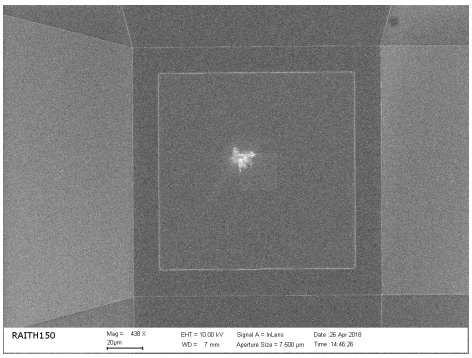
(a) 40×40 µm^2 junction.

(b) 40×40 µm^2 junction (close-up of pillar wall).

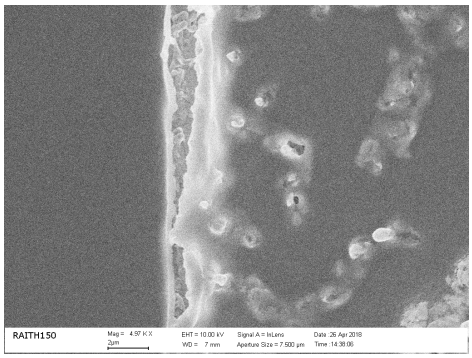
Figure 4.19: (**N3MA3**) SEM observation of 40×40 µm^2 unmeasured device.



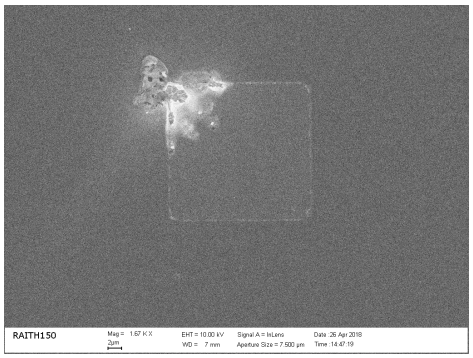
(a) 40×40 µm^2 junction (after 1 Set/Reset transition).



(b) 20×20 µm^2 junction (after 2 Set/Reset transitions).



(c) Close-up of pillar in Fig. (a).



(d) Close-up of pillar in Fig. (b).

Figure 4.20: (**N3MA3**) SEM observation of 20×20 µm^2 and 40×40 µm^2 devices after measurement-induced failure.

The devices in this sample exhibit the same general aspect as in sample **N3MA1**. Liftoff residues are quite pronounced around the pillar walls, as shown in Fig. 4.19b, which will aggravate the electromigration issues already described. This is seen for instance in Fig. 4.20c: the destruction of the pillar sidewall leads to the deposition of material forming a direct connection from the top to the bottom electrode during testing. Several spots where the AlSiCu has electromigrated upwards can also be seen.

When fabricated in an array configuration the memristor devices perform worse than individual elements, as found during testing. This is due not only to the specific challenges and restrictions of a crossbar architecture (longer current paths, capacitive interference between adjacent tracks, inability to address certain junctions due to the possibility of current sneak paths [48], etc.), but also to the difficulties of this specific fabrication process. In particular, the problem of residues is aggravated since a thicker oxide layer was deposited in the first passivation, making them taller and sharper and more likely to disrupt the AlSiCu film.

Since the junction pillar is defined by etching (subtractive process) and the passivation oxide involves a liftoff process (additive), the requirements for the shape of the photoresist and the etch pan angles are contrasting for the two steps. Thus, the optimization of positive photoresist to minimize liftoff residues is not straightforward.

A different approach to this issue would be to use a negative photoresist in the junction definition step. An undercut profile is much easier to obtain with this type of compound, so that no oxide is deposited

on its sidewalls; thus, residue formation is minimized. However, this is not part of the standard optical lithography procedure, and so this approach was not attempted.

A new, simpler process (described in detail in Section 3.3.2), that bypasses most of the complexity and time necessary in the first, was designed. It consists of only two lithography steps and a single passivation step. Samples **F3N2** and **F3N3** were fabricated according to this process, and their characterization is presented below.

4.2.3 Sample F3N2

Electric measurements

As in the previous cases, the initial resistance values of a large sample of devices and the RS cycling endurance of a subset of those are shown in Figs. 4.21 and 4.22.

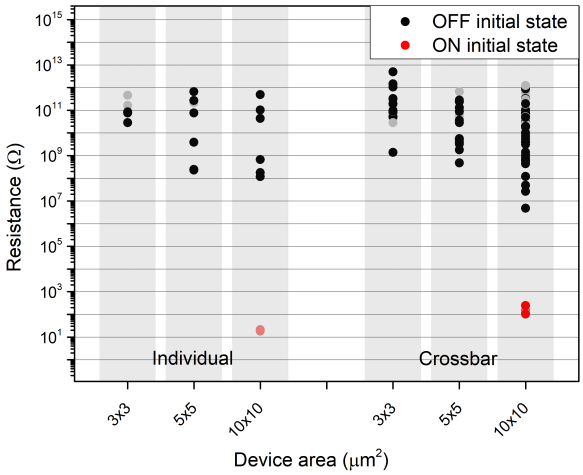


Figure 4.21: (**F3N2**) Initial resistance values and states of 105 devices in individual and crossbar configurations, before measuring, by area. The 32 points in lighter color correspond to devices where RS cycling was performed.

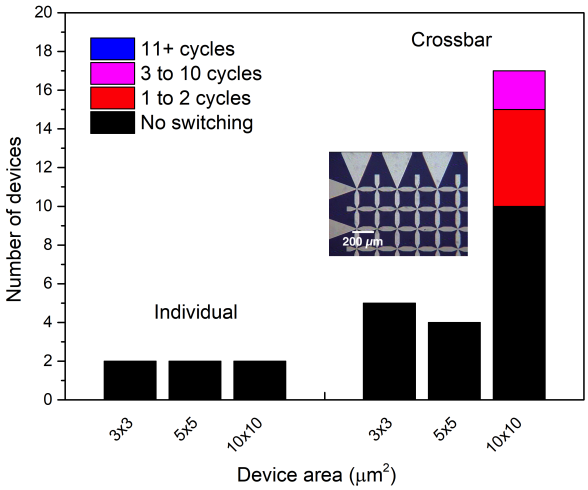


Figure 4.22: (**F3N2**) Histogram of number of complete Set-Reset cycles per device, before failure, by area; inset: optical microscope image of finished devices.

Contrary to the samples in the first fabrication process, only a very small number of 10×10 μm^2 junctions start in the LRS (9 out os 105). Since the bottom electrode is patterned first in this process and only afterwards the insulator and top electrode are deposited, issues of platinum redeposition persistent in the previous samples are highly unlikely here. These low resistance initial states may be explained then by specific regions where the leveling oxide layer does not cover the entire height of the bottom electrode sidewall. Thus, a direct path between top and bottom is created upon deposition of the former.

Regarding the majority of devices starting in the HRS, those that presented very high ($> 10^{10}$ Ω) initial resistances did not show any Set/Reset behavior. This indicates that these are not true resistive states but rather the MIM junction is ill defined. This is most likely due to alignment issues in the exposure of the second level, where no overlap with the first was achieved in the expected area.

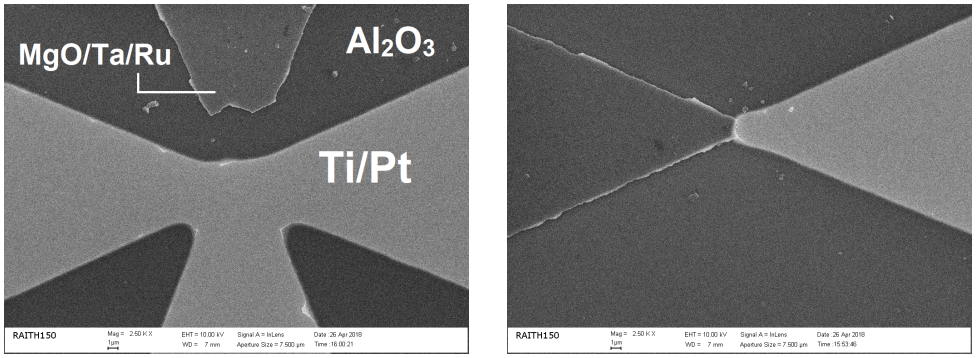
The issue of badly defined structures due to lack of overlap is more preponderant for smaller area junctions, as well as for individual devices that require a precise alignment in both planar directions.

Indeed, Fig. 4.22 shows that none of the measured individual devices, regardless of area, has demonstrated switching behavior. In the crossbar configurations only the 10×10 µm^2 junctions have exhibited some amount of cycling, although their endurance is still very low. All these observations are evidence that the MgO and top electrode films are not being deposited on top of the bottom electrode.

These results show that the new two-step fabrication process, in its current iteration, does not improve upon the long process in terms of the performance of either individual and arrays of memristors. Since the topography of the present structures is much simpler than before, a direct SEM observation will yield a more clarifying picture of fabrication issues and ways of improvement.

SEM inspection

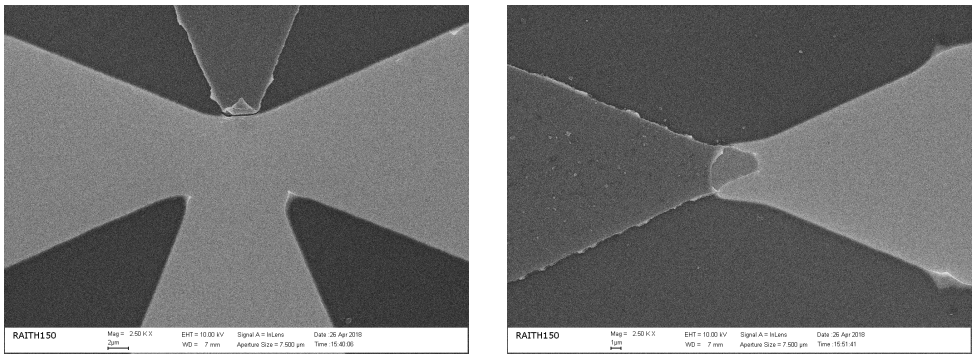
The SEM images for this sample are shown in Figs. 4.23-4.26.



(a) 3×3 µm^2 junction in single row-multiple columns array.

(b) 3×3 µm^2 individual junction.

Figure 4.23: (**F3N2**) SEM observation of 3×3 µm^2 unmeasured devices.

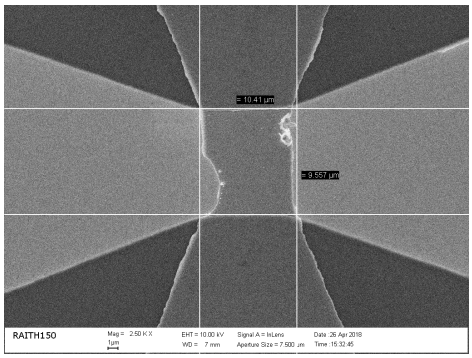


(a) 5×5 µm^2 junction in single row-multiple columns array.

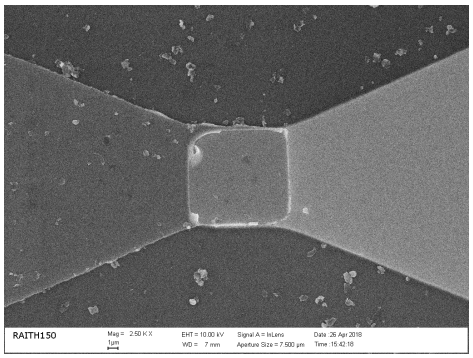
(b) 5×5 µm^2 individual junction.

Figure 4.24: (**F3N2**) SEM observation of 5×5 µm^2 unmeasured devices.

In the case of the 3×3 µm^2 junctions, the reason why only very low current values were read for all such devices and no resistance state changes were observed (as shown in Fig. 4.22) is readily apparent by observing Fig. 4.23. There is little to no overlap between the bottom and junction/top structures, and hence there is no path through which electric current can pass. The most likely explanation for this observation is the poor photoresist profile in the top level definition. If the development time had not

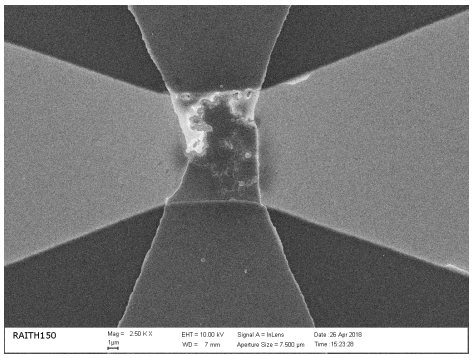


(a) 10×10 µm^2 junction in multiple rows-multiple columns array.

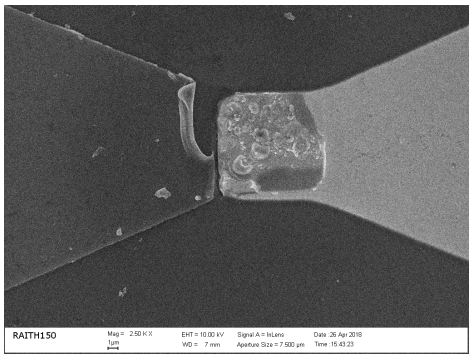


(b) 10×10 µm^2 individual junction.

Figure 4.25: (**F3N2**) SEM observation of 10×10 µm^2 unmeasured devices.



(a) 10×10 µm^2 junction in multiple rows-multiple columns array (after 6 Set-Reset transitions).



(b) 10×10 µm^2 individual junction (after 5 Set-Reset transitions).

Figure 4.26: (**F3N2**) SEM observation of 10×10 µm^2 devices after measurement-induced failure.

been sufficient to fully remove the photoresist in the intersection area, the MgO and top level materials would have been deposited over the covered area. Afterwards, they would be removed during the liftoff process, leaving no functional materials over the intersection and thus no working device.

For the 5×5 µm^2 devices the same kind of phenomenon happened: Fig. 4.24a shows a gap between the two levels, again due to a poor definition of the photoresist during the second exposure. In addition, a liftoff residue is clearly visible in the termination of the top electrode. In the individual junction shown in Fig. 4.24b there is some overlap between the two electrodes, but the intersection is poorly defined and does not have the intended shape or area. Thus, no resistive switching is observed for these junctions.

The 10×10 µm^2 devices are, in a general manner, better defined than those with smaller areas, since the overlap of the two levels is clear and the intersection area close to the expected value. Nevertheless, they are affected by the same lithography issues as the previous elements (seen especially in the poor definition of the top electrode contour and the indentation on the intersection zone, in Fig. 4.25a). In addition, the debris seen in Fig. 4.25b is the contamination of the sample surface with material from the deposited layers outside the desired areas. This is another typical side-effect of the liftoff process, however, such residues are unlikely to affect device operation.

The SEM inspection of devices after measurement immediately show the extent of the damage

caused by the measurement process. Each successive change of the resistive state of the device further degrades the thin films of the top electrode. Fig. 4.26a shows that the top electrode and reinforcement layer has been removed from most of the junction area. The individual device in Fig. 4.26b is broken at the interface between the top and bottom levels, while the remaining material in the junction appears discontinuous.

For LRS-HRS transitions rather high current compliances are usually needed, meaning that the current densities attained in the metallization layer are also very large. Table 4.2 summarizes the current density (all values in MA/cm^2) in the 1000Å AlSiCu film cross section for common I_{comp} values and for the widths of the devices that displayed some Set-Reset cycles in sample **F3N2** (5×5 µm^2 and 10×10 µm^2). The same values but for a thicker film of 6000 Å and a larger width of 100 µm are also presented for comparison.

I_{comp} (mA)	t = 1000 Å			t = 6000 Å		
	w = 5 µm	w = 10 µm	w = 100 µm	w = 5 µm	w = 10 µm	w = 100 µm
50	10	5	0.5	1.667	0.833	0.083
100	20	10	1	3.333	1.667	0.167
200	40	20	2	6.667	3.333	0.333
300	60	30	3	10.000	5.000	0.500
500	100	50	5	16.667	8.333	0.833

Table 4.2: Current densities in the AlSiCu reinforcement layer cross-section for select junction track widths and typical compliance currents, for two film thicknesses (in MA/cm^2).

Detailed work done by Kraft and Arzt [49] shows that the mean time-to-failure of a sputter-deposited AlSiCu film 2 µm wide and 0.88 µm thick can decrease by up to one order of magnitude, from 100 to 10 hours, by increasing the current density from 1 to 2 MA/cm^2. These structures have smaller widths than those treated in this work; in addition, the data is taken at constant voltage [50], unlike the voltage sweeps employed in the device characterization process. Nevertheless, these results are still valuable and allow a better understanding of failure conditions, and thus how to improve the fabrication process. In this light, the current density values presently attained during operation (in Table 4.2) will indeed lead to irreversible damage in the junction, and so it is necessary to reduce them significantly.

In summary, a number of issues with the two-step fabrication process have been identified in the SEM observation of devices before and after measurement. In the first place, the poorly defined shape of the photoresist exposed in the top level lithography results in faulty or even non-existent contact with the bottom electrode, leading to defective memristive devices. In junctions that are reasonably well defined only a few Set-Reset cycles can be achieved before the physical disruption of the thin films leads to device failure. This behavior is attributed to electromigration happening in the AlSiCu metal reinforcement layer. Another issue is the height step between the bottom electrode and the leveling oxide. Despite being small, it can lead to a localized increase in the current density at the interface with the MgO and top electrode levels, which exacerbates the electromigration in this region.

Having identified the problems described above, a number of changes have been made to the second fabrication process to increase its yield and the reliability of memristive devices:

- A 15 second pre-development step (described in Section 3.1.7) will be performed in both lithography steps, in order to verticalize the photoresist walls as much as possible and minimize liftoff residues in the leveling oxide and the top layers.
- A soft etch step will be performed before the metal reinforcement of the top electrode, to ensure the surface is clean of any environmental contaminants and residue left by previous process steps.
- The metallization film thickness will be increased from 1000 Å to 6000 Å. This will have the effect of decreasing the current density in this layer, consequently mitigating electromigration effects and improving device reliability.

4.2.4 Sample F3N3

Electric measurements

As in the previous samples, a statistical treatment of the robustness of the measured devices is presented in Fig. 4.27. Unlike the previous examples all measured devices started in the highly resistive state, so no initial resistances map is presented for sample **F3N3**.

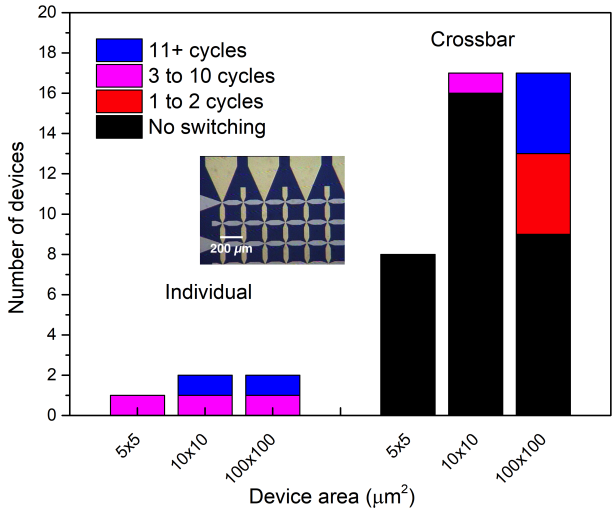
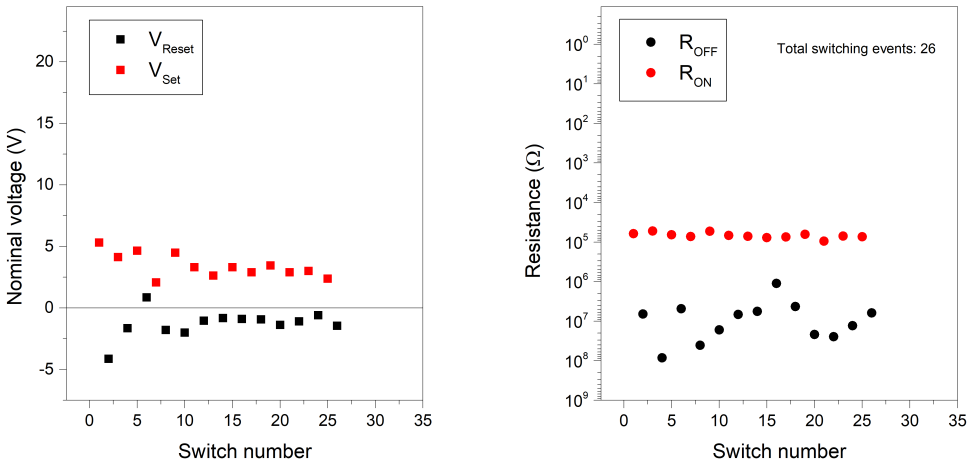


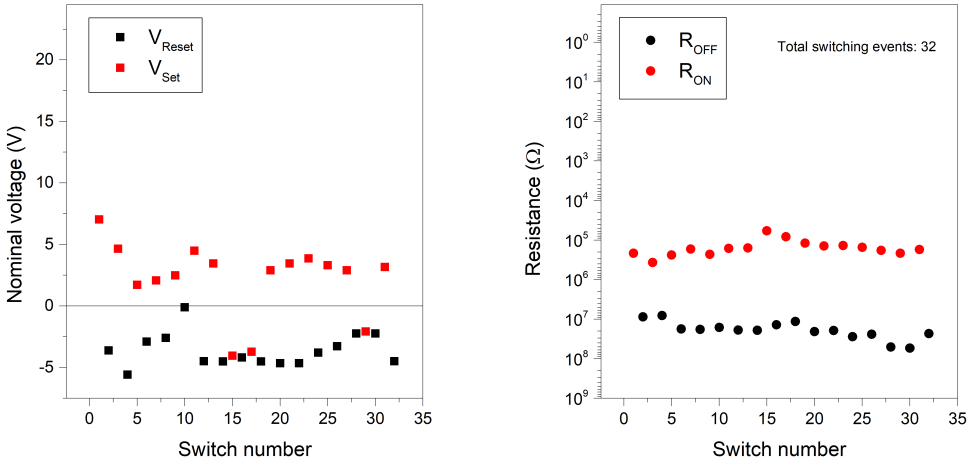
Figure 4.27: (**F3N3**) Histogram of number of complete Set-Reset cycles per device, before failure, by area, for 47 devices. The 100×100 µm^2 crossbar junctions that switch for 11+ complete cycles did not fail and are still operational after testing; inset: optical microscope image of finished devices.

Even though the yield of this process is still not optimal, as a large number of devices in crossbar configurations still do not show RS, the changes applied from the previous iteration of the process have resulted in significant improvements. All individual structures exhibit RS. The four 100×100 µm^2 crossbar devices that lasted for a large number of cycles presented stable V_{Set} and V_{Reset} values, as well as clearly separated ON and OFF states. Two such devices are represented in Fig. 4.28.

Both memristors needed a first electroforming step, around 5-7 V, but afterwards the threshold values become lower and remain so during the course of the measurements. Both devices featured a small number of unipolar transitions, as indicated by the Sets at negative voltages and Resets at positive bias, but this did not affect device reliability or endurance significantly.



(a) First stable 100×100 µm^2 crossbar junction (after 26 Set/Reset transitions).



(b) Second stable 100×100 µm^2 crossbar junction (after 32 Set/Reset transitions).

Figure 4.28: (**F3N3**) Set and Reset voltage thresholds and resistances in the On and Off states, for two 100×100 µm^2 junctions with large number of cycles.

The resistive states in both cases are well distinguishable, with a R_{OFF}/R_{ON} ratio of around 10^2. The first device shows the usual concentrated distribution of R_{ON} and the more spread out cluster of R_{OFF} values. The second memristor exhibits a very small deviation from the average for both values. This statistical treatment reveals that this process, as expected, not only has an increased yield but the electric characteristics of the devices that endure several RS cycles are also significantly improved.

The conduction mechanisms of the MgO-based memristor in this sample were also studied. By taking a log-log plot of I-V curves in both LRS and HRS, shown in Fig. 4.29, the linear parts of the curves can be fitted to a linear function. The slope thus calculated contains information about the main conduction mechanism in each state.

For the low resistive state, the slope was α_{LRS} = 0.99, the expected value for ohmic conduction. This result confirms the hypothesis that the conducting filaments in the insulator material act like ohmic conductors with an almost constant resistance value. Regarding the high resistive state, the fit of the linear-most part of the curve yielded a slope of α_{HRS} = 3.06. This value is not characteristic for any particular dielectric conduction mechanism, so it cannot be determined by a log-log graph alone. However, several such mechanisms have been proposed for MgO-based memristors, such as hopping conduction

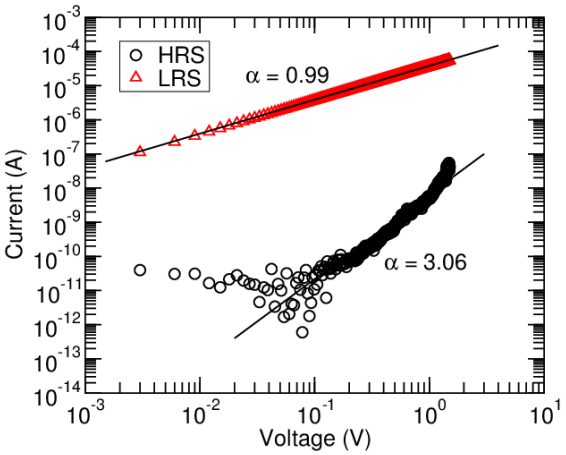


Figure 4.29: (**F3N3**) Conduction mechanisms of the Pt/MgO/Ta/Ru memristor in the high-resistance and low-resistance states.

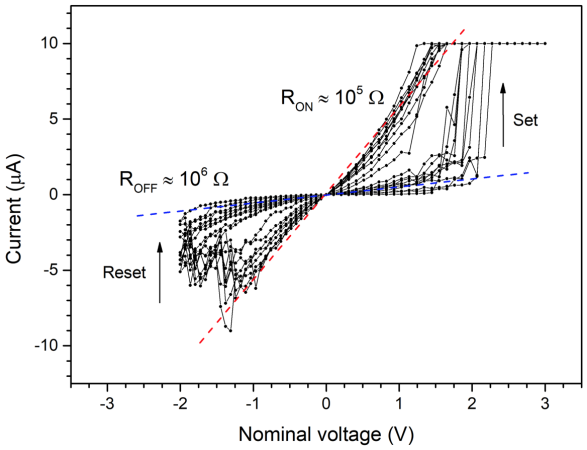


Figure 4.30: Smooth hysteretic behavior of 100×100 μm^2 crossbar junction during ∼ 10 transitions.

[28], space-charge-limited conduction [29], among others.

An interesting behavior was observed for a particular 100×100 μm^2 crossbar junction, shown in Fig. 4.30. Most other devices studied in this work so far show large resistance ratios and very abrupt Set and Reset events, with no special transition dynamics discernible. In this memristor, the ON-OFF ratio is fairly small, of just one order of magnitude. This translates in a very smooth hysteretic eight-loop figure similar to the idealized curve shown in theoretical derivations (Fig. 2.6). Also, V_{Set} and V_{Reset} values do not drift significantly with consecutive switchings, centered respectively at 2 V and -1.5 V, and neither do the resistance state values.

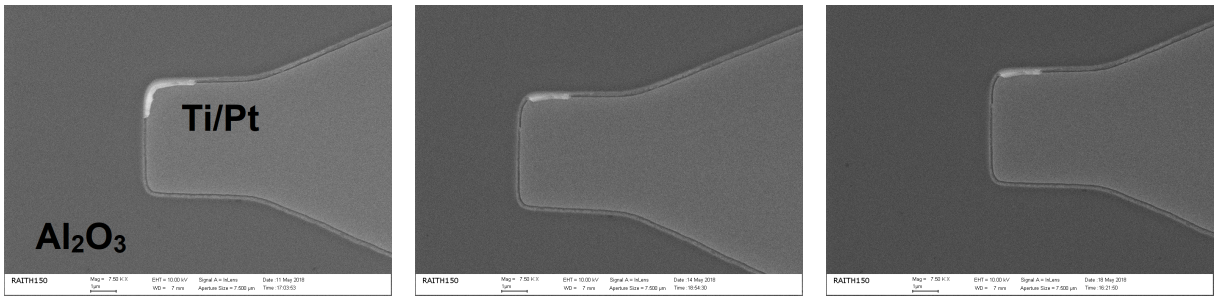
This behavior indicates that the memristive structures studied in this work could be used not just for resistive memory applications, owing to the large resistance ratios obtained in most devices, but might indeed be suited for implementations of adaptable circuits that exhibit neural-like properties. Posterior integration in more complex neural networks may be possible, although more testing is required to answer conclusively.

SEM inspection

Since the liftoff residues resulting from the leveling oxide deposition were identified in the previous samples as the main defect leading to device failure, SEM observations were carried out at the end of the first fabrication level.

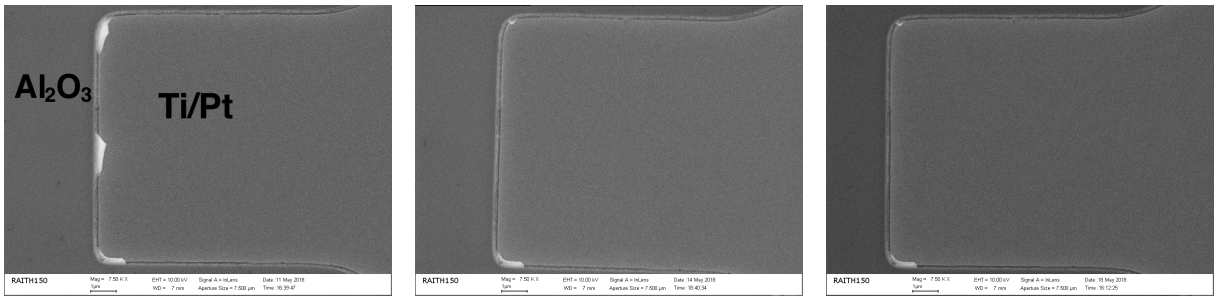
It is necessary to understand how long the Al_2O_3 liftoff process must be to remove or at least mitigate these residues. For that end, a number of structures, both individual and in crossbar configurations, were inspected at specific points during the process, and the evolution of the residues registered. The SEM images are shown in Figs. 4.31 and 4.32.

We can see that after 14 hours the liftoff residues are still quite pronounced, mainly around the corners of the bottom electrode. Continuing the process for a total of 20.5 hours results in some improvements, as some parts of these structures continue to break off or disappear completely. After 33 hours we get diminishing returns by extending the procedure, as the defects present in the previous



(a) (b) (c)

Figure 4.31: (**F3N3**) SEM observation of 5×5 µm^2 devices after incremental liftoff periods; a): 14 hours; b): 20.5 hours; c): 33 hours.



(a) (b) (c)

Figure 4.32: (**F3N3**) SEM observation of 10×10 µm^2 devices after incremental liftoff periods; a): 14 hours; b): 20.5 hours; c): 33 hours.

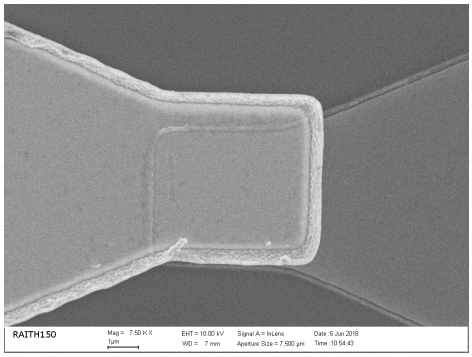
observation do not seem to degrade further.

We conclude that, mainly due to the large thickness of the deposited oxide, the liftoff is incomplete even after a very long time, and some residue remains. This means that the ultrasound bath with temperature is not sufficient to completely remove these structures. Other methods, such as chemical-mechanical polishing (CMP) or the already mentioned use of negative photoresist with an undercut profile would be more adequate to that end. On the other hand, the transition between the oxide and the bottom electrode appears even, without a large step between the two regions. We can thus attribute the significant improvement on device robustness partly on the more thorough residue removal along the edge of the bottom electrode, although some devices are still compromised by their presence.

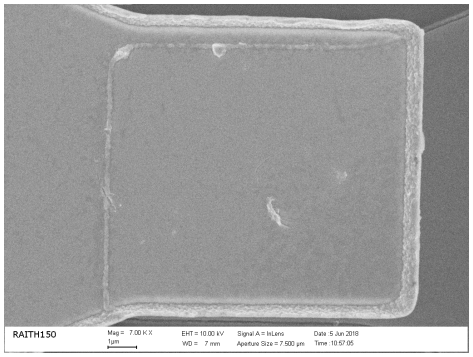
Another observation was performed after finishing the process, shown in Figs. 4.33-4.35.

We can see that the sidewall profile of the second level is considerably improved by the predevelopment step. Even though the individual devices in Fig. 4.33 have a slight misalignment between the two levels, it is not critical, and the issues of film peeling in the previous sample no longer happen. The contour of the junction/top electrode contact appears rougher in the crossbar devices depicted in Fig. 4.34. We thus conclude that the photoresist profile optimization still presents room for improvement.

The failure after a single transition in several devices indicates that structural issues, however mitigated, are still present. The 5×5 µm^2 junction in Fig. 4.35a presents a visible ridge along the bottom/top intersection, likely due to a sharp transition or liftoff residues, indicating that this remains a critical region.

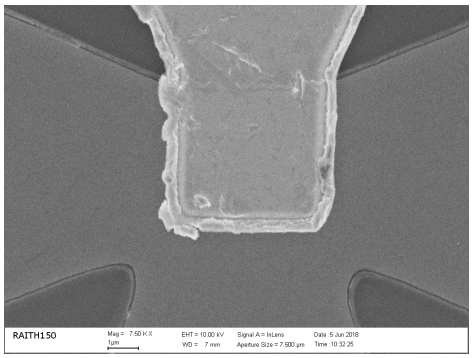


(a) 5×5 µm^2 individual junction.

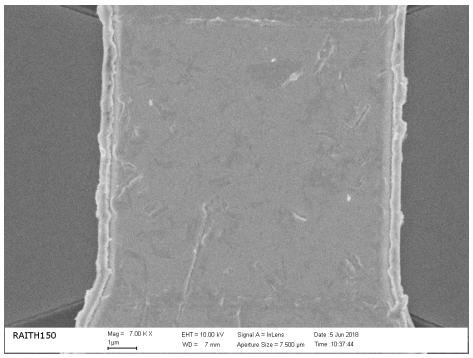


(b) 10×10 µm^2 individual junction.

Figure 4.33: (**F3N3**) SEM observation of 5×5 µm^2 and 10×10 µm^2 unmeasured individual devices.

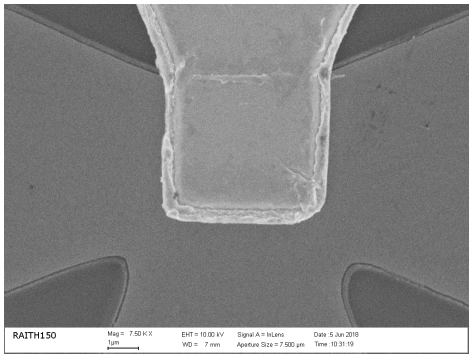


(a) 5×5 µm^2 junction in single row-multiple columns array.

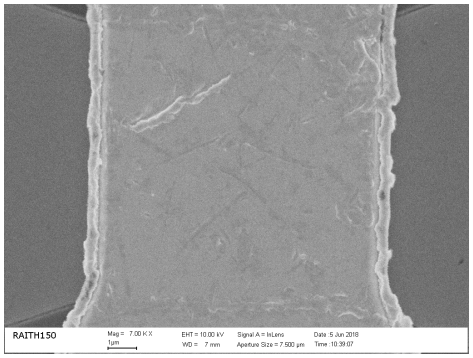


(b) 10×10 µm^2 junction in multiple rows-multiple columns array.

Figure 4.34: (**F3N3**) SEM observation of 5×5 µm^2 and 10×10 µm^2 unmeasured crossbar devices.



(a) 5×5 µm^2 junction in single row-multiple columns array (after first transition).



(b) 10×10 µm^2 junction in multiple rows-multiple columns array (after first transition).

Figure 4.35: (**F3N3**) SEM observation of 5×5 µm^2 and 10×10 µm^2 crossbar devices after measurement-induced failure.

Chapter 5

Conclusions

New computation paradigms are being developed to address the fundamental limitations of traditional, silicon-based integrated circuits. One such alternative is the so-called neuromorphic computation, in which the electric behavior and relationship between the fundamental elements of the architecture mimics those of biological neural tissue. As such, novel ways of implementing these artificial neural networks currently comprise a very active research field.

This thesis focused on the development of magnesium oxide-based memristive structures, in individual and crossbar array configurations. MgO, like an ensemble of other oxides and in films of appropriately small thickness, exhibits resistive switching. This is the property of changing between two or more resistance states in a non-volatile and reversible manner, and is also the main hallmark of a memristor. To that end, several material characterization and process optimization steps were undertook, using a Pt/MgO/Ta/Ru thin film stack.

The resistivity of the top electrode films, ruthenium and tantalum, respectively with thicknesses 293 $\pm$ 48 Å and 337 $\pm$ 34 Å, was determined to be 48.9 $\pm$ 5.8 and 174.8 $\pm$ 17.9 $\mu\Omega$·cm, respectively. The MgO ion beam etching rate in Nordiko 3600 was also determined using the standard and an iterative method, and it was found to be, respectively for these two methods, 0.76 $\pm$ 0.09 Å/s and 0.71 $\pm$ 0.06 Å/s for a 60º pan angle and 0.93 $\pm$ 0.03 Å/s and 0.97 $\pm$ 0.09 Å/s for a 30º pan angle. X-ray diffraction analysis of MgO, Ta and Ru revealed highly textured materials with a single highly preferred crystallographic orientation, respectively and using Miller indices notation, $\{2\ 0\ 0\}$, $\{1\ 1\ 0\}$ and $\{1\ 0\ 1\}$, which correspond to average interplanar distances of 2.08 Å, 2.61 Å and 2.11 Å.

Efforts to minimize platinum redeposition in the pillar sidewalls were also done, by optimizing the etching conditions in the pillar definition, using only 60º or 30º pan angles or a combination of both. However, the etched thicknesses across all samples were much lower than the expected values, and so the electric results were inconclusive. Even so, it was found empirically that etching the top electrode layers and most of the MgO film (70%) at 60º and the remainder of MgO with a 30 Å overetch at 30º yielded best results. No apparent short-circuits due to redeposition were found for large round test pillars (100-300 µm in diameter) defined by a single lithography level.

Two different fabrication processes were implemented. In the first, the MIM junction is defined by ion

beam etching and the sidewalls are passivated with aluminium oxide, before defining the bottom and top electrodes. In the second process, the bottom electrode is defined first and aluminium oxide is used to level the sample surface; the junction is then defined by depositing the MgO, Ta and Ru films in a precise overlap with the bottom electrode. In both processes several junction areas were defined, from 3×3 μm^2 up to 100×100 μm^2.

The first fabrication method did not have an ideal yield for patterning of individual devices. Around 60% of individual devices did not show any resistive switching behavior. Others presented a poor endurance during the measurement process, with around 33% of devices lasting only for one or two complete Set-Reset cycles before ceasing operation. Larger areas seem to be more resilient to testing, since 8% of tested devices, with 60×60 μm^2, 80×80 μm^2 and 100×100 μm^2 areas lasted between 3 and 10 full cycles. Two 100×100 μm^2 devices have exhibited a large number of Set-Reset cycles (~ 80), during which a clear separation of the ON and OFF states was observed, with an average R_{OFF}/R_{ON} ratio of about 10^2-10^3. The spread of V_{Set} voltages was larger than V_{Reset} values in both devices, with a range of 2 V to 18 V in one and 2 V to 8 V in the other; V_{Reset} was stable in both, varying between 0 and -3 V.

Crossbar arrays patterned with this process fared significantly worse. Out of 44 measured devices only 6 showed a very limited ability to perform resistive switching, lasting for one or two cycles. This leads to the conclusion that, as it stands, the first fabrication process is not adequate for the construction of these memristive devices in array configurations.

The first iteration of the second process did not bring significant improvements in comparison with the former method. None of the individual devices tested showed RS; only a limited number of 10×10 μm^2 crossbar junctions did so. However, their endurance remained poor.

SEM observations uncovered the same critical issue in both processes. Liftoff residues originating from the first passivating and leveling oxides, respectively for the first and second processes, resulted in very sharp protuberances that affect the topography of the films deposited on top. Such structures provoke a local thinning of the top electrode and metallization films. This, due to the large currents sometimes needed to operate the devices, exacerbates electromigration phenomena near those regions. Thus, during electric testing, successive voltage sweeps cause progressive degradation of the stack and ultimately lead to film rupturing and device failure. Other problems, such as badly defined intersections between top and bottom electrodes and a sloped photoresist profile, were also identified.

These issues were mitigated in the following iteration of the second process. The metallization layer thickness was increased from 1000 Å to 6000 Å to better handle electromigration. The liftoff step after the leveling oxide deposition was prolonged, up to a total of 33 hours, to remove residues to the biggest possible extent. A predevelopment step was also included in the second level definition to verticalize the photoresist walls and thus facilitate liftoff.

The above measures translated in a marked improvement in the yield of the process and the endurance of the memristive devices. All individual junctions measured have exhibited complete RS cycles, lasting between 3 and 10 and more than 11 cycles. Regarding the crossbar configurations, the improvements are more limited (100% of 5×5 μm^2, 94 % of 10×10 μm^2 and 53% of 100×100 μm^2 measured devices do not show any switching). However, for the devices that do show RS, the endurance is

better than previously, with 4 out of 17 100×100 μm^2 devices showing more than 11 full cycles without electric failure.

In many-cycles switching, the V_{Set} and V_{Reset} values of the two studied devices have low spread, mostly varying between 2 V and 5 V and between -0.2 V and -6 V with the number of cycles. The R_{OFF}/R_{ON} ratio is also stable throughout the measurement procedure, around 10^2.

In conclusion, despite shortcomings in the fabrication process, these results are very promising. Resistive switching has been shown in crossbar arrays of memristors using the Pt/MgO/Ta/Ru stack and developed with the tools available at INESC-MN. They present a good basis for future implementations of artificial neural networks. Other applications, such as resistive random access memories, are also possible to achieve with the devices studied in this work.

5.1 Future work

Electric characterization

Other characterization methods are useful to understand the behavior of the device under different requirements, such as unipolar measurements and pulsed measurements instead of continuous sweeps. The influence of the current compliance in Set transitions in the Reset voltages and OFF state resistances is also relevant.

Fabrication process

The liftoff residues present in the processes studied in this work remain a critical issue for yield and device reliability. Other techniques than those used here, aiming to fully remove these unwanted structures, may be more suitable, such as chemical-mechanical polishing or negative photoresists with undercut profiles. Atomic force microscopy may also be very useful to determine the step between the bottom electrode and the surrounding leveling oxide, in order to fine-tune the thickness of oxide necessary, as well as the average height of the liftoff residues. Cross-sectional SEM is also a very useful tool to directly observe the material hierarchy in the junction region. It is then possible to check for the presence of contaminants or defects introduced at various points in the fabrication process may hinder or prevent device operation.

Stack materials

Other thin film stacks may be used, such as for instance two active electrodes (Ta/MgO/Ta), to determine the influence of the stack composition in the electric response of the device. A quantification of the influence of the junction area on the electric parameters is also necessary.

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Appendix A

Runsheets

A.1 First process runsheet

Run Sheet – Memristors

Responsible: Tomás Martins **Sample ID:** N3MA3

Process Start: 28 / 2 / 18 **Process Finish:** 15 / 3 / 18

STEP 1: Stack deposition *28/2/18*

Machine: N2000

Deposition Conditions:

Run # 2068 **Seq:** MgO_IFIMUP

Deposition rates: MgO = 0.093 Å/s; Ta = 0.648 Å/s; Ru = 1 Å/s

Stack: MgO 300 Å/ Ta 200 Å/ Ru 200 Å

Nominal thickness: 700 Å

Measured thickness: 707 +- 29 Å

Notes: Include calibration sample to measure deposited thickness on profilometer.

STEP 2: 1st lithography – Junction definition (L1) *1/3/18*

Machine: N2000

1.1 Vapor Prime 30 min (Recipe – 0)

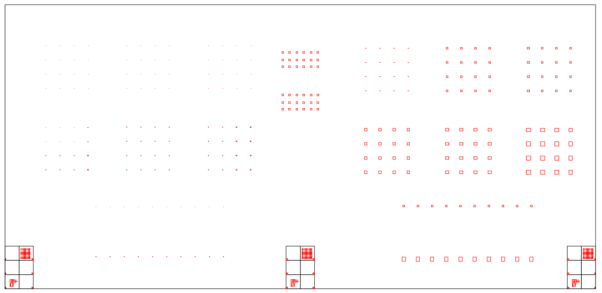
1.2 Coat 1.5 µm Photoresist (Recipe 6/2)

1.3 Lithography

Map: IFIMUP_M **Mask:** IFIMUP_Network3_Junc (\h3 - INVERTED)
Energy: 75% **Focus:** +35
Power: 100 mW
 # Dies: 2
Die dimensions: [X: 16700; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 200, 200 µm

1.4 Develop (Recipe 6/2): 40s

AutoCAD Mask :



Left:
Junction area (left to right, top to bottom):
3x3, 4x4, 5x5
6x6, 8x8, 10x10 um2
Bottom first row : 5x5 um2
Bottom second row : 10x10 um2

Right:
Junction area (left to right, top to bottom):
20x20, 40x40, 50x50,
60x60, 80x80, 100x100 um2
Bottom first row : 50x50 um2
Bottom second row : 100x100 um2

Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

STEP 3: 1st etch – Junction definition *2/3/18_*

Machine: Nordiko 3600

Total thickness to etch: (400 + 250 Å) @ 60º + (50 + 60 Å) @ 30º (20% MgO overetch)

Etch rates: Top @ 60º: 1.05 Å/s, MgO @ 60º: 0.76 Å/s, MgO @ 30º: 0.93 Å/s

Batch recipe: etch junction

Wafer recipe: etch junction first

Nominal thickness: 760 Å

Measured thickness: 725 +- 54 Å

Assist gun		Power (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flux (sccm)
Set values		190	735	105	350	-	11
Read values	**60º**	201	724.3	104.2	344.8	2.3	10.2
	30º						

Note:

Remove resist top left corner carefully with acetone in cotton swab to expose full stack; measure step to etched area.

STEP 4: Insulating layer deposition – Al2O3 *2-5/3/18*

Machine: UHV2

Nominal thickness: 1st etch thickness + 10% (≈ 850 Å)

Measured thickness:

Al2O3 thickness	Deposition	Ar gas flow	Pressure	Power Source
850 Å	65 min	45.2 sccm	2.1 mTorr	199 W

Note:

Include Si calibration sample to measure thickness and refractive index (ellipsometer, n = 1.46).

IMPORTANT: Include original wafer Ti/Pt calibration sample (sample S1) to calibrate thickness (ink lines), and to use stack Ti/Pt/Al2O3 on 2nd (step 7) and 3rd (step 10) etch calibration!

STEP 5: Lift-off *5/3/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Start time: 12:37 **Stop time:** 18:53

Note:

CRITICAL STEP: Pillars need to be clean of Microstrip! Perform optical inspection on microscope and measurements on profilometer (test structures).

STEP 6: 2nd lithography – Bottom electrode definition (L2) *6/3/18*

Machine: DWL

1.1 Vapor Prime 30 min (Recipe – 0)

1.2 Coat 1.5 µm Photoresist (Recipe 6/2)

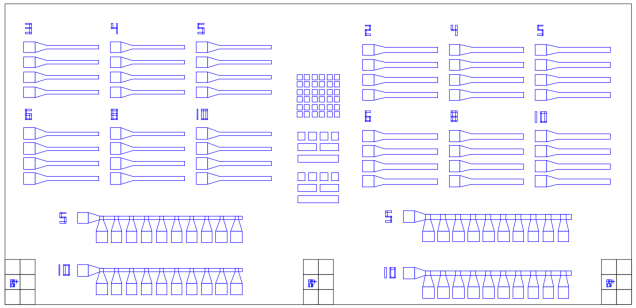
1.3 Lithography

Map: IFIMUP_M **Mask:** IFIMUP_Network3_Bot (\h3 - INVERTED)

Energy: 80% **Focus:** +35
Power: 120 mW
 # Dies: 2
Die dimensions: [X: 16700; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 200, 600 µm

1.4 Develop (Recipe 6/2)

AutoCAD Mask :



Left
Pad area: 300x300
Track width: 100

Right
Pad area: 200x200
Track width: 140

Test structures
Top squares: 140x140
Middle and bottom squares: 200x200
Middle rectangles: 200x500
Bottom rectangle: 200x1100

Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

STEP 7: 2nd etch – Bottom electrode definition *6/3/18*

Machine: Nordiko 3600

Total thickness to etch: Al2O3 layer thickness + 1750 Å (Ti 250 /Pt 1500) @ 45 deg

Batch recipe: etch junction

Wafer recipe: etch junction stack all 45 deg

Nominal thickness: ≈ 850 + 1750 = 2600 Å

Measured thickness:

Assist gun		Power (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flux (sccm)
Set values		190	735	105	350	-	11
Read values	45º	202.0	724.3	104.5	344.8	2.3	10.2

Note:

IMPORTANT: Include sample S1 with ink lines for etch thickness calibration.

Measure etched thickness on profilometer.

Check if bottom layer was etched: background must look like oxide and must not conduct current (test with multimeter).

STEP 8: Resist strip *7/3/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Start time: 11:27 **Stop time:** 12:10

STEP 9: 3rd lithography – Via opening to bottom electrode pads (L3) *7/3/18*

Machine: DWL

1.1 Vapor Prime 30 min (Recipe – 0)

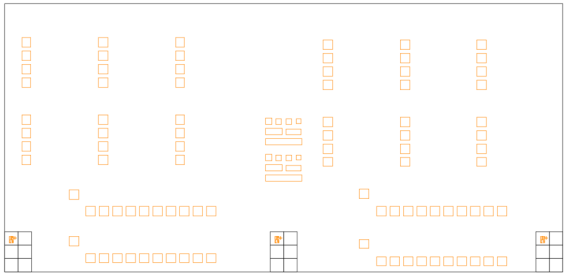
1.2 Coat 1.5 μm Photoresist (Recipe 6/2)

1.3 Lithography

Map: IFIMUP_M **Mask:** IFIMUP_Network3_Via1 (\h3 – NON-INVERTED)
Energy: 80% **Focus: +35**
Power: 120 mW
 # Dies: 2
Die dimensions: [X: 16700; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 200, 1000 µm

1.4 Develop (Recipe 6/2)

AutoCAD Mask :



Left and right
Pad area: 280x280 um2

Test structures
Squares: 190x190, 180x180, 160x160, 140x140
Middle rectangles: 190x490
Bottom rectangle: 190x1090

Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

STEP 10: 3rd etch – Via opening to bottom electrode pads *7/3/18*

Machine: Nordiko 3600

Total thickness to etch: Al2O3 layer thickness +10% overetch @ 45 deg

Batch recipe: etch junction

Wafer recipe: etch junction stack all 45 deg

Nominal thickness: ≈ 850 + 10% Å

Measured thickness: 885 +- 33 Å

Assist gun		Power (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flux (sccm)
Set values		190	735	105	350	-	11
Read values	**45º**	202.0	724.0	104.1	344.8	2.2	10.2

Note:

IMPORTANT: Include sample S1 using ink lines from 2nd etch for etch thickness calibration.

Check if open area looks like Pt (bright!)

Check for electric contact using 2-probe setup in characterization room (test structures).

Measure etched thickness after resist strip in profilometer.

STEP 11: Resist strip *8/3/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Start time: 15:40 **Stop time:** 18:00

STEP 12: Insulating layer deposition – SiO2 *12/3/18*

Machine: Alcatel/Electrotech

Nominal thickness: 1750 + 300 + 400 = 2500 Å

Measured thickness:

SiO2 thickness	Deposition	Ar gas flow	Pressure	Power Source
2500 Å	100 min	20 sccm	1.76 mTorr	100 W

Note:

Include Si calibration sample to measure thickness and refractive index (ellipsometer, n = 1.46).

IMPORTANT: Include original wafer Ti/Pt calibration sample to calibrate thickness (ink lines) and to use stack Ti/Pt/SiO2 on 4th etch calibration!

STEP 13: 4th lithography – SiO2 reactive-ion etching (L4) *14/3/18*

Machine: DWL

1.1 Vapor Prime 30 min (Recipe – 0)

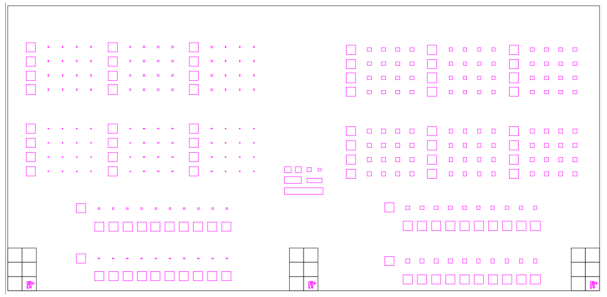
1.2 Coat 1.5 μm Photoresist (Recipe 6/2)

1.3 Lithography

Map: IFIMUP_M **Mask:** IFIMUP_Network3_Via2 (\h3 – NON-INVERTED)
Energy: 80% **Focus:** +35
Power: 120 mW
 # Dies: 2
Die dimensions: [X: 16700; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 600, 200 µm

1.4 Develop (Recipe 6/2)

AutoCAD Mask :



Left
Pad area: 260x260
Pillar area: 35x35

Right
Pad area: 260x260
Pillar area: 110x110

Test structures
Squares: 180x180, 160x160, 120x120, 80x80
Middle rectangles: 190x480
Bottom rectangle: 190x1080

Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

STEP 14: 4th etch – SiO2 reactive-ion etching *14/3/18*

Machine: LAM

Total thickness to etch: SiO2 layer thickness

Recipe: low power no O2

Nominal thickness: ≈ 2500 Å

Measured thickness:

Assist gun	Power (W)	WAP	Ar flux (sccm)	CF4 flux (sccm)	Clamp pressure (Torr)	Clamp flux (sccm)	Etch time (s)
Set values	100	-	200	100	14	-	-
Read values	102.3	177.2	200.7	100.0	14.2	32.1	450

Note:

Check if open area looks like Pt (bright!)

Check for electric contact using 2-probe setup in characterization room (test structures).

Measure etched thickness after resist strip in profilometer.

STEP 15: Resist strip *14/3/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Start time: 18:35 **Stop time: 19:45**

STEP 16: 5th lithography – Top contact definition (L5) *15/3/18*

Machine: DWL

1.1 Vapor Prime 30 min (Recipe – 0)

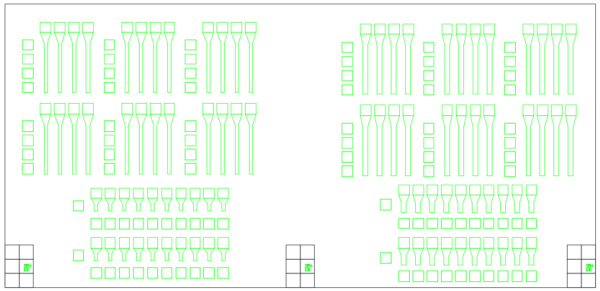
1.2 Coat 1.5 μm Photoresist (Recipe 6/2)

1.3 Lithography

Map: IFIMUP_M **Mask:** IFIMUP_Network3_Top (\h3 – NON-INVERTED)
Energy: 80% **Focus:** +35
Power: 120 mW
 # Dies: 2
Die dimensions: [X: 16700; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 600, 600 µm

1.4 Develop (Recipe 6/2)

AutoCAD Mask :



Left
Pad area: 300x300
Track width: 100x100

Right
Pad area: 300x300
Track width: 140x140

Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

STEP 17: Top contact definition *15/3/18*

Machine: Nordiko 7000

Sequence: Metalization

Run: 20838

Steps:

Mod 4 -f.1: (**AlSiCu deposition**, 3000 Å, 80 s) P = 2KW, p = 3mTorr, 50 sccm Ar

Mod 3-f.19: (**TiWN$_2$ deposition,** 150 Å, 27 s) P = 0.5 kW, p = 3mTorr, 50 sccm Ar + 10 sccm N$_2$

Read values: 2.00 kW/390 V/5.12 A/50.1 sccm/3.0 mTorr
0.50 kW/428 V/1.18 A/49.8 sccm/3.3 mTorr

STEP 18: Lift-off *15/3/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Start time: 17:05 **Stop time: 18:10**

A.2 Second process runsheet

Run Sheet – Memristors

Responsible: Tomás Martins **Sample ID:** F3N3

Process Start: 8/5/18 **Process Finish:** 30/5/18

STEP 1: 1st lithography – Bottom contact definition (L1) *8/5/18*

Machine: N2000

1.1 Vapor Prime 30 min (Recipe – 0)

1.2 Coat 1.5 µm Photoresist (Recipe 6/2)

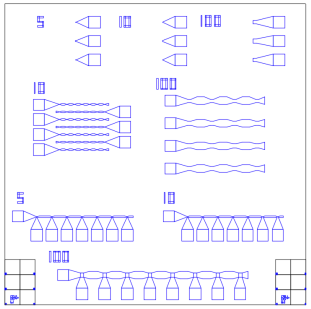
1.3 Pre-development 20 seconds (Recipe 6/2 – MANUAL 2nd station)

1.4 Lithography

Map: 2x2 **Mask:** IFIMUP_Networkz3_Bot (\h3 - INVERTED)
Energy: 70% **Focus:** +35
Power: 100 mW
 # Dies: 4
Die dimensions: [X: 8000; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 200, 200 µm

1.5 Develop (Recipe 6/2)

AutoCAD Mask :



Upper individual:
Junction area (left to right): 5x5, 10x10, 100x100 um2

Middle grids:
7 by 7 array of 10x10 um2 junctions
4 by 4 array of 100x100 um2 junctions

Bottom rows:
1 by 7 array of 5x5 um2 junctions
1 by 7 array of 10x10 um2 junctions
1 by 8 array of 100x100 um2 junctions

Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

STEP 2: 1st etch – Bottom electrode definition *8/5/18*

Machine: Nordiko 3600

Total thickness to etch: 1750 Å Ti/Pt layer + 50 Å overetch @ 45º

Etch rates: Pt @ 45º: 1.1 Å/s -> Etch time = 1650 s (8x200s + 50 s)

Batch recipe: etch junction

Wafer recipe: etch junction stack all 45 deg + clean assist gun

Nominal thickness: 1800 Å

Measured thickness:

Assist gun		Power (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flux (sccm)
Set values		190	735	105	350	-	11
Read values	**45º**	204	724.5	104.3	345.0	2.3	11.2

Note:

Remove resist top left corner carefully with acetone in cotton swab to expose full stack; measure step to etched area.

STEP 3: Insulating layer deposition – Al2O3 *9/5/18*

Machine: UHV2

Nominal thickness: 1st etch thickness (= 1800 Å)

Measured thickness:

Al2O3 thickness	**Deposition time**	**Ar gas flow**	**Pressure**	**Power Source**
1800 Å	3h 38min	45.1 sccm	2.5 mTorr	200 W

Note:

Include Si calibration sample to measure thickness and refractive index (ellipsometer, n = 1.6).

STEP 4: Lift-off *9-17/5/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Liftoff period:

9/5: 16:47- Microstrip change @ 18:40

10/5: 11:15-13:45 / 14:45-18:10

14/5: 11:15-17:45

16/5: 11:00-19:15

17/5: 14:05-18:25

Note:

Perform optical inspection on microscope and check for lift-off ears in bottom electrode border on profilometer.

STEP 5: 2nd lithography – Junction/top electrode definition (L2) *24/5/18*

Machine: DWL

1.1 Vapor Prime 30 min (Recipe – 0)

1.2 Coat 1.5 µm Photoresist (Recipe 6/2)

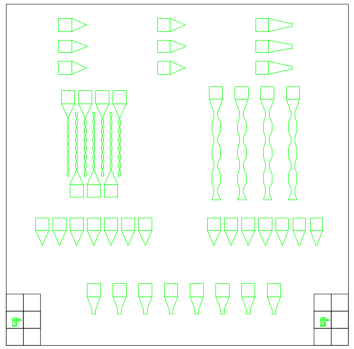
1.3 Pre-development 15 seconds (Recipe 6/2 – MANUAL 2nd station)

1.4 Lithography

Map: 2x2 **Mask:** IFIMUP_Networkz3_Top (\h3 – NON-INVERTED)
Energy: 100% (+20% than usual because of pre-development) **Focus:** +85
Power: 100 mW
 # Dies: 4
Die dimensions: [X: 8000; Y: 8000] µm
0, 0: 4000, 4000 µm (from bottom left corner)
Level alignment cross center: 200, 600 µm

1.5 Develop (Recipe 6/2)

AutoCAD Mask :



Note:

Check the feature size and shape under the optical microscope; check if resist is in expected areas.

Check the resist thickness using profilometer.

Very important to make sure resist has the correct profile!

STEP 6: Soft etch for junction/top deposition *24/5/18*

Machine: Nordiko 3600

Etch time: 30 s

Batch recipe: etch junction

Wafer recipe: soft etch @ 60º

Assist gun	Power (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flux (sccm)
Set values	190	735	105	350	-	11
Read values	208.0	724.8	104.5	345.2		

STEP 7: Junction/top deposition *24/5/18*

Machine: N2000

Deposition Conditions:

Run # 2216 **Seq:** MgO_IFIMUP

Stack: MgO 300 Å/ Ta 200 Å/ Ru 200 Å

Nominal thickness: 700 Å

Measured thickness:

Notes: Include calibration sample to measure deposited thickness on profilometer.

STEP 8: Soft etch for metalization *30/5/18*

Machine: Nordiko 3600

Etch time: 30 s

Batch recipe: etch junction

Wafer recipe: soft etch @ 60º

Assist gun	Power (W)	V+ (V)	I+ (mA)	V- (V)	I- (mA)	Ar flux (sccm)
Set values	190	735	105	350	-	11
Read values	199	724.5	104.3	345.0	2.3	10.2

STEP 9: Metallization *30/5/18*

Machine: Alcatel

Nominal thickness: [Cr 50/ Au 3000] x 2 = 6100 Å

Material	**Deposition time**	**Ar gas flow**	**Pressure**	**Power Source**
Cr	1 min 15 s	-	1.76 mTorr	20 W DC
Au	48 min	-	1.76 mTorr	20 W RF

STEP 10: Lift-off *30/5/18*

Conditions: Microstrip 3001 + Temperature : 60ºC + Ultrasounds

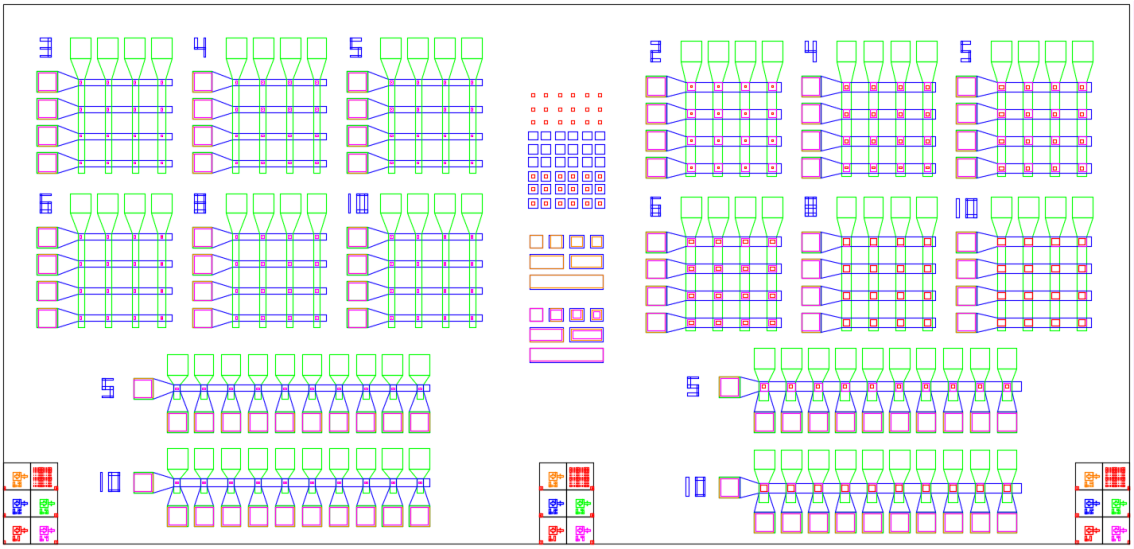
Cleaning: IPA rinse / DI water rinse / Dry with compressed air gun

Start time: 15:23 **Stop time:** 19:10 Microstrip change @ 16:33

Appendix B

AutoCAD masks

N3MA3:



F3N3: