Ultra Low Power Clock

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Abstract—In this work, a desk clock was designed. A method for measuring ultra-low, nanoampere currents is presented, as well as the complete mixed-signal design process of integrated circuits. The work consists of a demonstrator of features of Silicongate's real-time clock (RTC) SGC22300. The demonstrator is a mixed-signal circuit, working as a digital clock, interfacing the RTC and one liquid crystal display (LCD), capable of showing the current time. The complete RTC circuit, the user interface and the LCD driver were designed using GlobalFoundries' 22FDX®, employing **22 nm** Fully-Depleted Silicon-On-Insulator (FD-SOI) technology.

With the purpose of characterizing the LCD, a measurement setup was designed. The measurement method is relevant for circuits developed with Internet of Things (IoT) in mind, as such applications require increasingly lower currents to be measured, in the order of the pico or nanoampere. The method uses a platform with low-cost, off-the-shelf components and allows common measurement equipment, not adapted for ultra-low currents, to be used. An in-depth analysis of the sources of error is conducted, allowing accurate prediction of the maximum expected error of any measurement and optimization of parameters of the measurement to achieve a specific accuracy. Experimental results from thousands of measurements validate the operation at different supply voltages, in a current range of 3 orders of magnitude, starting at 25 nA, with achievable error of less than **1 %** in any scenario. Special design techniques adapted to ultra-low power circuits are demonstrated.

Index Terms—Ultra-low current measurement, mixed-signal design, LCD driver, frequency monitor.

I. Motivation

With the expected increase of the IoT market, there is a demand to develop technologies that enable products to be more energy efficient, thus reducing their physical size and allowing their batteries to last longer.

One of the reasons why achieving very low power is possible is the fact that IoT applications can perform tasks periodically; using RTCs to wake parts of the system at regular intervals, while consuming very low energy. It is fair to say that ultra-low power RTCs enable ultra-low power applications. RTCs requiring currents of less than 50 nA already exist, like Silicongate's SGC22300. Such currents are so small that a CR2032 battery could, in theory, last for more than 4 centuries[1], if ageing and self-discharge were not a problem.

[1] Assuming a typical capacity of 200 mAh and ignoring ageing and self-discharge. By accounting for the latter factors, the battery life is limited by the lifetime of the battery, which can range from 10 years to a few decades.

Silicongate Lda would like to have a demonstrator of the RTC that could be used as a marketing gift. The initial specifications that defined this work targeted the design of a table clock with Silicongate's existing RTC, and the new designed of a user interface and a LCD driver.

GlobalFoundries provided the possibility of prototyping a test chip in 22FDX® and this was the technology used in the project.

When low currents are involved, experimentally characterizing circuits becomes a challenge, since measurement equipment specially designed for the purpose (and not commonly available) is required. Measuring ultra-low currents is becoming more common as the industry evolves to increasingly lower powered devices. Simple methods for measuring currents, such as using a shunt resistor, are especially susceptible to noise and other sources of uncertainty and usually produce poor results when dealing with nanoampere currents.

II. Objectives

The aim of this work is the development of a fully working digital clock, incorporating the SGC22300, capable of demonstrating its low power capabilities, and development of a method to fully characterize currents of such low magnitudes. The work can be divided in two main parts — demonstrator circuit and current measurement — each with its set of objectives.

The demonstrator consists of an application-specific integrated circuit (ASIC), containing a digital circuit, which interfaces directly with the RTC, and an analog circuit that controls an LCD, as illustrated in Figure 1. The digital part is developed using a hardware description language (HDL), Verilog, making it synthesizable in both the target architecture and in programmable logic devices. This makes the developed code testable on a physical medium, a Complex Programmable Logic Device (CPLD), serving as an extra verification step. The analog circuit is composed of two distinct parts: a protection circuit, which monitors the clock from the RTC and protects the LCD in case of failure; and the drivers, which produce adequate waveforms for driving the display.

Validating the current consumption corresponds to a crucial step in the development of ultra-low power devices. Therefore, a measurement method using an inexpensive

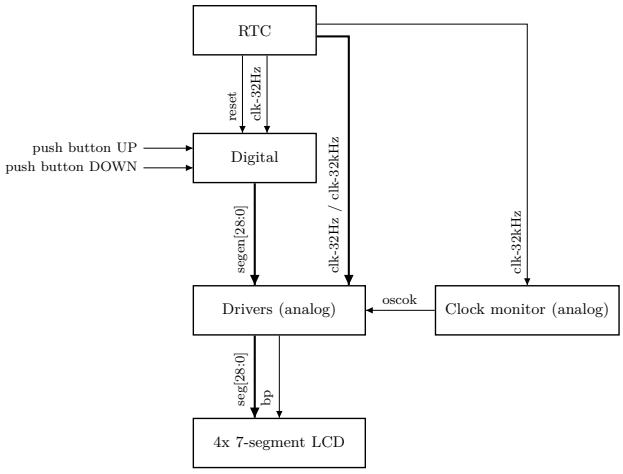

Fig. 1. Functional diagram of the demonstrator.

setup, while guaranteeing a predetermined accuracy, is of great value. The goal of this work is the development of an alternative method to using conventional transimpedance approaches (shunt resistors), while keeping the measurement setup simple and inexpensive.

In summary, the objectives for this thesis work are:

- Development of a demonstrator, consisting of a fully working digital clock, designed in GlobalFoundries' 22FDX® 22 nm FD-SOI process.
  - Development of the digital circuit, using HDL.
  - Validate the digital circuit both by simulation and by emulation on a CPLD.
  - Design LCD driver circuit.
  - Design clock fail detection circuit.
- Present an improved method for measuring nanoampere currents using an inexpensive setup and guaranteed accuracy.
  - Propose an alternative method to transimpedance approaches.
  - Analyze sources of error and develop model for predicting accuracy of measurements.
  - Validate method and accuracy model experimentally.
  - Validate consumption of blocks of the demonstrator already developed.

In this paper, the most innovative parts of the developed work are presented, namely, the proposed method for measuring ultra-low currents.

III. Ultra-low current measurement

Most current measurement methods can be divided in two main categories - the ones based on magnetic fields produced by some charge flow and the ones that measure a voltage drop across a shunt resistor [1]. For very low current measurements, the latter are used, since the resulting magnetic fields are too weak to be measured by ordinary equipment.

When using a resistor for measuring fast varying signals, the impedance variation at higher frequencies (caused by parasitic inductances or capacitances) must be considered and might become a limiting factor. The resistor value must be determined according to the Ohm's law so that the voltage drop across its terminals is high enough to be in the correct range of the detector and low enough to not interfere with the device under test (DUT). However, the lower the current, the larger the required resistor. By making the shunt resistor larger, the measurement process is more susceptible to: (a) thermal noise, whose RMS value is given by Equation (1), and (b) parasitic elements introduced by the measurement equipment.

$$v_n = \sqrt{4k_B \cdot T \cdot R \cdot \Delta f} \tag{1}$$

The effect of parasitic elements can be minimized by using high impedance probes or active buffering circuits. However, when measuring low amplitude, fast varying current signals, the thermal noise might become an issue, due to the high bandwidth required in conjunction with large resistors.

Exploiting the idea of a switched capacitor topology, the circuit of Figure 2 is used to overcome the limitations of measurements using shunt resistors. The presented circuit allows the DUT to operate without any influence, by connecting it directly to the voltage supply through switches Q1 and Q2. Briefly opening the switch Q2, allows the current to be integrated during a precisely defined time interval, after which Q1 is opened, allowing the voltage in C_P to be held constant. The result of the integration manifests itself as a voltage drop in the terminals of C_P.

In this configuration, the capacitor eliminates the need of a high bandwidth oscilloscope. No active integrator is used; therefore, there is no bandwidth limitation introduced by operational amplifiers or other amplifier circuits. To measure the voltage in capacitors, inexpensive unity gain amplifiers can be connected to the floating nodes to allow voltmeters with relatively low input impedances to be used.

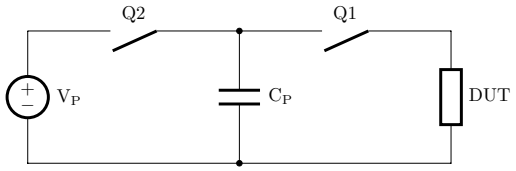

Fig. 2. Simplified experimental setup used to measure the current consumption.

Throughout this chapter, a review of the state of the art is first presented, followed by a more detailed description of how the measurement is performed and of the developed hardware for the measurement. The different contributions for errors in the measurement are later analyzed, with the purpose of creating a model for accurately predicting the expected maximum error of any measurement. Finally,

experimental results which prove the correctness of the proposed theory are presented, as well as a comparison between two types of capacitors and the case study measurement of the current of an LCD.

IV. State of the art

A similar circuit, called Fully Differential Frequency Converter [2], also exploits current integration to measure low currents. This approach uses operational amplifier integrators to integrate an input current during fixed time windows. Voltage comparators monitor when the integration value reaches a predefined threshold, signaling this event via an output pulse, and starting the integration of the symmetric of the input current instead, creating a close to a sawtooth waveform. During the integration time window, the number of output pulses is proportional to the current. This circuit allows a high dynamic range of current to be measured with great accuracy. However, it is susceptible to the propagation delays in the comparators, control logic, amplifier stages and switches. This problem is addressed by using extremely fast components throughout the circuit.

As opposed to the latter, the solution proposed in this work uses a simplified topology, which is not as susceptible to propagation delays. The use of common off-the-shelf components, with relaxed specifications, and hence lower costs, is its main advantage. By having the capacitor connected to the load via a switch, the behavior of the DUT might be affected by the voltage variation. However, an analysis of the errors introduced by this method shows that good accuracy can be guaranteed for voltage variations as low as a few millivolt.

In other applications, such as amperometry, which require measuring very small electric charges as result of chemical reactions, similar topologies provide good results, both in application-specific integrated circuits (ASICs) [3] and using discrete components on a printed circuit board (PCB) [4].

V. Current measurement using Delta-V of capacitors

The measurement is conducted as follows:

- The capacitor, the DUT and the reference voltage are connected, by closing switches Q1 and Q2. The DUT is allowed to operate normally for an indefinite amount of time until the measurement is performed.
- A measurement of the voltage in the capacitor is made and the switch Q2 is immediately opened. This initial voltage corresponds to v_i.
- After a Δt delay, denoted by charge integration time, Q1 is opened. A second voltage measurement, corresponding to v_f, is immediately triggered.

The current is calculated using the fundamental equation of current in a capacitor — eq. (2). Based on the values of the voltage in the capacitor C_P, measured before and after Δt, one can write the average current $\bar{i}$ supplied by C_P according to Equation (3). The voltage Δv was defined as $v_i - v_f$, so that the calculated current is positive when charges flows from the capacitor to the load.

$$i(t) = C_P \cdot \frac{dv(t)}{dt} \tag{2}$$

$$\bar{i} = C_P \cdot \frac{v_i - v_f}{\Delta t} = C_P \cdot \frac{\Delta v}{\Delta t} \tag{3}$$

A. Proposed implementation

The implementation of the proposed topology requires careful design, to deal with low currents and high impedance nodes. An equivalent diagram of the implemented circuit is depicted in Figure 3.

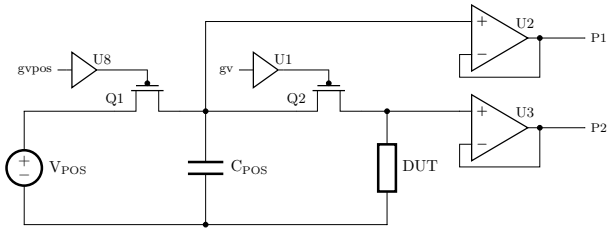

Fig. 3. Simplified experimental setup used to measure the current consumption.

When a measurement of the capacitor voltage is made, the measurement device must not significantly alter this voltage by changing the total charge in the capacitor. Any device will have a finite input impedance, and, therefore, will affect the voltage to some extent. This circuit is especially affected by this phenomenon, since it uses very-low-valued capacitors. Therefore, measurement devices with giga or teraohm equivalent input impedances are required, considering the order of magnitude of the currents being measured. This is achieved by connecting the capacitor and the low-impedance output node to unity-gain buffers (U2 and U3), implemented with operational amplifiers, with the required input impedance. The buffers isolate the sensitive nodes from the measurement devices.

Switches Q1 and Q2 are implemented using discrete MOSFETs, optimized for sample and hold circuits. Choosing the MOSFETs is crucial, since an arbitrary choice of devices can easily introduce undesired parasitic elements that render the circuit unusable. The required MOSFETs have particularly low parasitic capacitance and low leakage currents. The devices denoted by U1 and U8 are level shifters, which generate adequate voltages levels to drive the MOSFET gates.

Parasitic capacitances inject charge in C_P when the MOSFET turns on or off; thus, changing the voltage in the capacitor. Leakage currents also affect the voltage, by allowing charge to flow to or from the capacitor while the MOSFETs are turned off.

B. Printed circuit board

The PCB that was developed for the measurement is depicted in Figure 4. The board contains two capacitors for current measurement connected to two independent

voltage sources, one positive and one negative. Therefore, the circuit of Figure 3 is replicated twice in the schematic. Both voltages can be alternately applied to the DUT, allowing a rectangular waveform to be created. While this feature is relevant when measuring the current consumption of an LCD, the general case is studied instead, consisting of a direct implementation of the simplified circuit, since both circuits operate independently.

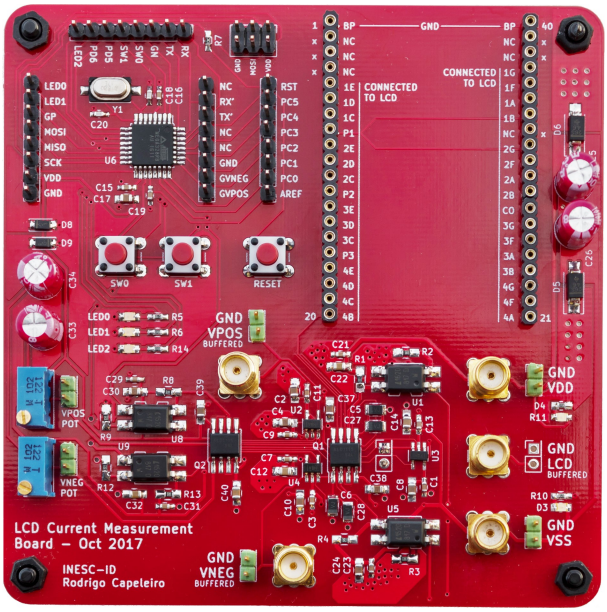

Fig. 4. PCB used for the current measurements.

The key components are the microcontroller, level shifters, MOSFETs, operational amplifiers and the capacitors. The microcontroller is responsible for generating the control signals for the MOSFETs and implements an RS232 interface. The level shifters are implemented with optocouplers for simplicity and reliability. They are the main source of propagation delays, which were measured to be approximately 17 µs. Although faster alternatives exist, the errors introduced by the level shifters do not compromise the accuracy of the results, even for charge integration times as low as 64 µs, as discussed later. The MOSFETs used in this application have low input capacitance (3 pF) and low drain leakage current (10 pA). The typical bias current of the selected operational amplifier is less than 1 pA and its input capacitance is less than 8 pF.

Known layout techniques for minimizing the leakage of the most sensitive traces on the PCB were implemented, such as surrounding high impedance nodes by guard rings at the same potential. Digital and fast switching signals were kept as far as possible from the sensitive traces and power and ground planes were selectively placed to avoid unnecessary parasitic capacitances.

VI. Error analysis

The measured current can be written as a function of multiple variables as:

$$\bar{i}(C_P, \Delta v, \Delta t) = C_P \cdot \frac{\Delta v}{\Delta t}, \tag{4}$$

of which the first order approximation via a Taylor series around $x_0 = (C_{P_0}, \Delta v_0, \Delta t_0)$ is:

$$\bar{i}(C_{P_0} + \epsilon_{c_P}, \Delta v_0 + \epsilon_{\Delta v}, \Delta t_0 + \epsilon_{\Delta t}) \approx \tag{5}$$
$$\approx \bar{i}(x_0) + \epsilon_{c_P} \frac{\partial \bar{i}}{\partial C_P}(x_0) + \epsilon_{\Delta v} \frac{\partial \bar{i}}{\partial \Delta v}(x_0) + \epsilon_{\Delta t} \frac{\partial \bar{i}}{\partial \Delta t}(x_0),$$

which is valid for small variations (errors) ϵ_{c_P}, $\epsilon_{\Delta v_0}$ and $\epsilon_{\Delta t}$ that affect the input variables. From Equation (5), one concludes that the error of the calculated $\bar{i}$ corresponds to the terms containing partial derivatives. The expression for the absolute error is:

$$\epsilon_i \approx \epsilon_{c_P} \frac{\partial \bar{i}}{\partial C_P}(x_0) + \epsilon_{\Delta v} \frac{\partial \bar{i}}{\partial \Delta v}(x_0) + \epsilon_{\Delta t} \frac{\partial \bar{i}}{\partial \Delta t}(x_0), \tag{6}$$

and the expression for the relative error, resulting from the calculation of the partial derivatives, is:

$$\eta_i = \left| \frac{\epsilon_i}{\bar{i}(x_0)} \right| \approx \left| \frac{\epsilon_{c_P}}{C_{P_0}} + \frac{\epsilon_{\Delta v}}{\Delta v_0} + \frac{\epsilon_{\Delta t}}{\Delta t_0} \right| \leq \eta_{c_p} + \eta_{\Delta v} + \eta_{\Delta t}. \tag{7}$$

Equation (7) establishes how a relative error in any of the variables affects the result. By analyzing this equation, it becomes evident that there are three contributions to the total error, which can be studied separately.

A. Voltage error

Assuming that the errors that affect the voltage measurements are random, the probabilistic distribution of the experimental values of Δv is a normal distribution, with mean value Δv_0.

If the same Δv measurement is performed repeatedly in the same conditions (same DUT, supply voltage and charge integration time), the standard deviation of the experimental results converges to the standard deviation, σ, of the normal distribution. In these circumstances, the probability of an experimental measurement of Δv being within 3 standard deviations of Δv_0 is $0.9973 \approx 1$. In other words, the probability of the experimental measurement of Δv being within 3σ of the true value of Δv is approximately 100 %. Therefore, it is fair to consider that:

$$|\epsilon_{\Delta v\text{-rand}}| \leq 3\sigma \quad \Leftrightarrow \quad \eta_{\Delta v\text{-rand}} \leq \frac{3\sigma}{\Delta v} = 3\sigma \cdot \frac{C_P}{\Delta t \cdot \bar{i}}. \tag{8}$$

In reality, the voltmeter will also introduce systematic errors (which affect the average value of the measurements), due to wrong calibration. This contribution is specified for any measurement equipment in its datasheet and must be accounted for, when determining the total error in Δv. One conservative formula for the total error is:

$$\epsilon_{\Delta v} \leq |\epsilon_{\Delta v\text{-rand}}| + |\epsilon_{\Delta v\text{-syst}}| \Leftrightarrow \tag{9}$$
$$\Leftrightarrow \eta_{\Delta v} \leq \eta_{\Delta v\text{-rand}} + \eta_{\Delta v\text{-syst}}.$$

B. Timing error

Three factors affect the charge integration time, Δt: turn-on and turn-off times of the switches, propagation delays of the level shifters and uncertainty of the control signals generated by the microcontroller.

The errors introduced by the microcontroller are negligible, since a precise crystal oscillator and hardware timers are used. The charge integration time is generated in 64 µs steps, while nanosecond errors are expected, due to the microcontroller uncertainty. Likewise, the turn-on and turn-off times of the MOSFET switches are orders of magnitude shorter than the charge integration time.

Regarding the propagation delays (t_P) of the level shifters, these are expected to be around 17 µs, exhibiting a strong dependence on working voltage. Despite being in the same order of magnitude of Δt, they are not expected to affect the result, due to the circuit topology. As mentioned in Section V, the switches Q1 and Q2 are opened sequentially: Q2 is open t_P after the microcontroller command, when the charge integration starts; Q1 is open t_P after the charge integration finishes. Therefore, with the proposed PCB implementation and measurement procedure, it is reasonable to assume:

$$\eta_{\Delta t} \approx 0. \tag{10}$$

C. Capacitance error

Although physically related to the actual value of the capacitor, the variable C_P in Equation (4) can be seen as a proportionality constant which relates a given $\frac{\Delta v}{\Delta t}$ ratio to an average current. In this sense, all the phenomena which affect the linearity of the method can be attributed to an error in C_P. These phenomena include:

- Uncertainty of the measured capacitance, $\eta_{c_p\text{-syst}}$.
- Leakage currents: when present, leakage currents cause charge losses in the capacitor, resulting in different values of Δv for the same $\bar{i}$, if the measurement conditions change.
- Dielectric absorption (DA), which is a well-known problem in sample and hold circuits, such as ADCs [5] or DRAMs [6]. DA manifests itself as a memory effect in the capacitor, causing its apparent capacitance to vary according to its initial charge, how fast it is discharged and how long after the integration period the voltage measurement is taken. A study of DA on different dielectrics conducted by Kuenen and Meijer [7] measured how much this phenomenon affects the apparent value of capacitors. The results showed that DA can be as high as 12.3 % for some dielectrics (or as low as 0.02 % in the most favorable case).
- Non-linearity of actual capacitance value, making the capacitor behave differently according to external factors such as ambient temperature, or, most commonly, bias voltage.

In summary, as with any measured quantity, the value of C_P will have an associated error, denoted by $\eta_{c_p\text{-syst}}$; the remaining phenomena cause the effective value of C_P to vary around its assumed value. Because the latter component refers to how linear the capacitor is under different measurement conditions, its associated error will be referred to as $\eta_{c_p\text{-lin}}$. According to these definitions, the error of relative error of C_P can be written as:

$$\eta_{c_p} = \eta_{c_p\text{-syst}} + \eta_{c_p\text{-lin}}. \tag{11}$$

The relevance of Equation (11) relies on the fact that every non-linearity that affects the measurement is covered by $\eta_{c_p\text{-lin}}$, and, more importantly, both contributions to η_{c_p} can be experimentally measured, as presented in Section VII.

D. Optimizing for a target accuracy

According to the error analysis that was performed, namely, the upper bounds for the error of Δv and C_P, a guaranteed accuracy[2] of the measured current can be determined. The accuracy is measured through the maximum relative error of a given measurement, denoted by k, which can be written as:

$$k = \eta_{c_p\text{-syst}} + \eta_{c_p\text{-lin}} + \eta_{\Delta v\text{-syst}} + 3\sigma \cdot \frac{C_P}{\Delta t \cdot \bar{i}}. \tag{12}$$

The latter equation assumes that C_P and its associated errors are calculated, prior to starting the measurements, and that σ is determined from a large set of measurement results. Based on these parameters, Equation (12) allows to determine the minimum Δt which guarantees the target accuracy k, according to a rough estimate of the current to be measured.

VII. Experimental results

A method for verifying the linearity of the measurement procedure and determining $\eta_{c_p\text{-lin}}$ is first presented. A second set of tests uses an automated setup, which generated 192320 measurements, allowing the validation of the proposed model for predicting the accuracy of the measurements. Finally, the proposed method is applied to the measurement of the current of the LCD which is used by the demonstrator.

A. Measuring linearity of tantalum capacitors

This test was performed in a first version of the measurement board, with tantalum capacitors, which were later replaced by polyester capacitors given that the latter are more stable. The results of this test allow the value of C_P to be experimentally determined, as well as $\eta_{c_p\text{-syst}}$, with which the accuracy of subsequent measurements can be predicted.

[2]The term "accuracy" refers to its ISO definition, combining both "trueness", or closeness of agreement between the arithmetic mean of a large number of test results and the true or accepted reference value, and "precision", which refers to the closeness of agreement between test results.

The DUT is a resistor, whose value is known, with a given tolerance. Let us consider the scenario of a resistor R, the DUT, in parallel a capacitor, C_P, which is precharged with some voltage and later allowed to discharge through the resistor. The voltage in the resistor, v_R, as the capacitor discharges from the initial voltage V_0, is expressed, as a function of time, as:

$$v_R(t) = V_0 \cdot e^{\frac{-t}{R \cdot C_P}}. \tag{13}$$

Using the notation introduced in Section V, the previous equation can be rewritten as Equation (14). In this equation, $v_i = v_R(0) = V_0$ represent the voltage precharged into the capacitor, and $v_f = v_R(\Delta t)$ represent the final voltage measured after Δt.

$$v_f = v_i \cdot e^{\frac{-\Delta t}{R \cdot C_P}}. \tag{14}$$

By repeating the measurement for series of discharge times (Δt_0, Δt_1, ... , Δt_n), and initial voltages $v_i[n]$, a series of estimated $C_P[n]$ values is obtained. Ideally, the same value of C_P is obtained in every measurement. However, if any of the phenomena listed in Section VI-C affects the measurement, v_f will not reflect solely the RC decay component and a shift in the values of $C_P[n]$ will be observed. Therefore, this test evaluates the linearity of the measurement circuit (given by $\eta_{c_p\text{-lin}}$) and it also allows to determine the value of C_P.

The above procedure was repeated for 3 initial voltages from 3 V to 5 V and 3 different loads — 100 kΩ, 1 MΩ and 2 MΩ. Figure 5 summarizes the measurements at 4 V, using a 2 MΩ resistive load. The convergence of the estimated values of capacitance to the nominal value, as the charge integration time increases, suggests that the equivalent series inductance (ESL) of the capacitor might be affecting the measurement. However, the time constant $\tau = L/R$ formed by the ESL ($\ll$ 1 µH) and the load resistor ($>$ 1 MΩ) is several orders of magnitude smaller ($\ll$ 1 ps) than Δt. Further experiments revealed that the capacitors had excessive leakage (compared to what is achievable with other dielectrics) and suffered from DA, resulting in inconsistent results between experiments. These factors explain the non-linearity that is observed in the graph.

The average capacitance value is 96.9 % of the typical value (4.4 µF) and the measured values of $C_P[n]$ vary as much as ±5 %. The uncertainty of the measured values of $C_P[n]$, $\eta_{c_p\text{-syst}}$, results from an analysis of the propagated uncertainties according to Equation (14) and was determined to be negligible, compared to $\eta_{c_p\text{-lin}} = 0.05$.

B. Measuring linearity of polyester capacitors

Polyester film capacitors have significantly lower leakage and lower dielectric absorption compared to tantalum capacitors. For this reason, they were used as an alternative to the latter. While the previous test method produces conclusive results with limited resources, it is laborious and not easily automatable.

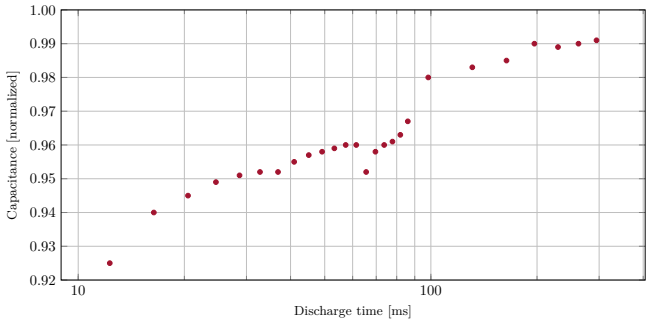

Fig. 5. Estimated values of C_P, based on measurements using a 2 MΩ resistor. A tantalum capacitor with 4.4 µF typical value was experimentally measured. The capacitor was initially charged with 4 V and discharged to successively lower voltages down to approximately 3.8 V.

This test consisted of charging the capacitor with a configurable voltage, imposing a current using a source meter and allowing the capacitor to discharge during Δt. By measuring v_i and v_f, all the results from this section and from Section VII-C were derived. The experimental validation consisted of 192 320 measurements, including 11 different test currents, spanning over 3 orders of magnitude, from 25 nA to 25.6 µA; 7 voltage levels, from 2 V to 5 V; and 119 values of Δt, logarithmically spaced between 64 µs and 1 s. Each permutation of these 3 variables was measured 32 times, to give a rough estimate of σ (standard deviation of observed Δv). The test setup is fully automated, consisting of:

- Source meter (Keithley 2611), in constant current mode, providing configurable loads.
- Multimeter (Keithley 2000), for measurement of Δv.
- Power supply (HP E3634A), for establishing the test voltage V_P.
- PC, controlling the instruments via GPIB and the measurement board via RS232 and logging the measurements.

For each individual measurement, the value of C_P is calculated. This value is the proportionality constant that translates the observed Δv to the true value of the current (imposed by the source meter). Since 32 measurements are taken for each test condition (imposed current, Δt and initial voltage), each set of 32 values of C_P can be averaged, to reduce the effect of random noise in the measurements.

Figure 6 depicts the calculated averages of 32 measurements of C_P, for which the observed standard deviation (normalized by the average) was less than 1 %. It must be noted that filtering out the measurements with high observed standard deviation is necessary since lower measured currents integrated during the shorter Δt result in Δv which are orders of magnitude smaller than the random noise (experimentally measured through σ),

therefore the calculated values of C_P are meaningless.

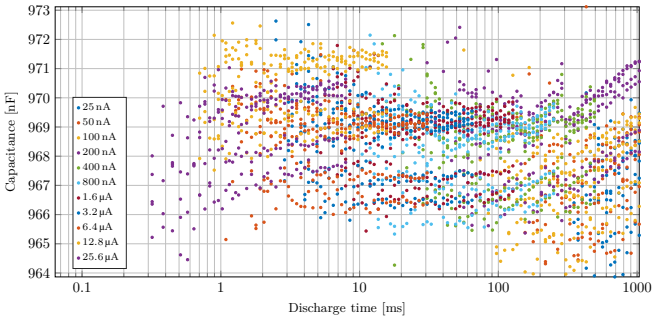

Fig. 6. Estimated values of C_P (average of 32 measurements in the same conditions), resulting from 192320 measurements, using an automated setup.

The results reveal that the calculated values of C_P vary between 963.9 nF and 973.1 nF, corresponding to a variance of ±0.47 % around the average value of 968.5 nF, or a maximum relative error $\eta_{c_p\text{-lin}} = 0.005$. Since C_P was calculated to match the currents imposed by the source meter, the maximum systematic error corresponds to the uncertainty of these currents. In this case, the relative error $\eta_{c_p\text{-syst}}$ is 0.0006.

C. Validation of error model

This validation was performed by analyzing again the same 192 320 data pairs $(v_i,\ v_f)$, now with information about the value of C_P, σ, $\eta_{c_p\text{-lin}}$ and $\eta_{c_p\text{-syst}}$.

Using the estimated value of C_P and the data pairs $(v_i,\ v_f)$, the measured current for each measurement was calculated. Figure 7 depicts the calculated current values (average of 32 samples) as function of "true" current and Δt. The graph shows, qualitatively, that the measured currents converge to the expected values as the charge integration time increases, and, therefore, Δv increases. The line shown in the graph represents the minimum measured current, for a given Δt, for which the expected $\eta_{\Delta v\text{-rand}}$ is less than 0.1, according to Equation (8). Therefore, a large dispersion is accepted in the measured values to the left of the line, as a maximum error of more than 10 % is expected.

To evaluate that the error in measurements can effectively be predicted by Equation (12), the maximum expected relative error (or accuracy), k, of each measurement was calculated assuming:

- $\eta_{c_p\text{-lin}} = 0.005$, as experimentally measured in Section VII-B.
- $\sigma = 98.9\,\mu\text{V}$, as observed in the data set.
- The true values of the measured currents are the currents imposed by the source meter. Therefore, $\eta_{c_p\text{-syst}} = \eta_{\Delta v\text{-syst}} = 0$. In fact, a systematic error exists, and an upper bound of such error was calculated in Section VII-B. However, it cannot be observed, because it is the "assumed-true" value that contains that error component. Furthermore, C_P was determined in a way that the measured currents are calculated from the $(v_i,\ v_f)$ pairs with a systematic error of 0.

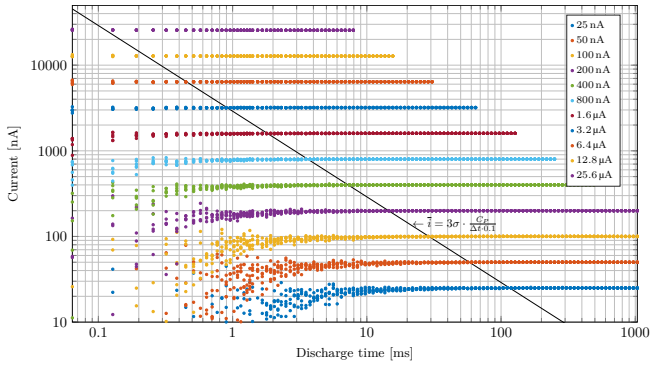

Fig. 7. Measured current as function of discharge time, at 3.0 V (average of 32 samples).

The results of all 192320 measurements show that only 212 measurements are outside the guaranteed range of accuracy predicted via Equation (12), corresponding to 0.11 %. Considering the size of the dataset, these results validate the previously made error analysis. Figure 8 presents the relative error of part of these measurements, obtained for one load (200 nA), and a plot of the minimum guaranteed accuracy for that specific load and each charge integration time.

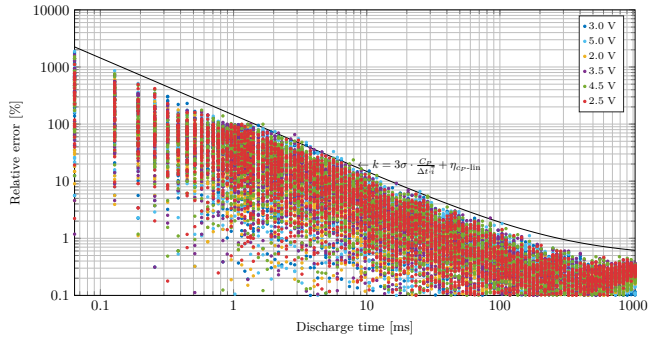

Fig. 8. Relative error of all measured current values for a load of 200 nA as function of discharge time.

D. LCD current measurement

The LCD requires an alternate stimulus from a positive and a negative supply. The measurement of LCD currents is made possible by using 2 independent capacitors: one charged with a positive voltage and one with a negative voltage. Both of the capacitors are connected to the DUT, alternately, to create a square waveform. The frequency of the waveform is directly controlled by the microcontroller and the test voltage is controlled by initially charging the capacitor with a predefined voltage. After operation during a given number of cycles, the LCD is disconnected and the voltages in the capacitors are measured for determination of the average current.

The same principles and equations that were presented for the general case are still valid. However, by having the CMOS switches toggle multiple times, a new source of error is introduced, consisting of charge injection due to parasitic capacitances. This error is mitigated, by performing one additional measurement in each test condition without the LCD, and latter compensating for the observed voltage drop in this measurement.

The data that was collected during the selection of the LCD display allowed to obtain initial estimations about the LCD current consumption. Depending on the source of information used, a wide range of currents was expected. Some sources indicated currents close to 10 times higher than the lowest estimations. This discrepancy served as motivation to the analysis that is made in this paper. The results of the measurements are presented in Table I.

	32 Hz	64 Hz	96 Hz
3 V	186 nA	361 nA	537 nA
4 V	277 nA	539 nA	799 nA
5 V	364 nA	707 nA	1049 nA

TABLE I

Current of the LCD measured experimentally. The presented results correspond to the current of 28 active segments scaled by a factor of 0.56 to be directly comparable to the theoretical predictions.

Two methods for estimating the current were used, based on the data provided by the manufacturers — using current per area approach and using a capacitance per area approach. Both approaches revealed to be conservative. Nevertheless, the purpose of the data provided by the manufacturers is not accurately predict the current, but provided an upper bound instead, yet as close as possible to the typical value. This is, indeed, achieved.

VIII. Conclusions

In this thesis work, the electronic system of a desk clock, powered by a button battery, was designed. The clock was specified to be used as a marketing gift and demonstrator of the real-time clock (RTC) of Silicongate Lda. Given the limited energy available in the small battery, it is very important for the autonomy of the clock that the complete electronic system is designed targeting ultra-low power operation. The RTC of Silicongate Lda requires 200 nA of supply current and the remaining electronic system designed in this thesis work (the LCD with its drivers and the control logic) was specified to require approximately the same current.

The work fully achieved the proposed objectives, with an efficiency of 93.7 % at 25 °C measured as the ratio between the current at the LCD's terminals and the current supplied to the complete circuit (including LCD drivers, control logic and enabling circuits). The proposed method for measuring currents was used to measure the current consumption of the LCD, isolated from the demonstrator, allowing a complete specification of its current requirements and high confidence on the obtained results.

The digital control was validated in a CPLD prototype and the masks required for the fabrication in GlobalFoundries' 22 nm FD-SOI technology were designed. The design of the digital part started with the state machine and included also the porting of digital cells for the target technology and their characterization, as well as the backend place and route. A technique of body-biasing was employed in the digital cell library, allowing further optimization of the leakage current. This feature will allow future studies, on a silicon-level, of the impact of body-biasing in transistor performance and consumption.

Three original contributions are identified in this thesis work:

1) A low noise, high efficiency, LCD driver that minimizes the noise on digital and analog supplies that is common to the RTC. This feature is achieved using the proposed feed forward, multiple phase control solution.
2) A frequency monitor solution that protects the LCD from static or excessive DC, due to erroneous duty-cycle, was proposed and validated.
3) With the purpose of measuring the LCD current, an ultra-low current measurement solution was proposed and evaluated. Error sources in the proposed current measurement solution are analytically and statistically analyzed with experimental data, validating the proposed design method for a given target current measurement accuracy.

Each of these original contributions of this work are currently submitted to scientific conference or journal papers (1 and 2 to Design of Circuits and Integrated Systems (DCIS) 2018 and 3 to Journal of Instrumentation).

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