Manifold reuse of silicon substrate in the layer transfer process with porous silicon

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Abstract

Considering the rapid depletion of fossil fuels the importance of renewable energy is rising. Solar photovoltaics (PV) are on the forefront of the new energy technologies that are considered green. A major disadvantage of PV, especially of the prevalent silicon PV technology, is that it is still very costly and the production is difficult due to the very specific conditions needed for a good cell to be achieved.

To reduce the overall cost of production, many new concepts for solar cells have been developed. Organic photovoltaics, dye-sensitized, CIGS and other thin-film solar cells are clear representative of such attempts. While those technologies are/have the potential to be cheaper, that also comes at certain costs like lower stability, lifetime and efficiency. On the other hand the current silicon PV technologies are on the opposite spectrum where the material and production costs are a limiting factor in the adoption of the technology. Thus a method for reducing the material expenses is a viable solution to making silicon solar cells more accessible. Such is the i^x-module concept where it is predicted that the amount of silicon (Si) used for the creation of a cell will be 10 times less than that needed for the current state-of-art silicon cells. There a thin-film of silicon is being epitaxially grown with CVD on a substrate. Afterwards, the film is being detached and further processed into a highly efficient solar cell, while the parent is further re-used for the growth of another thin-film. Theoretically the number of re-uses is in the order of several hundreds.

The current work presents the first steps taken into the realization of successful substrate re-use. It delineates the challenges that need to be overcome as the occurrence of various defects and undesirable features and discusses the steps taken into solving them. While doing this, multiple re-use has been carried out and its feasibility has been proven.

Keywords: layer transfer process, epifoil, thin film, crystalline silicon, solar cell, photovoltaics, porous silicon

1. Introduction

Before taking a deeper look at the re-use of substrates one should obtain a better understanding of the layer transfer process (see figure 1a):

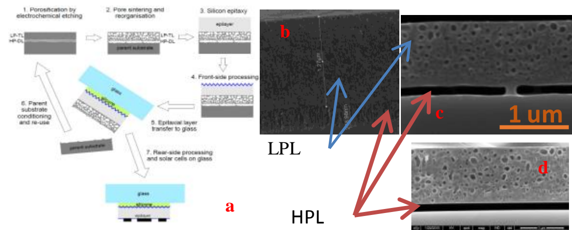

Figure 1 a) Processing steps in the LTP using porous silicon as a template and sacrificial layer as is used in imec (courtesy of H.S. Radhakrishnan[1]) b) double stack of porous silicon after anodization c) and d) double stack pSi after sintering (a pillar is visible on c))

1. The first step consists of electrochemically etching the parent substrate in order to obtain two layers of porous silicon (crystal orientation of the Si wafer is (100)). The top one is termed the low porosity layer (LPL or LP-TL i.e. low porosity – template layer) with porosity percentage at imec of about 20 to 30 and a varying thickness from ~300nm till 2um. The bottom layer is called the high porosity layer (HPL or HP-DL i.e. high porosity – detachment layer). It is 60-70% porous and much thinner than LPL – about 300-400 nm.(figure 1b) The tool used is Porous Silicon System MPSB, manufactured by AMMT[2]. After formation of the porous layers, the samples are sintered at high temperatures in an epitaxial reactor Epsilon 2000 (produced by ASM)[3], whereas can be seen from the figures 1c and 1d – dramatic structural changes ensue. The pores in the low porosity layer(LPL) close off and reorganize in spherical voids entrapped in a monocrystalline/quasi-monocrystalline matrix[4]. The top layer of the sintered LPL serves as a template for the consequent epitaxial growth of Si. As to the bottom high porosity layer (HPL) – there the transformation is even more drastic since the pores have reorganized into large extended void interrupted only by tiny pillars spaced far apart from each other. This makes the HPL structurally weak and easy to remove hence its function as a detachment/sacrificial layer. More information onto the enchanting physics of forming and further sintering porous silicon (pSi) can be found in [5].
2. After several minutes of annealing of the porous silicon under high temperatures when the pores from the top of the LPL have successfully closed off and the resulting surface is of sufficient smoothness, the growth through chemical vapour deposition (CVD) of epitaxial silicon begins. The grown thin film can be of

various thicknesses though at imec it normally is between 30-50um.

3. After the growth of a high quality epitaxial thin Si film, its top side is processed as the processing of a front-side of cell. In the case of an interdigitated back contact (IBC) design, this includes texturing, surface passivation and deposition of an antireflective coating.

4. The next step includes the bonding of the processed sample to a glass carrier/superstrate. After this has been completed, the foil is detached from its silicon parent substrate through the application of force. The fracturing is confined in the high porosity detachment layer due to its structural weakness.

5. After detaching the foil from its parent substrate, the latter can be easily conditioned and re-used again. Theoretically, a considerable number of reuses are possible (see figure 2 left). The re-use of the substrate is the main topic of this work and will be extensively dealt with in the following paragraphs.

6. The foil has been detached and remains glued on the glass which provides it with structural integrity during subsequent processing which involves the back-side processing steps for an IBC cell. The end result is a highly efficient solar cell requiring minimal amount of materials(figure 2 right).

Figure 2 From left to right: porosified 8inch wafer, free-standing epifoil(19 cm diameter), bonded epifoil (11cmx11cm) on a glass substrate.

2. Re-use of parent substrate:

The re-use of the parent substrate is an essential step towards the successful implementation of the LTP with porous silicon since it is the step where most of the Si is being saved compared with traditional wafer sawing techniques. Despite the critical importance of the process, the literature on re-use of substrate is quite limited. The reported data is often very superficial and insufficient for a general overview of the technology used to be obtained. So far multiple re-use has been reported by the companies Solexel [6],[7] and Crystal Solar [8],[9] and by Brendel et al. in ISFH[10]. The former two reported over 50 re-uses for a single wafer with no noticeable decrease in the quality of the foils, while the latter demonstrated 13-fold re-use of a single substrate.
It is generally hard to compare the progress outlined in the current work with the work of the above teams for mainly two reasons: 1) difference is processing equipment and conditions, 2) variation in the process methodology. This paired with the little information provided on the challenges that the teams faced makes it hard to measure the development stage that imec is currently at.
In order for a substrate to be successfully re-used, it has to be properly treated after detachment of the foil so that its end condition should resemble as close as possible its original one before the porosification step. This can be translated into the following criteria:

- The surface of the parent should be smooth enough so that it is comparable to its original smoothness.
- Following the previous prerequisite, it should be added that there should be no surface defects.
- The parent should be mechanically and structurally strong to endure the subsequent processing for many numbers of cycles.
- The doping concentration profile of the parent should be should be as uniform and at the same values of concentration as it was during its original state.
- Desirably, the amount of defects near the surface and the bulk of the substrate(micro-cracks, dislocations, boron- oxygen precipitations) should not be drastically increasing, as to allow large number of re-uses with the production of high quality foils.

2.1. Detachment:

There are many ways to detach a foil in the pSi LTP.
In imec there are generally three techniques which are being used after first laser scribing the desired detached area. All of them utilize a similar principle. Start a crack at the laser scribe and initiate its propagation by mechanically pulling the foil and the parent away:

- Manual detachment – the parent is being gently twisted and bended and thus various stresses are induced which result in the breakage of pillars and consequent detachment of the foil. Such method is crude for several reasons:
1) every wafer is being detached in a different manner i.e. resulting stresses from bending vary in strength and direction for each particular sample. This impedes accurate measurement of yield and exact comparison between samples.
2) it increases the risk of introducing contaminants on the foil and the subsequent equipment. 3) According to the experience of the author, a well-developed vacuum chuck detachment might accomplish better yield 4) the method can be highly time consuming and its yield often depends on the skills of the operator.

- Gluing the whole substrate-foil structure to a glass and then mechanically separating them. The foil remains on the glass. A variation of the technique is instead of the mechanical pull between the glass and substrate, to put them in ultrasonic bath where the vibrations contribute to the breakage of the pillars. This is often used as an alternative method to manual detachment since a degree of conformity of detachment conditions among the samples can be introduced.

- Using a vacuum chuck which is covered by the still attached foil. When a pump is connected to the chuck, its suction is enough to keep the foil attached to the chuck while the parent is being mechanically separated. The author had started developing this method while working in imec. The chuck is a microporous vacuum one, produced by Horst-Witte [11]. The sample, after being laser scribed is being put on the chuck. After starting the

pump, suction is applied on the epifoil which upon lifting of the substrate remains on the chuck.

A comprehensive discussion regarding the mechanical characterization of detachment with regards to the methods used in imec has been introduced by H.S. Radhakrishnan [12]. There he performs a COMSOL simulation of stresses induced during detachment. The stress distribution profiles are shown in the figure 3.

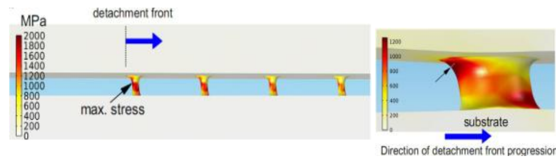

Figure 3 Stress mapping of Si pillars: (left) the pillars closest to the detachment front, (right) close-up mapping of a single pillar. Note: Pillars have width of 0.1 um and spacing between them is 1 um. (obtained from [12]).

When assuming that the areas with highest stress concentration are the most probable ones for crack initiation and propagation, the map presented agrees very favourably with observations made on detached substrates and foils.

Below in figure 4 are shown several surface features that can be observed on the detached substrate that are representative for the possible crack propagation paths in the detachment layer. In 4d) one can observe a typical path of crack propagation that goes straight through the pillar. Nonetheless, when the stress at the upper part of the pillar is sufficiently high, an alternative path is formed (4a and 4b). There the crack propagates into the sintered low porosity (LP) layer since structurally it is weaker than bulk crystalline silicon. For simplification purposes such structure will be called "mushrooms" or hillocks. One can also observe that in b) there are actually two pillars close to each other. Such conglomerations of pillars have been monitored many times over the experiments and later in the chapter their origin will be discussed in more detail.
Figures 4c and 4f show the least favourable outcome of detachment where after the crack propagated into the porous layer, it continued into the bulk silicon and thus generally, either perforated or cracked the epifoil thus rendering it unusable for further cell processing. The ensuing feature has been named “large hillock”. The last possible path for crack spreading is under the pillar as shown in e). The resulting formation will onwards be named "pit".

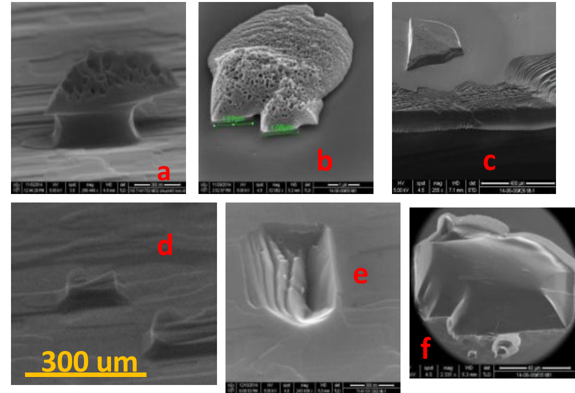

Figure 4 Variations of crack propagation front in the detachment of epifoils resulting in most common features/defects on the substrate's surface.

Martini [13] and Radhakrishnan [12] have both identified correlations whether the crack will propagate through the pillars (desirable) or deviate into the LP layer or the bulk of the substrate. Whenever the pillars are too think or too closely spaced, the crack propagation is always in the less desirable path (above or under the pillars). Such notions were observed and confirmed during the conduction of the experiments for this work.

2.2. Searching for a solution:

When looking for a suitable etch solution that would successfully polish the substrate for further re-uses, it was decided to use in parallel two etchants available at imec – one alkaline and one acidic. In this way it could be checked whether the isotropic or anisotropic manner of Si dissolution will be most beneficial for suitably conditioning the substrate's surface. Similar approach has been undertaken in ISFH [10]. Multiple experiments were to be run testing different concentrations, etching times and temperatures for both types of solutions. The primary goal was to investigate which conditions produce the best surface quality and dispense in the best manners of the defects described in the previous chapter.

After conducting the preliminary tests for choosing process parameters for the alkaline and acidic solutions etches, they were tested in real re-use experiments. Below are discussed some brief overviews of the selection processes of the etchants and consecutively how they dealt with some of the worse surface defects.

An important note is that after detachment all of the samples undergo vigorous cleaning procedure of two sequences of 10 min dip in SPM and 2 min dip in HF/HCl/H_2O. SPM (sulphur peroxide mixture) known also as "piranha", is a 1:4 volume ratio of H_2O_2: H_2SO_4. The mixture is excellent for removing any organic contaminants from the substrate. HF/HCl/H_2O (subsequently called HF-dip) has volume ratio of 1:1:20. The sequence of SPM and HF dip with deionized water rinses in-between is also known as imec clean[14].

<u>Tetramethyl Ammonium Hydroxide (TMAH):</u>

As an alkaline solution of choice, TMAH is a very suitable for polishing. Nonetheless, it is not that very cheap. A more economical solution would be KOH which is in many ways similar to TMAH(albeit somehow more difficult to handle), but the deciding factor for using TMAH was that the ix-module team, as well as the author, had already acquired expertise in working with the material utilizing it for etching of sintered pSi and seed layers on foils. It was concluded that once the use of TMAH was well-investigated, a switch to KOH would be comparatively uncomplicated.

It is known that the etching rate for n-type Si is slightly higher than that of p-type Si[15]. Also the etch ratio of (100)/(111) planes decreases with the increase of concentration and temperature reaching a minimum at 25% TMAH. This results in the (100) planes of the samples to be covered with hillocks when the concentration is below 15% w.t., but smooth surfaces can be obtained for concentrations above 22% w.t.[16].

Worthy of note that the wafers used in the experiments were highly doped p-type (100) crystalline Si. Multiple tests were carried out. The varying parameters were the concentration of TMAH in an aqueous solution, the etching time and the working temperature. The main concentrations used were 2% w.t. and 25% w.t.. The temperatures used were either room temperature or high temperature in the range of 75-80 °C.

Important to note is that before each etch the samples were dipped for 1 min in a low concentration aqueous solution of HF/HCl in order to remove the native oxide since TMAH has a very low etch rate on it.

The best results were achieved with 15 min etch of 25% TMAH at a temperature of 75-80 °C, where the etch rate was calculated to be around 0.33 um/min for the p++ bulk of the wafer. The etch rate was found to be very satisfactory since not a lot of material was being removed while still managing a good quality surface. Nonetheless, in the future, it will be beneficial to further fine-tune the process so that even less material be removed and thus increasing the theoretical number of possible re-uses for a wafer. Lower concentrations, temperature and etching times resulted in a bad quality surface: pyramid formations and various defect delineations.
However, after the TMAH etch, the surface has been well-smoothened and many of the smaller hillocks have been removed. The size of the large ones has also visibly diminished.

In the red circle in fig. 5a is shown a large hillock with area of approx. 50µm x150µm. In fig. 5b it can be seen that the hillock has been etched away. Images 5c, d and e are gradual close-ups of the surface where the hillock was. It can be seen that there is a small bump and some pSi on top of it. Considering the fast etch rate of pSi under TMAH (mainly because of the large surface area) it can be safely assumed that the hillock was in fact undercut and whatever that was left of it was removed when the sample was taken out of the solution. Again it is important to note that despite the unsuccessful removal of the large hillocks from the surface, the image is actually a proof that under the chosen condition TMAH can actually successfully condition most of the re-use samples which lack such severe surface defects.

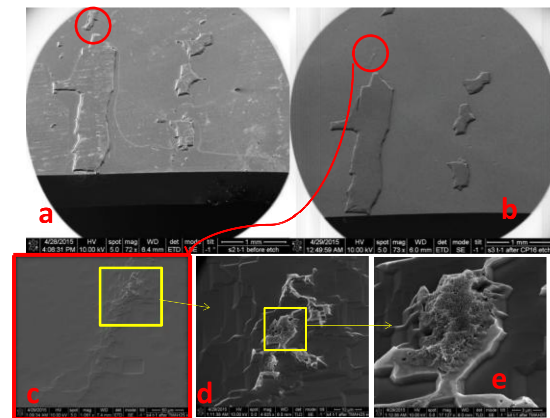

Figure 5 XSEM imaging of sample before and after TMAH etch. Hillocks.

Regarding the elimination of large pits, the results have been somewhat ambiguous. XSEM measurements have shown clear expansion of the etched pits, but a profile measurement is needed in order to determine whether they are deeper than before the etching though it should be of the same depth as before since both bottom of the pit and the surface above it are (100) oriented. Nonetheless, the widening of the features is always good because it will introduce fewer defects in the next foil after re-use because after etching the bottom of the pit has become visibly more faceted. Such abrupt change in profile will surely introduce dislocations into the epitaxial foil during CVD deposition (see fig. 7).

Chemical Polish (CP):

The acidic solution chosen to be tested was CP i.e. Chemical Polish. The one used was a mixture of nitric acid (HNO_3), HF and acetic acid (CH_3COOH). Normally, it is denominated as CPX where X is an integer denoting the following volume ratios 70% HF: 50% HNO_3: CH_3COOH = 1:X:1. Therefore the higher the integer X, the bigger amount of HNO_3 in the solution. The lower the concentration of HF in the solution, the lower the etch rate. This combined with the isotropical character of the etchant make it widely used for etching the back side of polycrystalline Si solar cells. The acetic acid in the solution has high viscosity and thus facilitates smoother surfaces [17]. So far only low p/n selectivity has been observed [18]. For the testing, 4 different variation of CP with varying etch times were investigated: CP4, CP8, CP16 and CP32. Before etching the solution was left for about 30-60 min to condition in order to ensure the measurement of more consistent etch rate. Polishing capabilities and the etch rate of the solutions decreased with the decrease of HF concentration. Nonetheless, CP16 was chosen as a suitable solution with satisfactory polishing capabilities and a lower etch rate of about 2-3 um/min. the timing of the etch was chosen to be 2 min, thus limiting the removed material to about 4-6 um of depth.

Under the particular conditions used, CP16 also yielded positive results. The micrograms in figure 6 show how a large hillock (fig. 6a) has been removed. In its place is left a small bump (fig. 6b). Taking count the near or complete isotropic manner of the etchant, it can be easily deduced the height of the bump should not be larger than 4-6 um. The remaining porous silicon on top and the small amount of crystalline Si (fig. 6c) signifies that the hillock was indeed undercut and consequently removed during the movement of the sample in the solution.

Again, it is important to note that this result is significant because it means that smaller surface defects are easily eliminated with the quality of the surface remaining good.

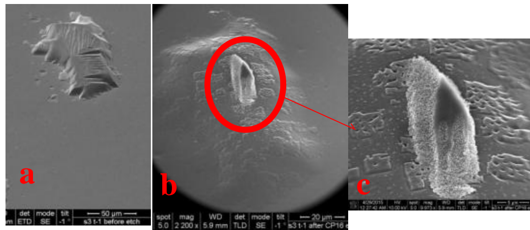

Figure 6 XSEM imaging of sample before and after CP16 etch. Hillocks.

Regarding the elimination of pits, analogously with TMAH, CP16 also yields somewhat ambiguous results. Comparing the investigated pits before and after etch, it seemed that the features had become "smoother", especially the surfaces around them. Nonetheless, it could not be confirmed without profile mapping in order to compare the relief before and after etch.

3. Results. Quality of epitaxy:

When using CP 16 as a conditioning agent for the substrate, it has been found that the resulting epifoils have a mirror-like polished look. That is not so true for substrates treated with TMAH, where the re-use epifoils do not have a polished look. Nonetheless, during XSEM inspection it was found that the roughness of the surface is considerably small, though no profilometry was performed in order to quantify it. Nonetheless, without knowledge on the effective carrier lifetime and defect density of the bulk, it cannot be concluded with certainty whether the quality of the surface of the re-use epifoils is good or bad.

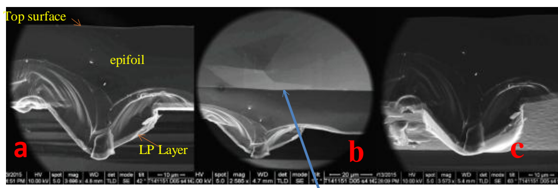

Figure 7 Epitaxy over a pit: XSEM imaging from 3 different angles showing how a defect in the substrate transfers onto the foil.

Figure 7 is important since it is a proof that foils can be produced and detached even if grown on surface with great deformations such as is a pit. Nonetheless, it has not yet been determined how detrimental this feature is on the quality of the foil, nor the exact way that the crystalline structure of the silicon has been impacted. Upon completion of the thesis, the sample had been prepared for TEM (transmission electron microscopy[19]) which would provide useful information on the crystal structure of Si in the feature. After looking at the local growth of an epifoil above a pit, it is logical to investigate how a hillock which has not been completely removed will influence the formation of an epifoil above it.

Figure 8 shows just that. Images a) and b) are SEM micrograms of such a feature and one can easily observe the delineation of the hillock among the Si of the epifoil (see fig 8c). There also can be noted two generations of porous silicon – the original pSi stack of the hillock is on top while underneath is located the current pSi stack (the one over which the foil was grown).

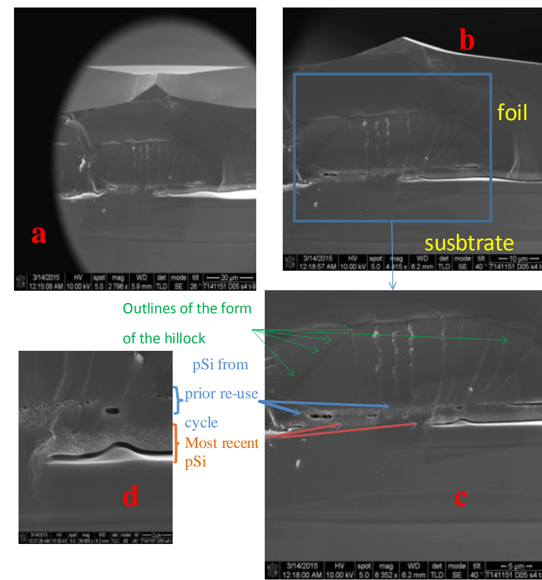

Figure 8 Epitaxy over a hillock: XSEM images, a) and b) show the stacking faults induced, which protrude from the epifoil's. top surface as a hillock. c) and d) -two generations of pSi.

4. Conclusions

The main goal of the current work was to demonstrate multiple re-use of a substrate for the production of epifoils while using LTP methodology. This was achieved. Several substrates were re-used 3 times. For that purpose, two suitable solutions for the reconditioning of the substrates were developed. Both solutions (TMAH and CP16) exhibited subjectively good performance in polishing the substrates and removing some of the defects and features off their surfaces. It was shown that small pits, pillars and hillocks were easily removed. Defects like large hillocks and pits were not always being removed and their effect on the formation of the new epifoil was shown. Of course it is worthy to note that the occurrence of such large defects was not very usual (between 10-20%, depending on batches). Nonetheless, tackling them is of great significance since they present an obstacle towards achieving sufficiently high yield (>

95%) in order to make the LTP suitable for industrial production.

Next steps towards a more precise evaluation of the process methods proposed in the current work are needed. It is important to note that relevant parameters that inform on the quality of the foils produced were not monitored, namely effective minority carrier lifetime and defect density. This occurred due to reliability issues with the in-house lifetime measurement procedure and the absence of appropriate defect etching solution. However, all the samples obtained during the preparation of this thesis have been carefully preserved so that as soon as the above issues get cleared, appropriate measurements will be done. Those should be the first future steps towards building on the current work.
Other characterization technique to be used on the epifoils during re-use cycles is Transmission Electron Microscopy (TEM) which will give valuable information about the Si lattice orientation in particular parts of the epifoil.

Important for the yield of detachment as well as the number of defects on the substrate surface is the detachment method. A vacuum chuck detachment procedure was started to be developed by the author. Once fully implemented, it will certainly improve not only the overall yield, but also the homogeneity of the substrate's surface.

Another possible action that will improve those two parameters is if different pSi stack is implemented. The current one consists of low porosity (LP) and high porosity (HP) silicon. If changed to LP, HP and LP silicon, then after thermal annealing the stack will reorganize into a detachment layer between to sintered LP layers. Such configuration will allow for better control of defects produced during detachment: pits and some hillocks will no longer be a big issue because they will be made of porous silicon which is really easy to etch away i.e after conditioning of the substrate, the resulting surface will be smoother through the undercutting of those large defects. Additionally, having two LP porous layers between the DL will provide more options for crack propagation, resulting in possibly smaller number of hillocks. Such stacks have already been created by Tayanaka et al. [20][21].

Further work on tuning the solutions for substrate reconditioning will for certain be needed along with trying out some new ones like polyetch, KOH, etc, since the ones developed in this work are far from ideal.

Early anticipation of further challenges can be beneficial so that a solution can be offered in a timely manner. Such a challenge can be the reduced mechanical integrity of the substrate throughout the re-use cycles. Increase in boron-oxygen precipitations can as well pose an issue for the foil quality after multiple re-use.

5. Bibliography:

[1] H. S. Radhakrishnan, "Silicon Epitaxial Layers Grown On Buried Porous Silicon Templates For Solar Cells," KU Leuven, 2014.

[2] "Porous Silicon Etching – AMMT." [Online]. Available: http://www.ammt.com/products/porous-silicon-etching/mpsb/. [Accessed: 15-Nov-2015].

[3] "Epsilon Epitaxy." [Online]. Available: http://www.asm.com/solutions/products/epitaxy-products/epsilon-epitaxy. [Accessed: 15-Nov-2015].

[4] K. Van Nieuwenhuysen, I. Gordon, T. Bearda, C. Boulord, M. Debucquoy, F. Dross, J. Govaerts, S. Granata, R. Labie, X. Loozen, R. Martini, B. O. Sullivan, H. S. Radhakrishnan, and K. Baert, "High-Quality Epitaxial Foils , obtained by a Layer Transfer Process , for Integration in Back-Contacted Solar Cells processed on Glass," pp. 1833–1836, 2011.

[5] I. Sharlandzhiev, "Manifold reuse of silicon substrate in the layer transfer process with porous silicon," Instituto Superior Tecnico, 2015.

[6] H. Fatemi and Solexel Inc., "Productization and Manufacturing Scaling of High-Efficiency Solar Cell and Module Products Based on a Disruptive Low-Cost , Mono-Crystalline Technology Final Technical Progress Report Productization and Manufacturing Scaling of High- Efficiency Solar Cell," 2012.

[7] "http://engineering.case.edu/centers/sdle/sites/engineering.case.edu.centers.sdle/files/solexel_thin-silicon_solar_startup_lands_31m_more_in_vc_funding_greentech_media.pdf." .

[8] R. Hao, T. S. Ravi, V. Siva, J. Vatus, D. Miller, J. Custodio, K. Moyers, C.-W. Chen, A. Upadhyaya, and A. Rohatgi, "High efficiency solar cells on direct kerfless 156 mm mono crystalline Si wafers by high throughput epitaxial growth," in *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, 2014, pp. 2978–2982.

[9] T. S. Ravi and I. Crystal Solar, "Technology Development for High-Efficiency Solar Cells and Modules Using Thin (< 80 μm) Single-Crystal Silicon Wafers Produced by Epitaxy," 2013.

[10] V. Steckenreiter, J. Hensen, A. Knorr, E. G. Rojas, and S. Kajari-Schröder, "Reconditioning of silicon substrates for manifold re-use in the layer transfer process with porous silicon," in *The 22nd International Photovoltaic Science and Engineering Conference*, 2012, pp. 1–4.

[11] "https://media.horst-witte.com/cms-downloads/en/2014/Vakuumkatalog-2014-05-ENG_screen.pdf." .

[12] H. Sivaramakrishnan Radhakrishnan, R. Martini, V. Depauw, K. Van Nieuwenhuysen, T. Bearda, I. Gordon, J. Szlufcik, and J. Poortmans, "Kerfless layer-transfer of thin epitaxial silicon foils using novel multiple layer porous silicon stacks with near 100% detachment yield and large minority carrier diffusion lengths," *Sol.*

Energy Mater. Sol. Cells, vol. 135, pp. 113–123, Apr. 2015.

[13] R. Martini, “Study of crack propagation for the fabrication of ultra-thin silicon solar cells,” KU Leuven, 2014.

[14] M. Meuris, S. Arnauts, I. Cornelissen, K. Kenis, M. Lux, S. Degendt, P. Mertens, I. Teerlinck, R. Vos, L. Loewenstein, M. M. Heyns, and K. Wolke, “Implementation of the IMEC-Clean in advanced CMOS manufacturing,” in *1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings (Cat No.99CH36314)*, 1999, pp. 157–160.

[15] J. T. L. Thong, W. K. Choi, and C. W. Chong, “TMAH etching of silicon and the interaction of etching parameters,” *Sensors Actuators A Phys.*, vol. 63, no. 3, pp. 243–249, Dec. 1997.

[16] O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugiyama, “Anisotropic etching of silicon in TMAH solutions,” *Sensors Actuators A Phys.*, vol. 34, no. 1, pp. 51–57, Jul. 1992.

[17] M. S. Kulkarni and H. F. Erk, “Errata: ‘Acid-based Etching of Silicon Wafers: Mass-Transfer and Kinetic Effects’ [J. Electrochem. Soc., (147), 176],” *J. Electrochem. Soc.*, vol. 147, no. 8, p. 3166, Aug. 2000.

[18] V. Lehmann, *Electrochemistry of Silicon: Instrumentation, Science, Materials and Applications*. Wiley, 2002.

[19] L. A. Kosyachenko, *Solar Cells - Silicon Wafer-Based Technologies*. InTech, 2011.

[20] H. Tayanaka, K. Yamauchi, and T. Matsushita, “Thin-film crystalline silicon solar cells obtained by separation of a porous silicon sacrificial layer,” *Proc. 2nd World Conf. Photovolt. Sol. …*, pp. 1272–1277, 1998.

[21] R. Brendel, *Thin-Film Crystalline Silicon Solar Cells: Physics and Technology*. John Wiley & Sons, 2011.